Application Note
RS422/RS485 Transceiver
AN-CM-220

Abstract
This application note shows how to implement an integrated transceiver for RS422/RS485 protocols using a Dialog GreenPAK™ SLG46533V. This application note comes complete with design files which can be found in the References section.
RS422/RS485 Transceiver

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1 Terms and Definitions

TIA           Telecommunications Industry Association
EIA           Electronic Industries Alliance
IC            Integrated circuit

2 References

For related documents and software, please visit:

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Dialog Semiconductor provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Dialog IC.

RS422/RS485 Transceiver

3 Introduction

Digital communications are the most used method to share data between devices. There are several standard buses to implement them and the main differences between them are data rate and noise sensitivity. On industrial applications, or environments with high noise levels, noise interference is one of the most important problems for the communication systems. This is the main reason to choose differential buses, where the sensitivity to noise is greatly reduced.

RS485, also known as TIA-485(-A) or EIA-485, is a standard defined by the Telecommunications Industry Association and Electronic Industries Alliance (TIA/EIA). It is based on balanced electrical signaling (a differential bus) which can be used effectively over long distances and in electrically noisy environments such as industrial environments.

RS422, also known as TIA/EIA-422, is a standard defined by the same associations of the RS485 that specifies electrical characteristics of a digital balanced signaling circuit. This bus is very similar to RS485. The main difference is that the RS485 can implement linear bus topologies with only a twisted pair of cables.

These buses are commonly used with embedded systems which implement half-duplex asynchronous serial communications. To do this, a conversion from single-ended buses to differential buses must be used.

There are several different brands of commercial IC’s that implement the single-ended to differential bus conversion. This is a simple way to convert RS232 compatible buses to RS422/RS485 bus. These IC’s are called RS422/RS485 Transceivers.

In this application note, the digital logic required to implement an integrated transceiver for RS422/RS485 protocols converting single-ended to differential data when transmitting or differential to single-ended data when receiving, managed by control signals is implemented. To implement this, we used a Dialog GreenPAK SLG46533V.

The implemented system has two differential input/outputs as the interface to the RS422/RS485 bus, one control signal for flow data control and one serial data input (Tx to the bus) and one serial data output (Rx from the bus) as the interface to the single-ended bus. With this implementation, the SLG46533V will work as a Transceiver, replacing commercial IC’s.

4 Differential Communications

On serial communication buses, there are two basic forms of data transmission circuits, called single-ended bus and differential bus.

Single-ended or unbalanced circuit, shown in Figure 1, determines the bus state by the voltage difference between the signal line and common local ground. In the same figure, the electrical schematic diagram of a single-ended transmission circuit and the noise sources V_N and V_G are shown. Noise voltages are added directly to the signal voltage, V_S.

![Figure 1: Single-Ended Bus Schematic](image-url)
A differential or balanced circuit is shown in Figure 2. In this case, the bus state is determined by the voltage difference between two complementary signal lines. In the same figure, the electrical schematic diagram of a single-ended transmission circuit and the noise sources $V_N$ and $V_G$ are shown. Noise voltages $V_N$ and $V_G$ are added to each signal line and are common to both signals.

\[
V_{IA} = V_{SA} + V_G \\
V_{IB} = V_{SB} + V_N + V_G
\]

The differential receiver measures the difference between the two lines. The received signal voltage results:

\[
V_{RX} = V_{IB} - V_{IA} = V_{SB} - V_{SA}
\]

In this case, input voltages to the receiver stage result:

In Figure 1 it can be seen that single-ended buses are susceptible to external noise influences. Also, due to no complementary signal presence, the electromagnetic fields created by the single-ended signal are not canceled, so it radiates much more noise than differential circuits. Electromagnetic noise susceptibility and emissions relegate single-ended interfaces to low signaling rates and short transmission lines.

It can be seen that the differential receiver rejects the common voltage of the signals. If this bus type is used with closely coupled lines, the complementary signals cancel each other’s noise resulting in high immunity and low noise emissions.

This immunity to external noise influence are the main reason for choosing differential signaling when relatively high signaling rates and long distance are required in electrically noisy, or noise-sensitive applications. The disadvantage of differential buses is the additional cost of the line driver, receiver, and interconnection if it is compared with the cost of single-ended transmission buses.

5 RS422/RS485 Bus

RS422 and RS485 are very similar differential bus standards defined by the Telecommunications Industry Association and Electronic Industries Alliance (TIA/EIA). The first published standard was the RS422, but due to the lack of bidirectional capabilities allowing for multipoint connections, the RS485 was created as an evolution of the RS422.

The standard RS485, also known as TIA-485(-A) or EIA-485, defines the electrical characteristics of the interconnection, including driver, line, and receiver. It allows data rates up to 35 Mbps and line lengths of up to 1200 mts. As it is expected, both limits cannot be reached at the same time. There are several recommendations about wiring and termination. The standard does not specify the connector or any protocol requirements.
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RS485 standard defines a half-duplex and differential transmission method designed for twisted-pair cables and other balanced media. The standard requires drivers to deliver a minimum differential output voltage of 1.5 V with up to 32 unit loads of about 12 kΩ each, plus termination resistors at each end of the bus.

In contrast to RS422, which has a single driver circuit which cannot be switched off, RS485 drivers use three-state logic allowing individual transmitters to be deactivated. This allows RS-485 to implement multipoint linear bus topologies using only two wires.

The linear bus topology is often based in a master-slave arrangement where one device (the master device) initiates all communication activity.

As explained before, due to its differential transmission form, RS485 is very robust against electrical noise. Due to its wide common-mode voltage range, it is tolerant to ground potential shifts between nodes. These two characteristics are the main reason for using RS485 in applications where low noise emissions and susceptibility is required.

In most applications, the signaling rate and long distance lines is sufficient to control a process line or share data in industrial environments. An RS485 network schematic is shown in Figure 3.

![Figure 3: RS485 Network Schematic](image)

The RS485 standard does not define particular protocols for communications with the bus, it only specifies electrical characteristics of the interconnection. Because of this, RS485 is used with many communication protocols as the physical layer of the communication system.

Because of the differential nature of the RS485 bus, transceivers are used to convert single-ended buses to differential ones. This is done because typical communications systems or microcontroller serial communications peripherals are single-ended. To implement this, the logic shown in Figure 4 is used.

![Figure 4: RS485 Transceiver Logic Schematic](image)
RS422/RS485 Transceiver

Since RS485 communications are half-duplex, a flow control input called /RE DE is used. When flow control is low, the Rx stage is active so the A and B lines are input lines. Data at the differential bus is decoded by the Rx stage and the result is at the R output pin.

When flow control is high, the Tx stage is active so the A and B lines are output lines. Data at the single-ended input D is converted to differential data by the Tx stage to transmit it via the differential bus connected to pins A and B.

One of the most used protocols that use RS485 as the electrical layer is the RS232 serial communication protocol. An RS422/RS485 is used because of the single-ended nature and full duplex scheme of the RS232 serial data transmission. Typically, low bitrates are used, such as 19200 bps or 38400 bps, due to the industrial environment where RS485 buses are installed.

6 Implementation

The implementation of the RS422/RS485 transceiver is made with a SLG46533V GreenPAK. This CMIC has 4 Analog Comparators and GPIO’s which can be used as input/output simultaneously by configuring it with a control signal. The outputs of this Stage are two square waveforms, one for each group.

The flow control input is implemented with Pin 3, which is configured as a digital input and is called /RE DE.

To implement the receiver mode of the transceiver, SLG46533V must convert a differential input to a single-ended output. To do this, we used an analog comparator. Figure 5 shows ACMP3 configuration.

![Figure 5: Analog Comparator Configuration](image)

The analog comparator is configured with 25 mV hysteresis and without Low Bandwidth in order to obtain higher speed communications.
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The selection of the ACMP is made based on the idea of using the same pins for differential input and differential output, as it is required by a RS485 transceiver. This is the main reason for choosing ACMP3, because it can have input pins which have I/O control signals for configuring them as an input or an output for receiving or transmitting data.

The inputs of the Analog comparator are the differential inputs of the transceiver, called A and B. To do this, positive input of the ACMP is connected to Pin 13 (ACMP2 In+ Source) and the negative input is connected to Pin 14 (the external V<sub>ref</sub> of the ACMP3).

When the transceiver flow control bit is low, the transceiver works as a receiver of data. In this case, Pin 13 and Pin 14 are configured as analog inputs and the Analog comparator process both inputs to define a high level or a low level at its output. The output of the ACMP is connected to Pin 5, called R, and it represents the received data.

Figure 6 and Figure 7 show the configurations of Pin 13 and Pin 14 respectively.

When the transceiver flow control bit is high, the transceiver works as a transmitter of data. In this case, Pin 13 and Pin 14 are configured as digital outputs. The single-ended serial data input to the transceiver is implemented with Pin 4, called D.

In order to obtain differential data at the outputs, LUT0 is used a NOT gate to obtain the inverse of the data input. These two signals (Data and its inverse) are connected to outputs A and B so the differential data is transmitted to the bus.
Figure 7: Pin 14 Configuration

LUT0 configuration is shown in Figure 8.
Logic states of inputs and outputs and functionalities of the RS422/RS485 transceiver are shown in Table 1.

### Table 1: Logic Table and Functionalities

<table>
<thead>
<tr>
<th>/RE DE</th>
<th>D</th>
<th>R</th>
<th>A and B</th>
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<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>Received Data</td>
<td>Data Inputs from Bus</td>
</tr>
<tr>
<td>1</td>
<td>Transmitted Data</td>
<td>X</td>
<td>Data Outputs to Bus</td>
</tr>
</tbody>
</table>

The entire implementation is shown in Figure 9.
7  Tests and Conclusion

To test the implementation, the transceiver was used as a receiver and a transmitter in separate cases so the inputs and the outputs can be registered with a logic analyzer.

As a receiver, the RS485 transceiver received a binary stream via the differential bus and the logic analyzer registered the differential inputs and the single-ended data output. The binary stream sent to the transceiver was

1101001010

Figure 10 shows the transmitted stream data by the outputs A and B and the data input pin D. Also, the flow control signal /RE DE set to a high logic level in order to configure the RS485 transceiver as a data transmitter.

As a transmitter, the RS485 transceiver transmitted a binary stream (corresponding to the single-ended binary stream at the D input) via the differential bus and the logic analyzer registered the differential inputs and the single-ended data input. The binary stream sent by the transceiver was

1001101010
8 Conclusion

In this application note, a RS422/RS485 transceiver is implemented using SLG46533V. RS422/RS485 transceivers are used in many applications where this industrial bus is used, because of its differential nature which is not compatible with the single-ended nature of binary communication systems.

There are several commercial ICs that implement this type of transceiver. In this application note, a compatible transceiver is created with the RS485 specifications with respect to input differential voltage sensitivity, differential output voltage, typical data transfer rates and typical common mode voltages. Our system complies with the RS485 specifications, with an added benefit of a much smaller IC size.
Revision History

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<th>Date</th>
<th>Description</th>
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<td>26-Feb-2018</td>
<td>Initial version.</td>
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Status Definitions

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<td>DRAFT</td>
<td>The content of this document is under review and subject to formal approval, which may result in modifications or additions.</td>
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<tr>
<td>APPROVED or unmarked</td>
<td>The content of this document has been approved for publication.</td>
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