
ClockMatrix

Trigger Registers

Abstract

This document provides a process to quickly identify the trigger registers for a specific ClockMatrix register. Although this information is contained in the *8A3xxx Family Programming Guide*, the registers have been extracted and summarized into lookup tables that are more user-friendly.

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1. Overview

Many ClockMatrix register modules include a trigger register that must be written to cause register changes within that module to take effect; the trigger register must be written even if the contents of the trigger register are not changed. Where present, the trigger register is always the last register in the module so that the last write of a burst will trigger any changes in the module. After a trigger register is written the user should wait 200 microseconds before reading or writing any register in the device.

Example: If the CLK0 input frequency needs to be updated, it would require a write to the corresponding numerator register, IN0_FREQ_M, which starts at offset 0xC1.B0, and is 6 bytes long. For this example, let's assume that the frequency change only requires 0xC1.B0 to be modified. If the user were only to update register 0xC1.B0, the LSB, the CLK0 frequency would not update. For an explanation of how to identify the trigger register, see the next example.

2. Trigger Register Lookup Tables

Renesas provides a zip file named "ClockMatrix FW x.y.x Trigger Registers.zip", which contains a trigger register file for each ClockMatrix variant, where "x.y.x" represents the FW version. Figure 1 shows an excerpt of the trigger registers file, which is a lookup table, for the 8A34001 device.

There are two columns separated by a colon. The first column is the register and the second column is its associated trigger register. If a register is not listed in the file then it does not require a trigger register. The first row shows that register 0xC1.60 is its own trigger register and does not need an additional trigger register. In contrast, the excerpt shows that changes to register 0xC1.88 to 0xC1.92 (red outline below) require a write to register 0xC1.92 (orange outline below).

Register	Trigger Register
C1.60	C1.60
C1.61	C1.61
C1.64	C1.64
C1.65	C1.65
C1.66	C1.66
C1.67	C1.67
C1.68	C1.68
C1.69	C1.69
C1.6C	C1.6C
C1.6D	C1.6D
C1.88	C1.92
C1.89	C1.92
C1.8A	C1.92
C1.8B	C1.92
C1.8C	C1.92
C1.8D	C1.92
C1.8E	C1.92
C1.8F	C1.92
C1.90	C1.92
C1.91	C1.92
C1.92	C1.92

Figure 1. Trigger Registers List

Example: Continuing the previous example. Figure 2 shows that a change to 0xC1.B0 requires that its associated trigger register, 0xC1.BD, also be written. Either a block register write from 0xC1.B0 to 0xC1.BD can be used, or alternatively, only 0xC1.B0 and 0xC1.BD can be written.

C1.A3:	C1.AD
C1.A4:	C1.AD
C1.A5:	C1.AD
C1.A6:	C1.AD
C1.A7:	C1.AD
C1.A8:	C1.AD
C1.A9:	C1.AD
C1.AA:	C1.AD
C1.AB:	C1.AD
C1.AC:	C1.AD
C1.AD:	C1.AD
C1.B0:	C1.BD
C1.B1:	C1.BD
C1.B2:	C1.BD
C1.B3:	C1.BD
C1.B4:	C1.BD
C1.B5:	C1.BD
C1.B6:	C1.BD
C1.B7:	C1.BD
C1.B8:	C1.BD
C1.B9:	C1.BD
C1.BA:	C1.BD
C1.BB:	C1.BD
C1.BC:	C1.BD
C1.BD:	C1.BD
C1.C0:	C1.CD
C1.C1:	C1.CD
C1.C2:	C1.CD

Figure 2. IN0_FREQ_M and Associated Registers List

When writing several registers to the chip, it is recommended to iterate through the register list and for each register, if there is an associated trigger register, append the trigger register to the list. If multiple registers require the same trigger, then the trigger can be added after the last register for that module. The trigger register must be added regardless of its value, otherwise the module will not be updated.

3. Conclusion

This document explained how to use the files within the “ClockMatrix FW x.y.x Trigger Registers.zip” folder as lookup tables to identify the corresponding trigger registers for a specific ClockMatrix register. For more information, see the *8A3xxxx Family Programming Guide* or contact Renesas Applications support at IDT-Support-sync@lm.renesas.com.

4. Revision History

Revision	Date	Description
1.0	Dec.10.20	Initial release.

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