ClockMatrix Power Supply Filtering Recommendations

The ClockMatrix™ devices have several groups on the power supply, including the digital (core/control/GPIO/Serial Port), analog, input and output powers. Generally, they need to be separated by a ferrite bead to avoid crosstalk from each other. This application note provides guidance on which power groups can be combined in order to simplify the power filtering.

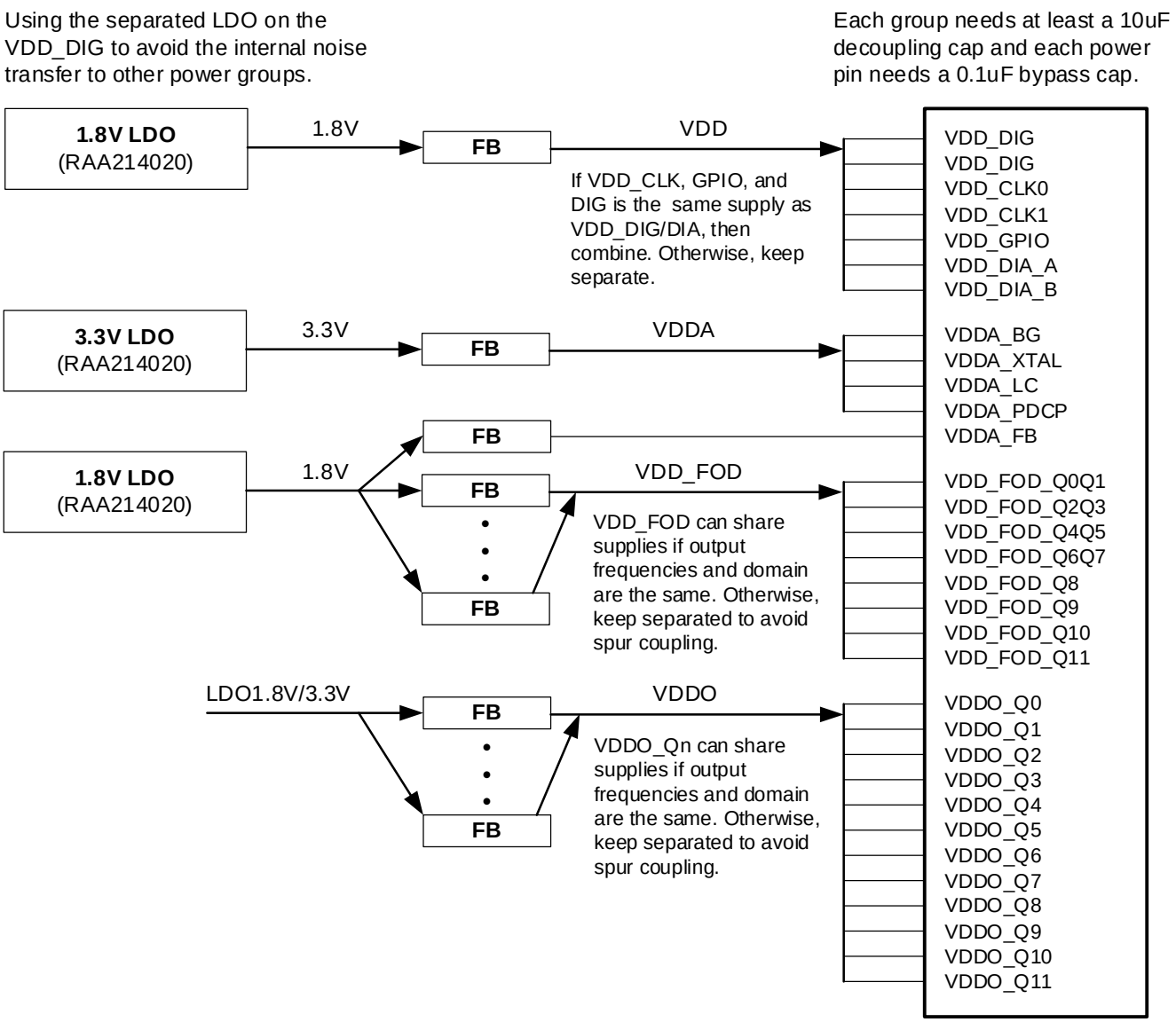
Contents

1. Power Filtering Reduction

Below is the recommendation for the power filter reduction on the 8A340xx devices (doesn't include 8A34005). Crosstalk among outputs needs to be avoided and the digital noise needs to be isolated to prevent it from coupling noise to other power domains, especially VDDA.

Power Filtering Reduction	▪ VDD_DIG, VDD_GPIO (combine if same supply). ▪ VDD_CLK (if same supply as VDD_DIG/GPIO then combine. Otherwise, keep separate). ▪ VDDA_XTAL, VDDA_PDCP (can combine). ▪ VDDA_FB (keep separate). ▪ VDDA_BG, VDDA_LC (next compromise is combining these two if board space allows. Keep separated). ▪ VDD_DIA_A/B (keep separated; possible course of coupling). ▪ VDD_DCO_Qn (keep separated; chance of increased spurs if at different frequencies). ▪ VDDO_Qn (can share supplies if output frequencies are the same. Otherwise, keep separated to avoid spur coupling).
VDD_DCO_Qx	Unused channels do not require VDD_DCO to be powered. However, if the channel is used for TDC operations, be sure to power it.
VDDO	Unused banks do not require VDDO connections. Be sure to configure unused outputs as HiZ in the tcs file.

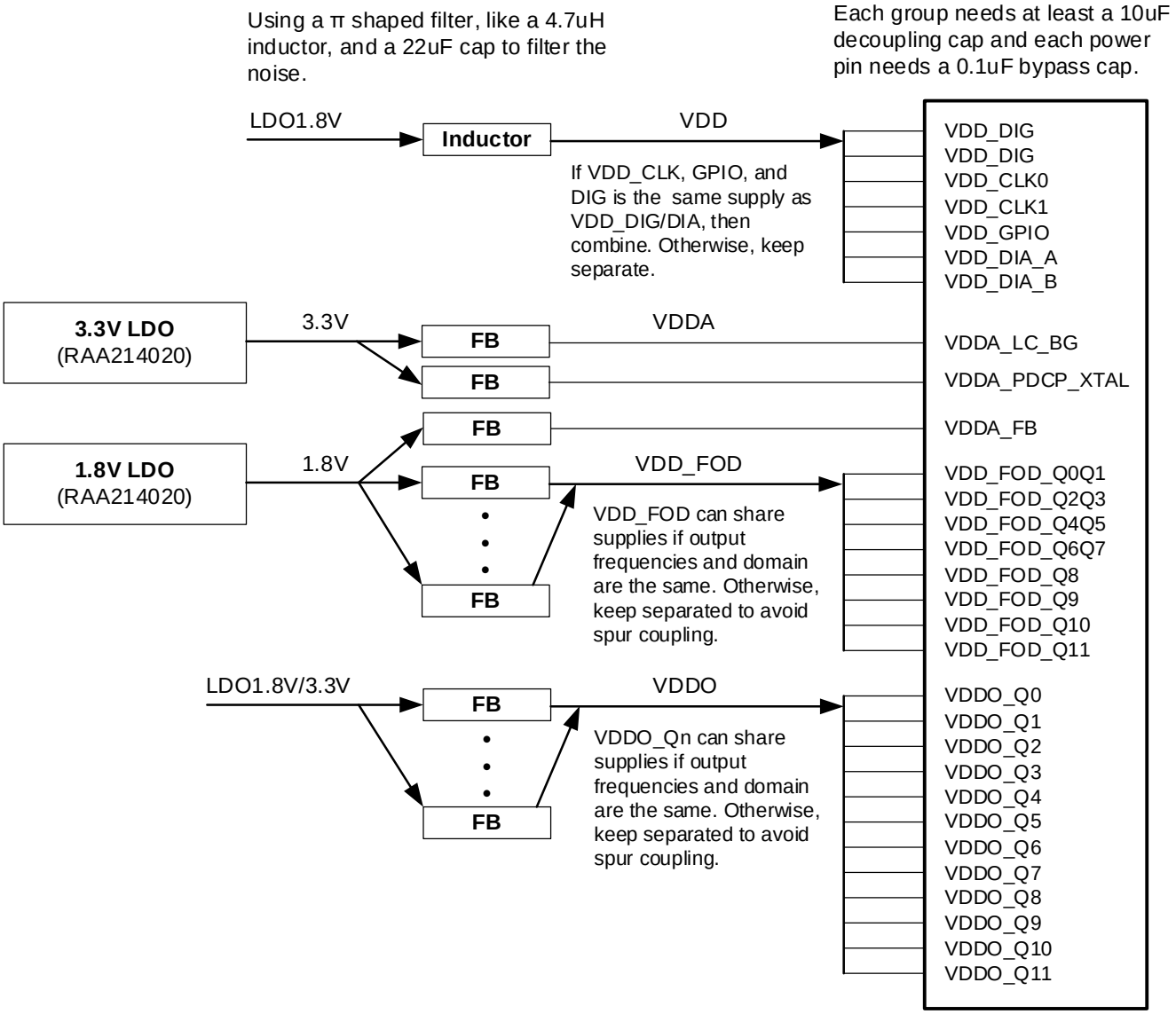
1.1 Simplified Power Supply–Case 1



1.2 Simplified Power Supply–Case 2

Below is the recommendation for the power filter reduction on the 8A34005, RC32012A and RC38612 devices.

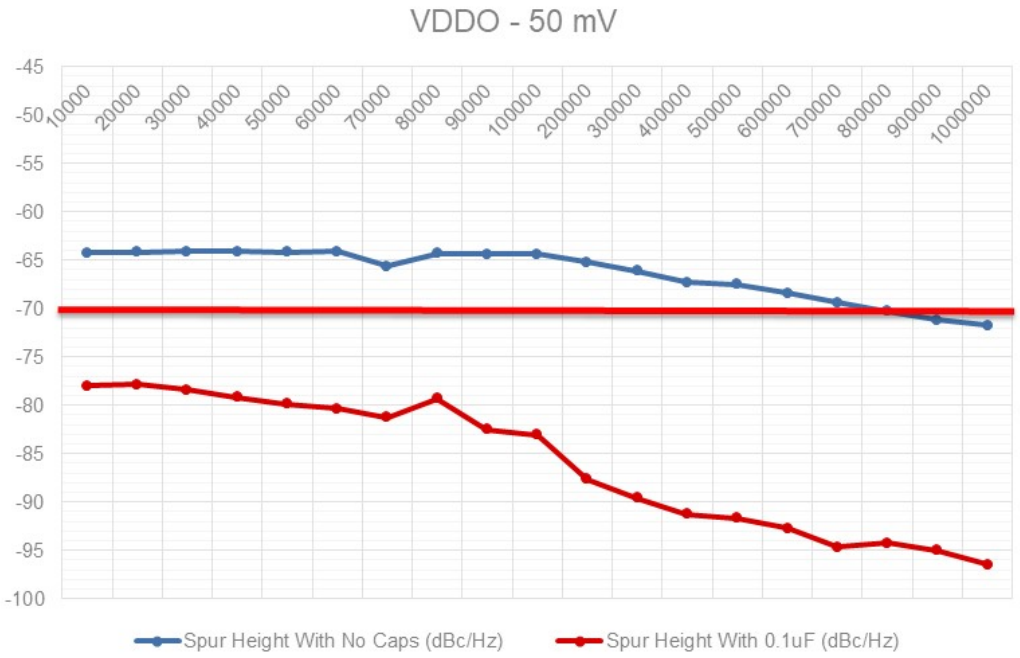
Power Filtering Reduction	▪ VDD_DIG (keep separate). ▪ VDD_CLK (if same supply as VDD_DIG/GPIO then combine. Otherwise, keep separate). ▪ VDDA_PDCP_XTAL (keep separate). ▪ VDDA_FB (keep separate). ▪ VDDA_BG_LC (keep separate). ▪ VDD_DIA_A/B, VDD_GPIO (keep separated; possible course of coupling). ▪ VDDO_Qn (can share supplies if output frequencies are the same. Otherwise, keep separated to avoid spur coupling).
VDDO	Unused banks don't require VDDO connections. Be sure to configure unused outputs as HiZ in the tcs file.



2. PSRR Tests on VDDO, VDDD, VDDA, VDD_FOD, VDDA_XTAL_PDCP and VDD_LC_BG

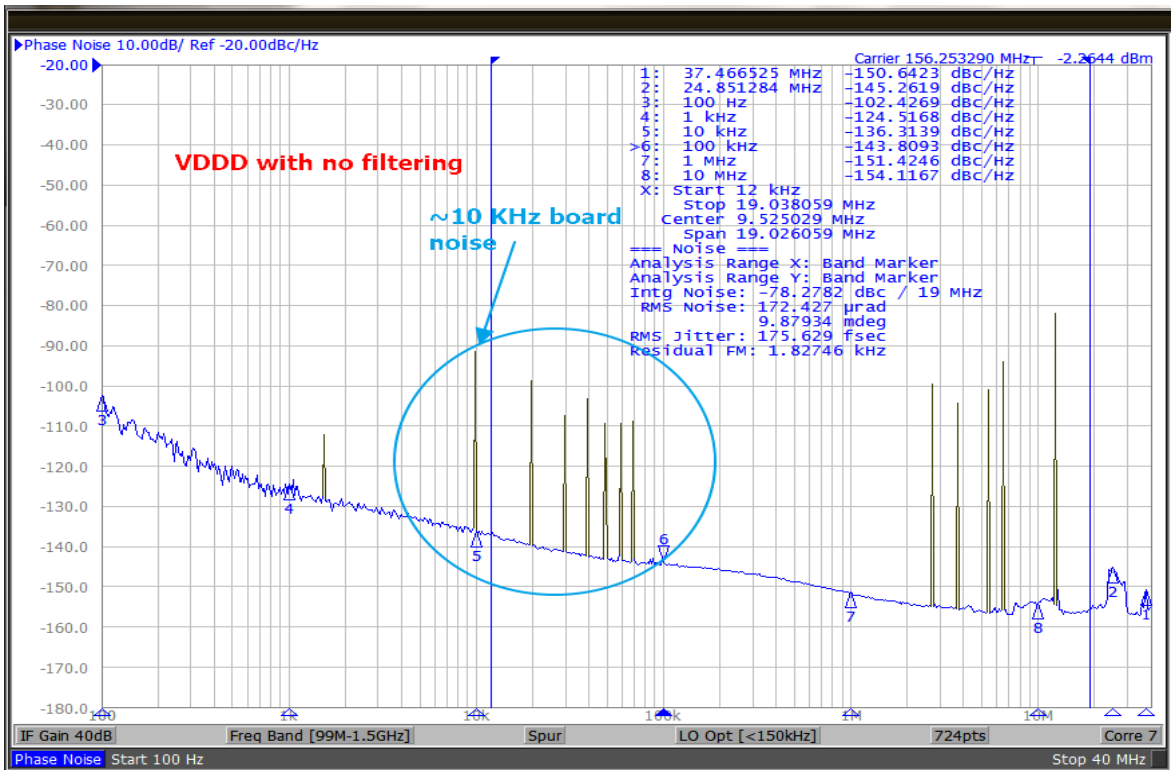
2.1 PSRR of VDDO

With a 0.1µF bypass capacitor on the VDDO pin, the PSRR can achieve better than -75dBc.



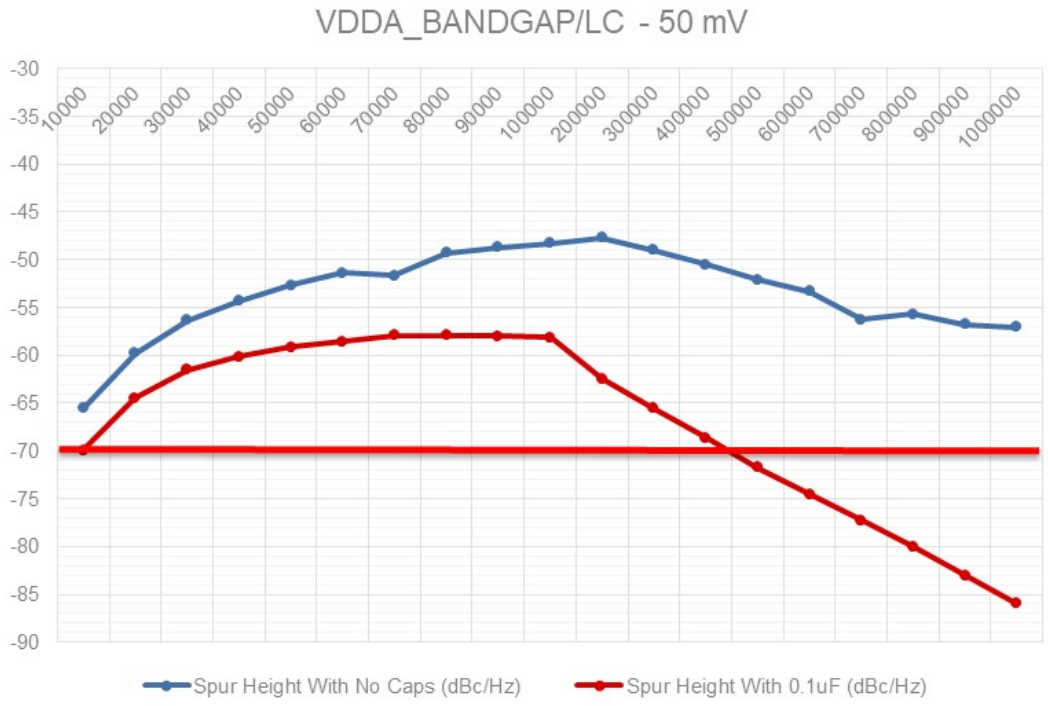
2.2 PSRR of VDDD

With no filtering on the VDDD pin, the PSRR can achieve better than -90dBc.



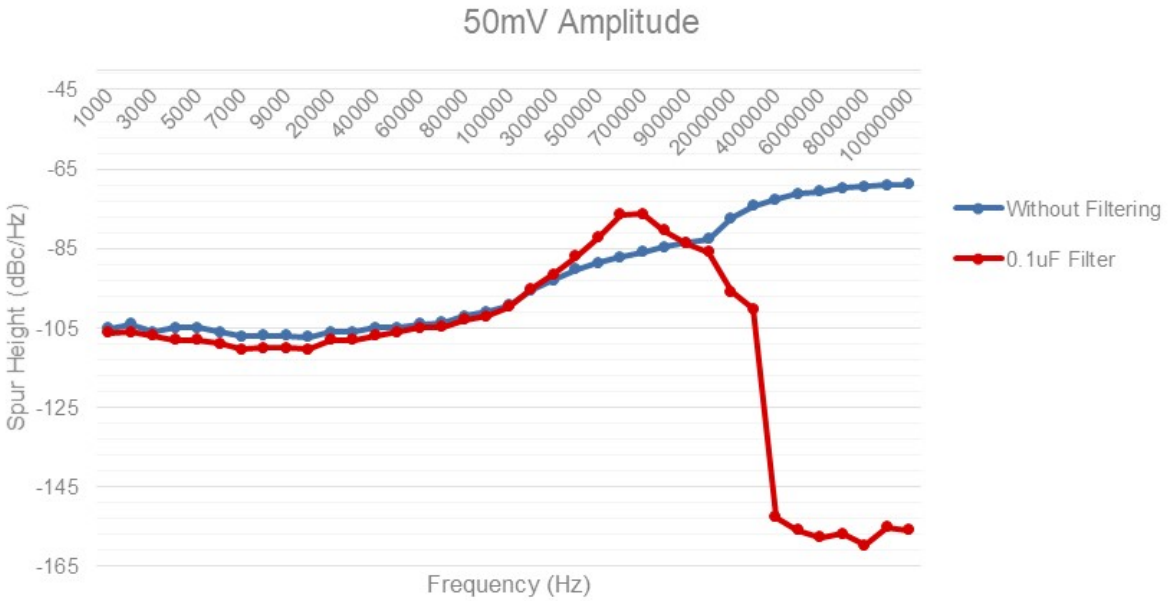
2.3 PSRR of VDDA_BANDGAP/LC

With a 0.1µF bypass capacitor on the VDDA_BANDGAP/LC pin, the PSRR can achieve better than -55dBc. With a switching frequency near that of the DC/DC supply (500kHz or more), the PSRR is better than -70dBc.



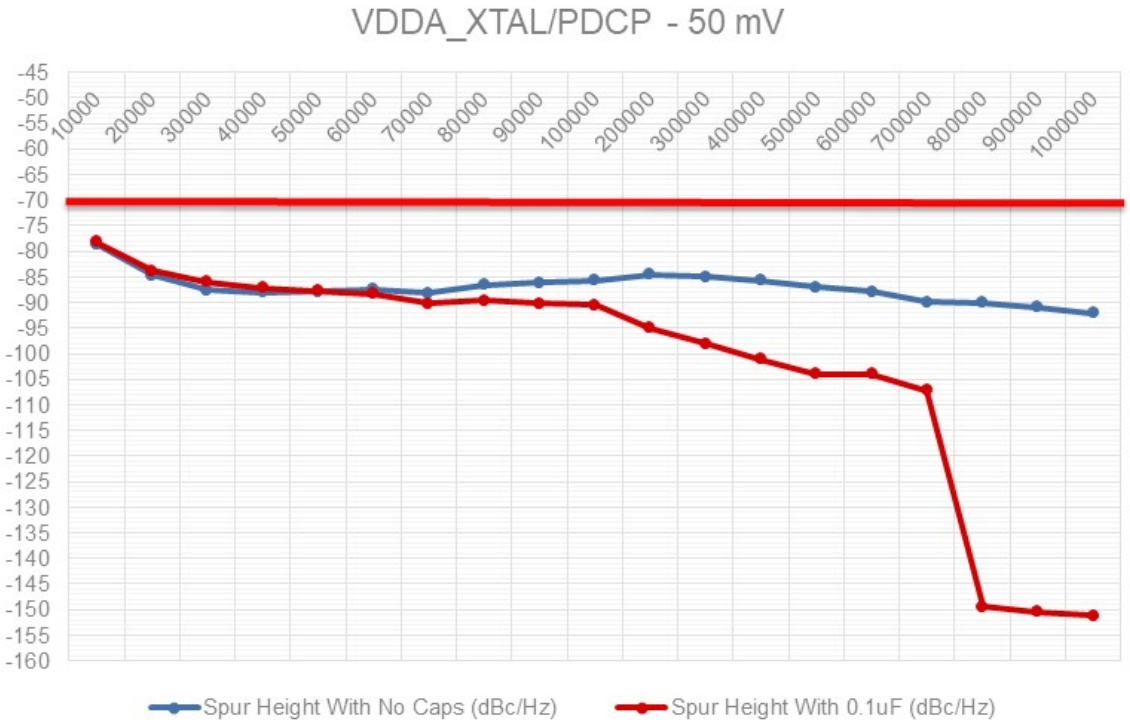
2.4 PSRR of VDD_FODx

With a 0.1µF bypass capacitor on the VDD_FODx pin, the PSRR can achieve better than -70dBc.



2.5 PSRR of VDDA_XTAL/PDCP

With or without a 0.1µF bypass capacitor on the VDDA_XTAL/PDCP pin, the PSRR can achieve better than -75dBc.



3. Revision History

Revision	Date	Description
1.00	Jul 13, 2023	Initial release.