ClockMatrix™
Methods for Changing DPLL Settings during a Reference Switch

Abstract
This document explains how to configure a ClockMatrix to have different DPLL settings for different references.

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Related Information
For more information, visit our website: ClockMatrix™ Timing Solutions.
1. Introduction

A user of a ClockMatrix DPLL may need to change the configuration of a DPLL as it switches references because of input frequency or a required standard compliance. For two different configurations, the DPLL can change its settings during a reference switch automatically using predefined configurations or using manual register writes. For more than two DPLL configurations, the user must use the manual register write method.

2. Using Predefined Configurations

For this method, the DPLL settings are included in the loaded .tcs file. There are two predefined configurations for each DPLL. They include Loop Bandwidth, Damping Factor, and Phase Slope Limiting. (There is also a Decimation Factor, which the GUI sets to “4x”.) The GUI sets each reference for group Predefined Config 0 or Predefined Config 1. The use of predefined configurations is set on a per DPLL basis, which are different references.

2.1 Using Predefined Configurations in the GUI

For cases with only two configurations, use the predefined configuration feature in ClockMatrix. When configuring the device through the configuration (.tcs) file, the user does not need to do any additional register writes after the system is running.

2.2 Example Predefined Configuration for 25MHz and 1 PPS (1Hz)

For this application, the device requires a high bandwidth for 25MHz on CLK0 and requires a low bandwidth for 1Hz input on CLK1. The example uses channel/DPLL 0. In Figure 1, the 25MHz input is set to predefined configuration 0 (pred0), and in Figure 2, the 1 PPS input is set to predefined configuration 1 (pred1). Channel 0 uses automatic switching between 0 and 1, and this also works with a manual reference selection. For DPLL parameters not listed under predefined configuration, both references use the same parameters.

![Figure 1. CLK0 Configuration](image-url)
Figure 2. CLK1 Configuration

Figure 3. Channel 0
3. Using Register Writes

Procedure:

1. Check that the DPLL is locked before starting the procedure using STATUS.DPLLn_STATUS.DPLL0_STATE[3:0].
3. Change the settings on the DPLL:
   - Loop bandwidth, damping factor, phase slope limiting (PSL), decimation factor
   - Lock criteria
   - Fast lock settings
4. Change the reference for the DPLL.
5. Put the DPLL in automatic/manual mode to lock to new reference.
6. Change the DPLL mode to allow relocking process to begin by setting DPLLn_State_mode → automatic.

The automatic reference mode and the automatic DPLL state mode work differently. For a reference, the automatic mode selects a reference using the reference priority list. (Alternatively, a manual mode can be used to either select a reference or to use holdover if that reference is unavailable.) For a DPLL, automatic mode allows the DPLL to switch between its states automatically instead of being locked to a mode (such as forced holdover). Note: The DPLL state machine operates when the DPLL is in PLL_MODE = “PLL_MODE” rather than synthesizer or DCO modes.
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<table>
<thead>
<tr>
<th>Category</th>
<th>Register</th>
<th>Trigger Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set DPLL State</td>
<td>DPLL_n.DPLL_MODE.STATE_MODE[2:0]</td>
<td>DPLL_n.DPLL_MODE</td>
</tr>
<tr>
<td>Get DPLL State</td>
<td>STATUS.DPLLn_STATUS.DPLL0_STATE[3:0]</td>
<td>N/A</td>
</tr>
<tr>
<td>Loop Bandwidth - value</td>
<td>DPLLCTRL_n.DPLL_BW.DPLL_BW[13:0]</td>
<td>Self-triggering</td>
</tr>
<tr>
<td>Loop Bandwidth - unit</td>
<td>DPLLCTRL_n.DPLL_BW.BW_UNIT[15:14]</td>
<td>Self-triggering</td>
</tr>
<tr>
<td>Damping factor</td>
<td>DPLLCTRL_n.DPLL_DAMPING.DAMP_FTR[3:0]</td>
<td>Self-triggering</td>
</tr>
<tr>
<td>PSL</td>
<td>DPLLCTRL_0.DPLL_PSL.DPLL_PSL[15:0]</td>
<td>Self-triggering</td>
</tr>
<tr>
<td>Decimation Factor</td>
<td>DPLLCTRL_n.DPLL_BW.MULT.MULT[7:0]</td>
<td>Self-triggering</td>
</tr>
<tr>
<td>Lock Criteria - Value</td>
<td>DPLL_n.DPLL_LOCK_1.PHASE_LOCK_MAX_ERROR[5:0]</td>
<td>DPLL_n.DPLL_MODE</td>
</tr>
<tr>
<td>Lock Criteria - Unit</td>
<td>DPLL_n.DPLL_LOCK_1.PHASE_UNIT[7:6]</td>
<td>DPLL_n.DPLL_MODE</td>
</tr>
<tr>
<td>Fast lock – fast acquisition</td>
<td>DPLL_n.DPLL_FASTLOCK_CFG_0.LOCK_REC_FAST_ACQ_EN[6]</td>
<td>DPLL_n.DPLL_MODE</td>
</tr>
<tr>
<td>Fast lock – frequency snap</td>
<td>DPLL_n.DPLL_FASTLOCK_CFG_0.LOCK_REC_FREQ_SNAP_EN[4]</td>
<td>DPLL_n.DPLL_MODE</td>
</tr>
<tr>
<td>Fast lock – phase snap</td>
<td>DPLL_n.DPLL_FASTLOCK_CFG_0.LOCK_REC_PHASE_SNAP_EN[5]</td>
<td>DPLL_n.DPLL_MODE</td>
</tr>
</tbody>
</table>

1. In the ClockMatrix, the settings for a group of related registers (such as DPLL configuration) will not be applied until a trigger register is written. Other registers are self-triggering so their impact on the device is immediate. Trigger mode does not apply to status registers.

3.1 Example Manual Configurations

This example uses an application with three requested configurations for DPLL0: a very low bandwidth for GNSS (1Hz) up-convert, a SyncE compliant DPLL, and a high bandwidth for locking to a PTP clock.

<table>
<thead>
<tr>
<th>Profile</th>
<th>Input Frequency</th>
<th>Bandwidth (Hz)</th>
<th>PSL (μs/s)</th>
<th>Max Freq. Offset (ppm)</th>
<th>Lock Criteria (ns/s)</th>
<th>Fast Lock Enabled?</th>
</tr>
</thead>
<tbody>
<tr>
<td>G.8262 option 2</td>
<td>25MHz</td>
<td>0.1</td>
<td>0.885</td>
<td>52</td>
<td>600</td>
<td>Yes – fast acquisition</td>
</tr>
<tr>
<td>GNSS Up-convert Lock to 1Hz</td>
<td>1 PPS (1Hz)</td>
<td>0.02</td>
<td>0.01</td>
<td>1</td>
<td>100</td>
<td>Yes – frequency snap/phase snap</td>
</tr>
<tr>
<td>PTP Clock</td>
<td>25MHz</td>
<td>25</td>
<td>Unlimited</td>
<td>244</td>
<td>10</td>
<td>No - Not required</td>
</tr>
</tbody>
</table>

All profiles use DPLL mode with hitless reference switching.

A user can dynamically change the DPLL BW settings while locked to a reference, however, Renesas does not recommend this method. This change can cause a change of state especially when changing the lock criteria. During the DPLL reconfiguration, the output should not glitch. Note: The DPLL does not check the criteria for fast lock until the next state transition (e.g., from locked to holdover to LOCKREQ (lock recovery) state). Renesas recommends setting the DPLL to holdover when making changes the DPLL configuration.
### 3.2 DPLL Performance for the Example Configuration

The following plots show a TIE (time interval error) capture for a DPLL switching between the profiles in the previous section.

<table>
<thead>
<tr>
<th>Figure</th>
<th>From Profile</th>
<th>To Profile</th>
<th>Time of Switch</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 5</td>
<td>JA</td>
<td>8262</td>
<td>30 seconds</td>
<td>Lock immediate</td>
</tr>
<tr>
<td>Figure 6</td>
<td>JA</td>
<td>GNSS</td>
<td>30 seconds</td>
<td>Lock after 15 seconds</td>
</tr>
<tr>
<td>Figure 7</td>
<td>8262</td>
<td>JA</td>
<td>6 minutes</td>
<td>Lock immediate</td>
</tr>
<tr>
<td>Figure 8</td>
<td>GNSS</td>
<td>JA</td>
<td>12 minutes</td>
<td>Lock immediate</td>
</tr>
<tr>
<td>Figure 9</td>
<td>8262</td>
<td>GNSS</td>
<td>30 seconds</td>
<td>Lock after 15 seconds</td>
</tr>
<tr>
<td>Figure 10</td>
<td>GNSS</td>
<td>8262</td>
<td>15 minutes</td>
<td>Lock immediate</td>
</tr>
</tbody>
</table>

![Example TIE from JA to 8262 with Switch at 30 Seconds](image-url)
Figure 6. Example TIE from JA to GNSS with Switch at 30 Seconds

Figure 7. Example TIE from 8262 to JA with Switch at 360 Seconds (6 Minutes)
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Figure 8. Example TIE from GNSS to JA

Figure 9. Example TIE from 8262 to GNSS with Switch at 30 Seconds
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4. Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Nov.4.20</td>
<td>initial release.</td>
</tr>
</tbody>
</table>
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Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Email: contact@renesas.com

Contact Information
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