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H8/300L SLP Series

Clock Synchronization Serial Data Slave Transmission

Introduction

This application note describes clock synchronization serial data slave transmission using the Serial Communication Interface 3 (SCI3) module of the H8/38024.

Target Device

H8/38024

Contents

1. Specifications

- Clock synchronization serial data slave transmission is performed using SCI3 of the H8/38024, as shown in figure 1.
- Four bytes of serial data are transmitted in this sample task.
- The communication format is the LSB first format with the data length fixed to 8 bits, and the bit rate is 250 kbps.

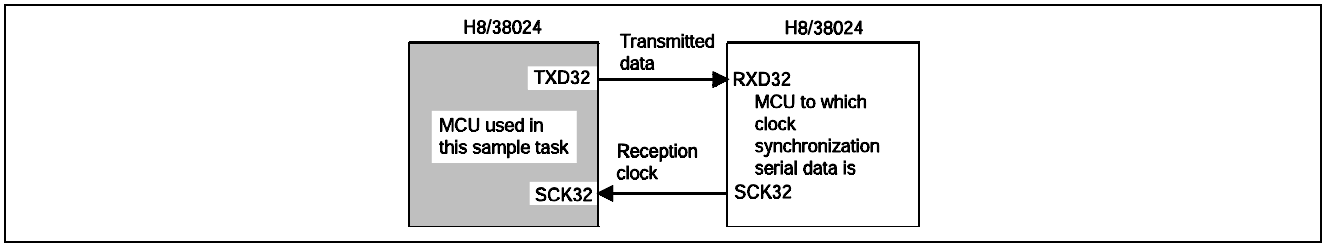


Figure 1 Clock Synchronization Serial Data Slave Transmission with the H8/38024

2. Description of Functions

- In this sample task, clock synchronization serial data slave transmission is performed using Serial Communication Interface 3 (SCI3). A block diagram of SCI3 is shown in figure 2 and the functions are described below the figure.

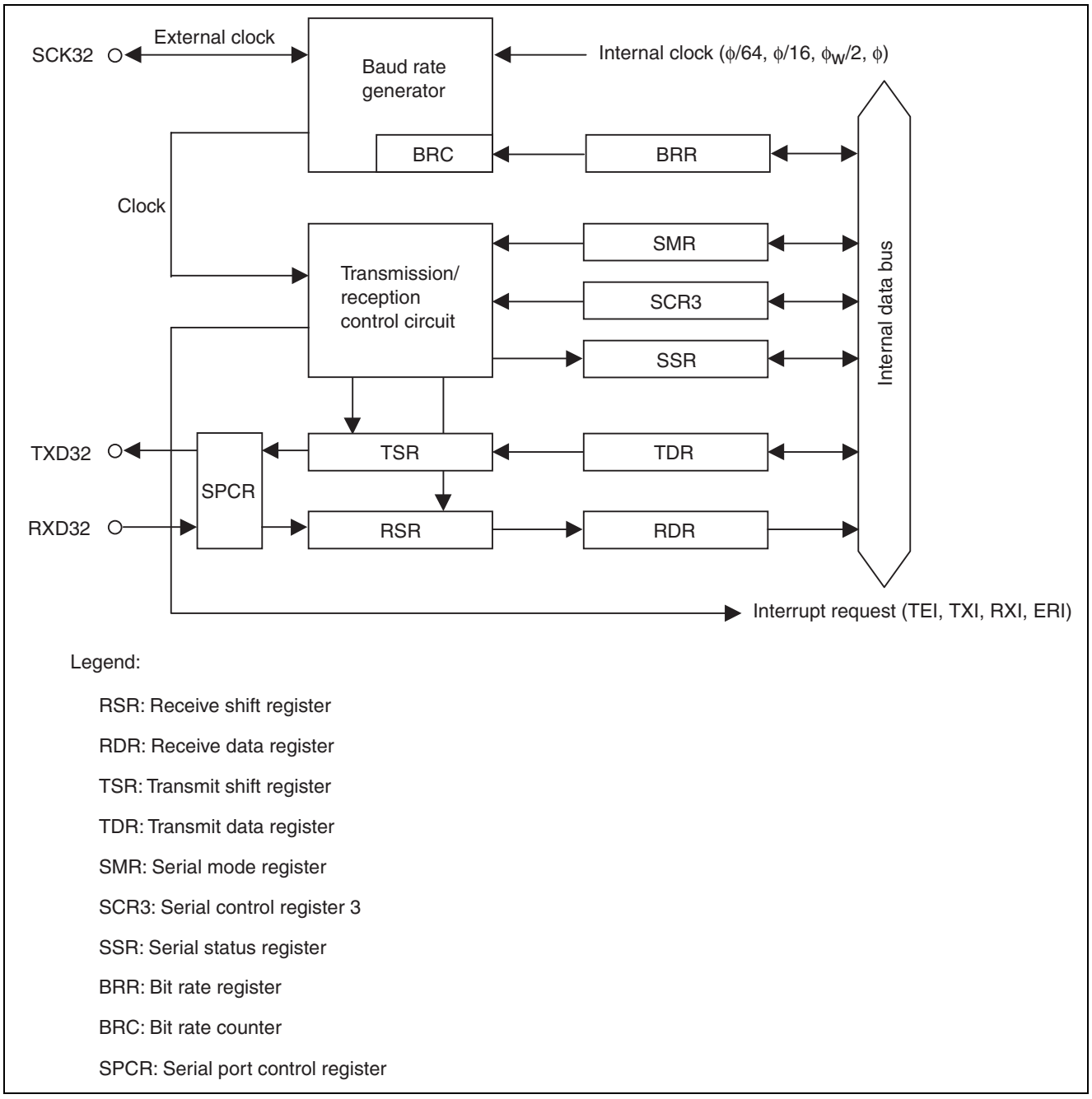


Figure 2 Block Diagram of SCI3

- Clock synchronization mode
  Data is transmitted or received in synchronization with clock pulses. It is possible to perform serial data communication with another LSI that has the clock synchronization communication function. The length of communication data is fixed to 8 bits.
- Internal clock ϕ
  This reference clock is used for operation of built-in peripheral functions and is generated by the clock pulse generator (CPG).
- Transmit shift register (TSR)
  This register is used to transmit serial data. After one frame of data has been transmitted, the data is transferred from the transmit data register (TDR) to TSR and then the data is output from the TXD32 pin. TSR cannot be directly accessed by the CPU.
- Transmit data register (TDR)
  This 8-bit register stores transmission data. When space is detected in TSR, the data written in TDR is automatically transmitted to TSR and serial data transfer is started. Since TDR and TSR have a double buffer structure, after one frame of data is transmitted, the next data can be continuously written to TDR because the previous data in it is automatically transferred to TSR. The CPU can always read from or write to TDR, but make sure that the TDRE bit of the serial status register (SSR) is 1 before writing to TDR.
- Serial mode register (SMR)
  This 8-bit register is used to set the serial data communication format and select the clock source for the built-in baud rate generator.
- Serial control register 3 (SCR3)
  This register is used to control transmission/reception and interrupts, and select a clock source for transmission/reception.
- Serial status register (SSR)
  This register consists of the SCI3 status flags and transmit/receive multiprocessor bits. TDRE, RDRF, OER, FER, and PER can only be cleared.
- Bit rate register (BRR)
  This 8-bit register is used to adjust the bit rate. Since SCI3 has an independent baud rate generator for each channel, a separate bit rate can be set. For details related to settings and the execution rate, see the hardware manual.

- Table 1 describes the pins and registers used in this sample task.

Table 1 Assignment of Functions

	Name	Description
Pins	SCK32	SCI3 clock input/output pin
	TXD32	SCI3 transmit data output pin
	RXD32	SCI3 receive data input pin
Registers	SMR	Sets the communication format to the clock synchronization mode.
	SCR3	Enables transmit operation
	SSR	Status flag indicating the SCI3 operating state
	BRR	Sets the communication bit rate.
	TSR	This register is used to transmit serial data.
	TDR	This register stores transmission data.
	RSR	This register is used to receive serial data.
	RDR	This register stores received data.
	SPCR	This register sets to the TXD32 output pin to prevent the TXD32 output data from being inverted.

3. Principles of Operation

- Figure 3 illustrates operation during clock synchronization mode transmission in this sample task. It also describes software and hardware processings.

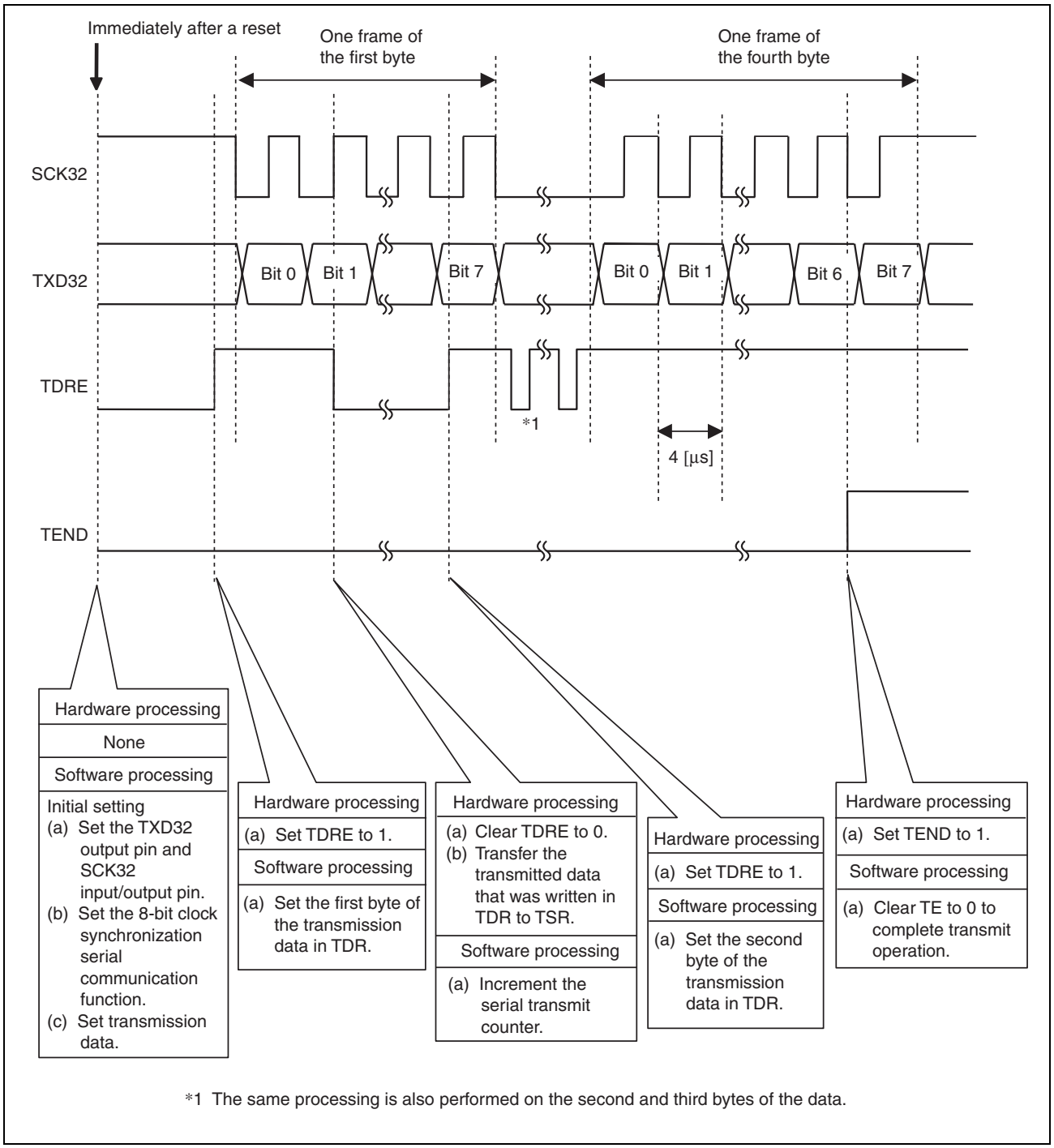


Figure 3 Operation during Transmission of Data

4. Description of Software

4.1 Description of Modules

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Function	Description
main	Clock synchronization serial data slave transmit operation
init_SCI3	Initializes SCI3.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

The internal registers used in the sample task are described below. The following settings are the values used in this sample task, not the default values.

- SPCR Serial port control register Address: H′FF91

Bit No.	Bit Name	Setting	R/W	Description
5	SPC32	1	R/W	Switching of the P42/TXD32 pin function Functions as the TXD32 output pin.
3	SCINV3	0	R/W	Switching of TXD32 pin output data inversion Does not invert TXD32 output data.

- SMR Serial mode register Address: H′FFA8

Bit No.	Bit Name	Setting	R/W	Description
7	COM	1	R/W	Communication mode Operates SCI3 in the clock synchronization mode.
2	MP	0	R/W	Multiprocessor mode Disables the multiprocessor communication function.

- BRR Bit rate register Address: H′FFA9

  Function: 8-bit register used to set the transmit and receive bit rates according to the operating clock of the baud rate generator selected by CKS1 and CKS0.

  Setting: H′04

  R/W: R/W

- SCR3 Serial control register 3 Address: H′FFAA

Bit No.	Bit Name	Setting	R/W	Description
5	TE	1	R/W	Transmit enable Enables transmit operation. (The TXD32 pin is used as the transmit data pin.)
1	CKE1	0	R/W	Clock enable 1, 0
0	CKE0	0	R/W	Selects the external clock as the clock source and selects the synchronization clock input as the SCK32 pin function.

- TDR Transmit data register Address: H′FFAB
  Function: 8-bit register that stores transmit data
  Setting: -
  R/W: R/W

- SSR Serial status register Address: H′FFAC

Bit No.	Bit Name	Setting	R/W	Description
7	TDRE	-	R/(W)*	Transmit data register empty TDRE = 0: The transmission data written in TDR is not transferred to TSR. TDRE = 1: The transmission data is not written in TDR or the transmission data written in TDR was transferred to TSR.
2	TEND	-	R/(W)*	Transmit end TEND = 0: Transmission in progress TEND = 1: Transmission completed

"-" indicates "Don't care".
* Only 0, which clears the flag, can be written.

4.4 RAM Usage

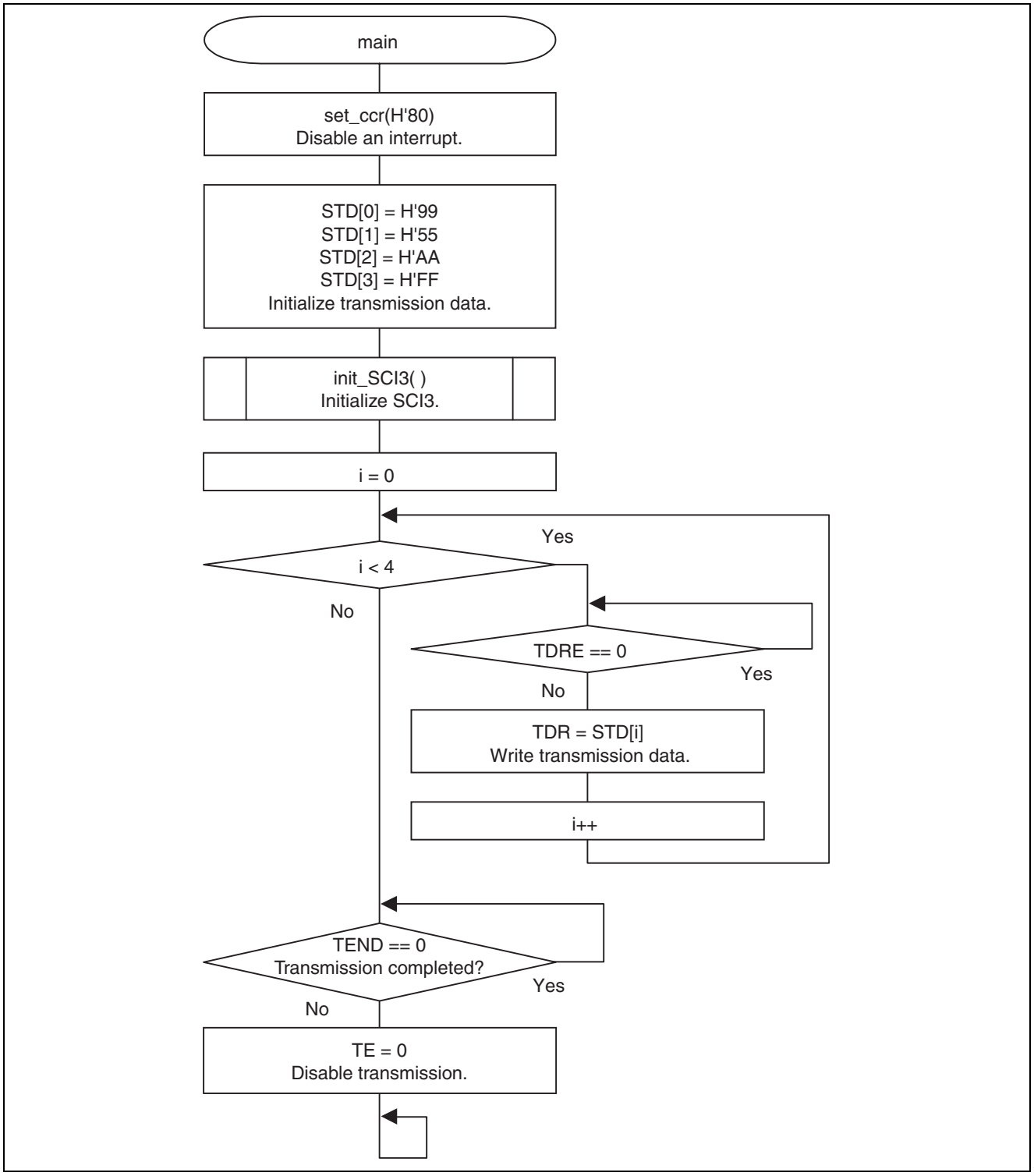
- Table 3 describes RAM usage in this sample task.

Table 3 RAM Usage

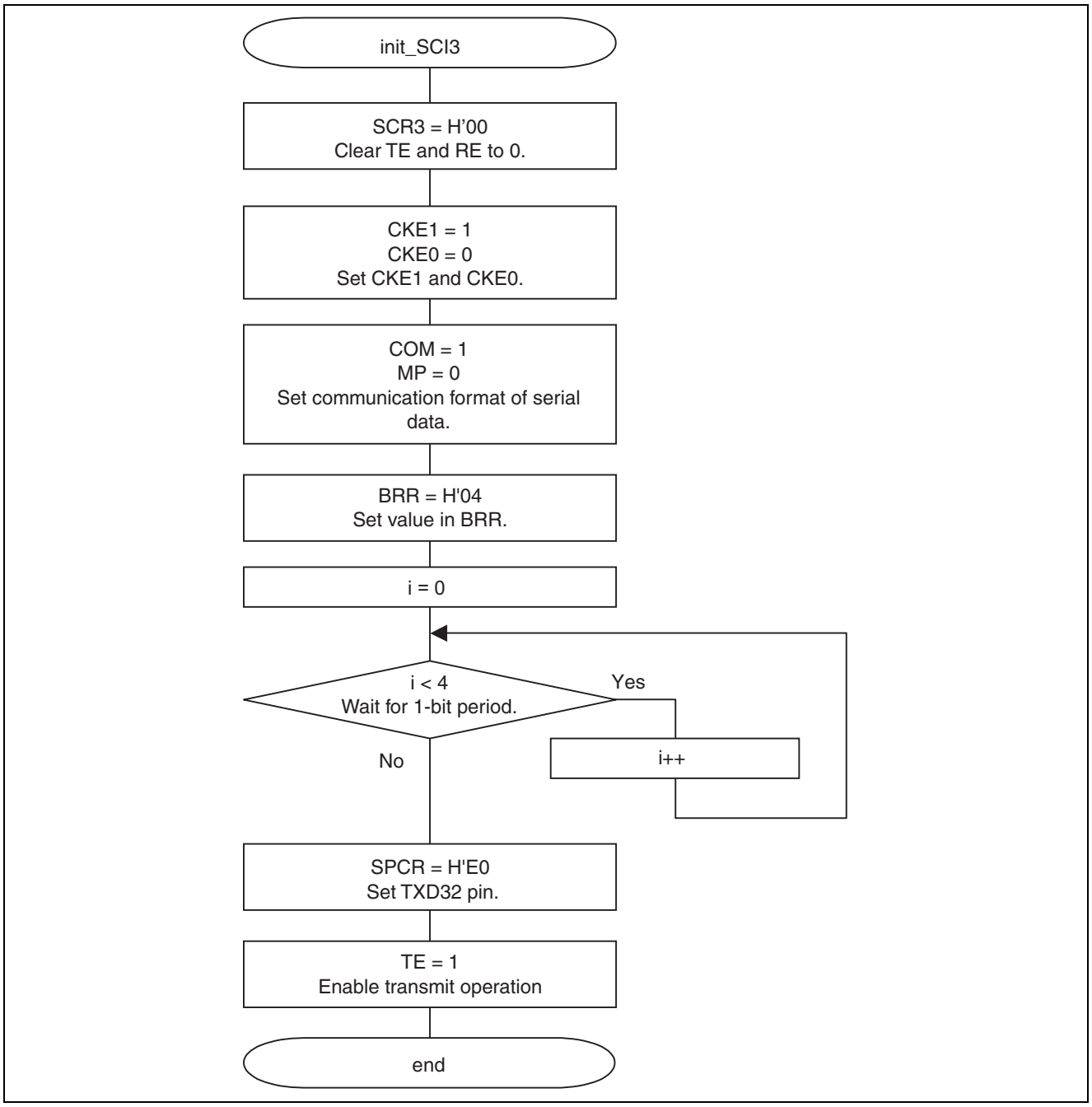
Argument	Description	Address	Amount of Memory Used	Function Used
STD[4]	Buffer for storing clock synchronization serial transmitted data	H′FB80	4 bytes	main

5. Flowchart

5.1 main



5.2 init_SCI3


init_SCI3
SCR3 = H'00
Clear TE and RE to 0.
CKE1 = 1
CKE0 = 0
Set CKE1 and CKE0.
COM = 1
MP = 0
Set communication format of serial data.
BRR = H'04
Set value in BRR.
i = 0
i < 4
Wait for 1-bit period.
Yes
i++
No
SPCR = H'E0
Set TXD32 pin.
TE = 1
Enable transmit operation
end

5.3 Link Addresses

Section Name	Address
CV1	H′0000
P	H′0100
B	H′FB80

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.16.04	—	First edition issued

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