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H8/300L SLP Series

Clock Synchronization Serial Data Master Reception

Introduction

This application note describes clock synchronization serial data master reception using the Serial Communication Interface 3 (SCI3) module of the H8/38024.

Target Device

H8/38024

Contents

1. Specifications

- Clock synchronization serial data master reception is performed using SCI3 of the H8/38024, as shown in figure 1.
- Four bytes of serial data are received in this sample task.
- The communication format is the LSB first format with the data length fixed to 8 bits, and the bit rate is 250 kbps.

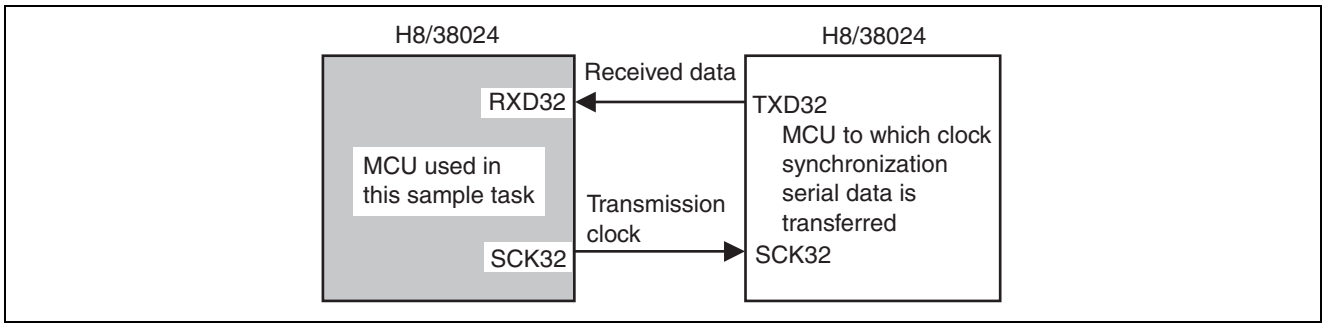


Figure 1 Clock Synchronization Serial Data Master Reception with the H8/38024

2. Description of Functions

- In this sample task, clock synchronization serial data master reception is performed using Serial Communication Interface 3 (SCI3). A block diagram of SCI3 is shown in Figure 2 and the functions are described below the figure.

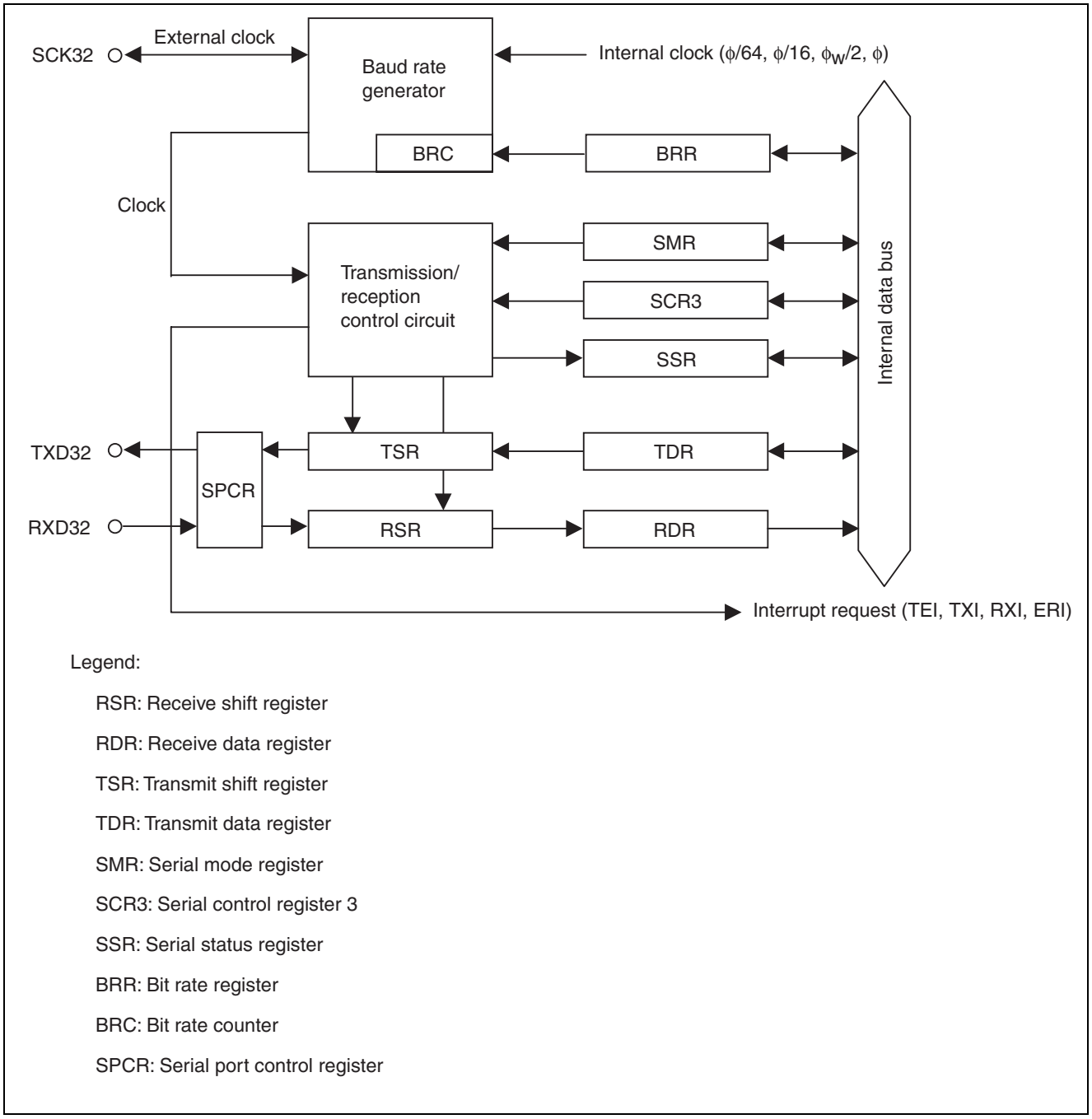


Figure 2 Block Diagram of SCI3

- Clock synchronization mode
  Data is transmitted or received in synchronization with clock pulses. It is possible to perform serial data communication with another LSI that has the clock synchronization communication function. The length of communication data is fixed to 8 bits.
- Internal clock ϕ
  This reference clock is used for operation of built-in peripheral functions and is generated by the clock pulse generator (CPG).
- Receive shift register (RSR)
  This register is used to receive serial data. Serial data that is input from the RXD32 pin is set in RSR in the order in which the data is received, beginning with LSB (bit 0). The data is then converted into parallel data. After one frame of data has been received, the data is automatically transferred to the receive data register (RDR). RDR cannot be accessed by the CPU.
- Receive data register (RDR)
  This 8-bit register stores received serial data. After one frame of data has been received, RSR automatically transfers the data to RDR. RSR and RDR have a double-buffer structure, so data can be continuously received. Since RDR is a read-only register, it can only be read by the CPU.
- Serial mode register (SMR)
  This 8-bit register is used to set the serial data communication format and select the clock source for the built-in baud rate generator.
- Serial control register 3 (SCR3)
  This register is used to control transmission/reception and interrupts, and select a clock source for transmission/reception.
- Serial status register (SSR)
  This register consists of the SCI3 status flags and transmit/receive multiprocessor bits. TDRE, RDRF, OER, FER, and PER can only be cleared.
- Bit rate register (BRR)
  This 8-bit register is used to adjust the bit rate. Since SCI3 has an independent baud rate generator for each channel, a separate bit rate can be set. For details related to settings and the execution rate, see the hardware manual.
- Port mode register 2 (PMR2)
  This register controls switching of the P43/$\overline{\text{IRQ0}}$ pin function.
- IRQ edge select register (IEGR)
  This register is used to specify the rising or falling edge sense of the $\overline{\text{IRQ0}}$ pin.
- Interrupt enable register 1 (IENR1)
  This register enables or disables an $\overline{\text{IRQ0}}$ interrupt request.
- Interrupt request register 1 (IRR1)
  When an $\overline{\text{IRQ0}}$ interrupt request is issued, the corresponding flag is set to 1.

- Table 1 describes the pins and registers used in this sample task.

Table 1 Assignment of Functions

	Name	Description
Pins	SCK32	SCI3 clock input/output pin
	TXD32	SCI3 transmit data output pin
	RXD32	SCI3 receive data input pin
Registers	SMR	Sets the communication format to the clock synchronization mode. Sets the clock source for the built-in baud rate generator to ϕ clock.
	SCR3	Enable receive operation
	SSR	Status flag indicating the SCI3 operating state
	BRR	Sets the communication bit rate.
	TSR	This register is used to transmit serial data.
	TDR	This register stores transmission data.
	RSR	This register is used to receive serial data.
	RDR	This register stores received data.
	SPCR	Does not invert RXD32 input data.
	PMR2	Functions as the $\overline{\text{IRQ0}}$ input pin.
	IEGR	Detects the falling edge of $\overline{\text{IRQ0}}$ pin input.
	IENR1	Enables an $\overline{\text{IRQ0}}$ pin interrupt request.
	IRR1	$\overline{\text{IRQ0}}$ interrupt request flag

3. Principles of Operation

- Figure 3 illustrates operation during clock synchronization mode reception in this sample task. It also describes software and hardware processings.

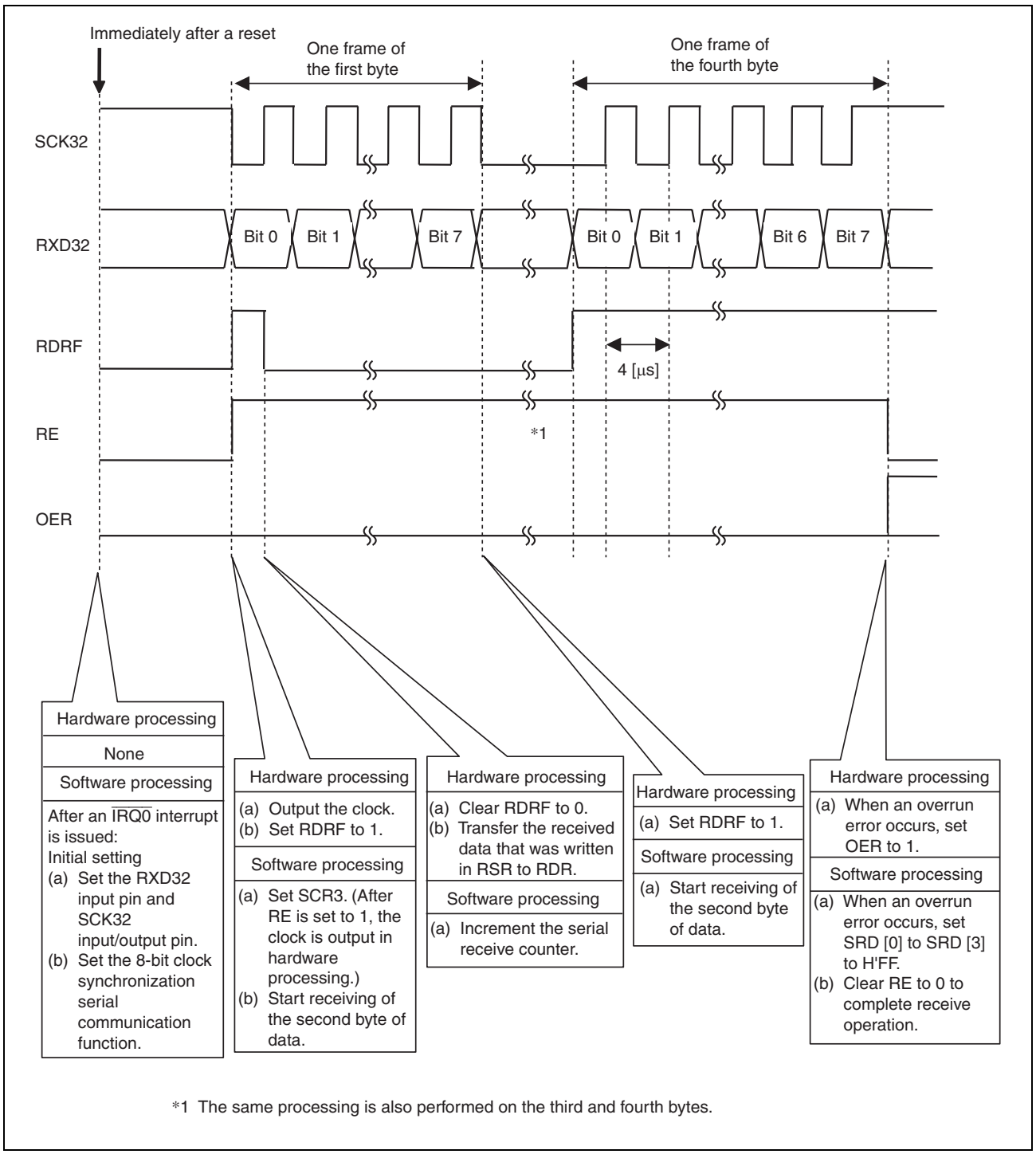


Figure 3 Operation during Reception of Data

4. Description of Software

4.1 Description of Modules

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Function	Description
main	Sets clock synchronization serial data master receive operation and the $\overline{\text{IRQ0}}$ interrupt.
init_SCI3	Initializes SCI3.
irq0int	Handles the $\overline{\text{IRQ0}}$ interrupt.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

The internal registers used in the sample task are described below. The following settings are the values used in this sample task, not the default values.

- SPCR Serial port control register Address: H′FF91

Bit No.	Bit Name	Setting	R/W	Description
2	SCINV2	0	R/W	Switching of RXD32 pin input data inversion Does not invert data input from the RXD32.

- SMR Serial mode register Address: H′FFA8

Bit No.	Bit Name	Setting	R/W	Description
7	COM	1	R/W	Communication mode Operates SCI3 in the clock synchronization mode.
2	MP	0	R/W	Multiprocessor mode Disables the multiprocessor communication function.
1	CKS1	0	R/W	Clock select 1, 0
0	CKS0	0		Select ϕ clock as the clock source for the built-in baud rate generator.

- BRR Bit rate register Address: H′FFA9
  Function: 8-bit register used to set the transmit and receive bit rates according to the operating clock of the baud rate generator selected by CKS1 and CKS0.
  Setting: H′04
  R/W: R/W

- SCR3 Serial control register 3 Address: H′FFAA

Bit No.	Bit Name	Setting	R/W	Description
4	RE	1	R/W	Receive enable Enables receive operation. (The RXD32 pin is used as the receive data pin.)
1	CKE1	0	R/W	Clock enable 1, 0
0	CKE0	0	R/W	Selects the internal clock as the clock source and selects the synchronization clock output as the SCK32 pin function.

- SSR Serial status register Address: H′FFAC

Bit No.	Bit Name	Setting	R/W	Description
6	RDRF	-	R/(W)*	Receive data register full RDRF = 0: Data is not stored in RDRF. RDRF = 1: Data is stored in RDRF.
5	OER	0	R/(W)*	Overrun error OER = 0: Reception is completed or in progress. OER = 1: An overrun error occurred during reception.
4	FER	0	R/(W)*	Framing error FER = 0: Reception is completed or in progress. FER = 1: A framing error occurred during reception.
3	PER	0	R/(W)*	Parity error PER = 0: Reception is completed or in progress. PER = 1: A parity error occurred during reception.

"-" indicates "Don't care".
* Only 0, which clears the flag, can be written.

- RDR Receive data register Address: H′FFAD
  Function: 8-bit register that stores received data.
  Setting: -
  R/W: R

- PMR2 Port mode register 2 Address: H′FFC9

Bit No.	Bit Name	Setting	R/W	Description
0	$\overline{\text{IRQ0}}$	1	R/W	Switching of the P43/$\overline{\text{IRQ0}}$ pin function $\overline{\text{IRQ0}}$ = 0: The pin functions as the P43 pin. $\overline{\text{IRQ0}}$ = 1: The pin functions as the $\overline{\text{IRQ0}}$ input pin.

- IEGR IRQ edge select register Address: H′FFF2

Bit No.	Bit Name	Setting	R/W	Description
0	IEG0	0	R/W	$\overline{\text{IRQ0}}$ edge select IEG0 = 0: The falling edge of $\overline{\text{IRQ0}}$ pin input is detected. IEG0 = 1: The rising edge of $\overline{\text{IRQ0}}$ pin input is detected.

- IENR1 Interrupt enable register 1 Address: H′FFF3

Bit No.	Bit Name	Setting	R/W	Description
0	IEN0	1	R/W	$\overline{\text{IRQ0}}$ interrupt enable IEN0 = 0: An $\overline{\text{IRQ0}}$ pin interrupt request is disabled. IEN0 = 1: An $\overline{\text{IRQ0}}$ pin interrupt request is enabled.

- IRR1 Interrupt request register 1 Address: H′FFF6

Bit No.	Bit Name	Setting	R/W	Description
0	IRRI0	0	R/(W)*	$\overline{\text{IRQ0}}$ interrupt request flag [Clearing condition] When 0 is written if IRRI0 is 1 [Setting condition] When the $\overline{\text{IRQ0}}$ pin is set as interrupt input and the specified edge is input in the $\overline{\text{IRQ0}}$ pin

* Only 0, which clears the flag, can be written

4.4 RAM Usage

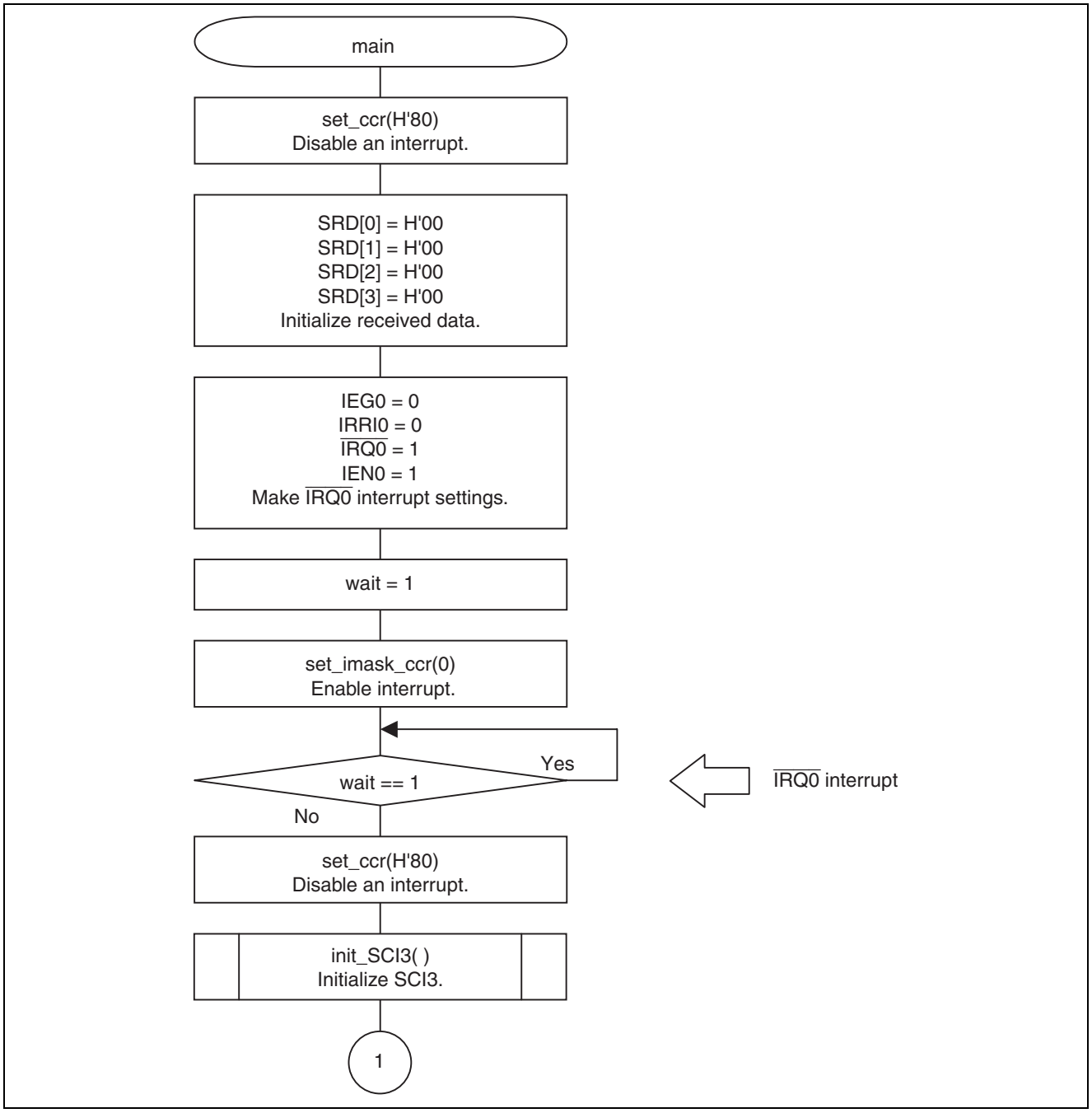
- Table 3 describes RAM usage in this sample task.

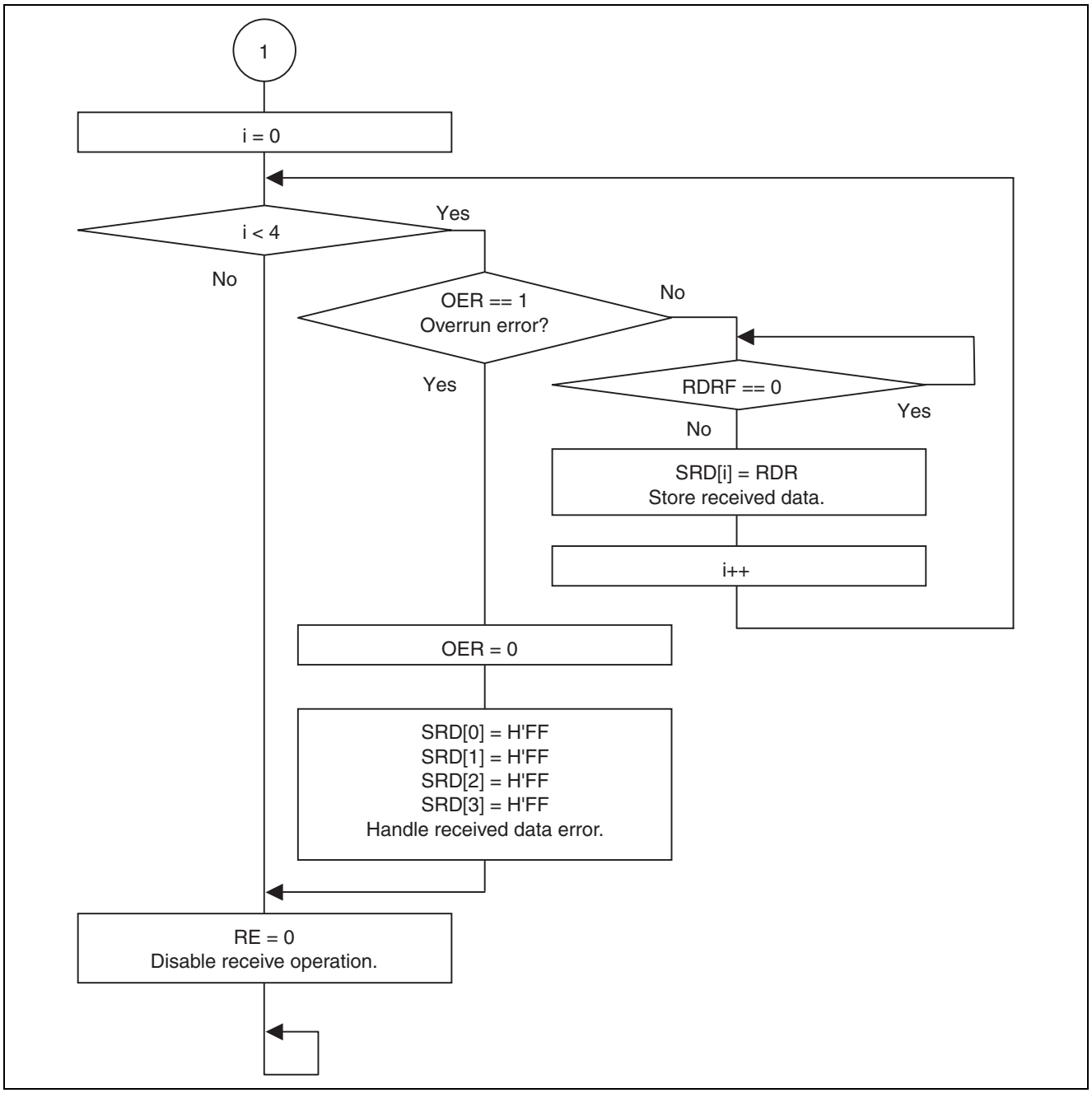
Table 3 RAM Usage

Argument	Description	Address	Amount of Memory Used	Function Used
SRD[4]	Buffer storing clock synchronization serial received data	H′FB80	4 bytes	main
wait	Waiting for an $\overline{\text{IRQ0}}$ interrupt	H′FB84	1 byte	main, inq0int

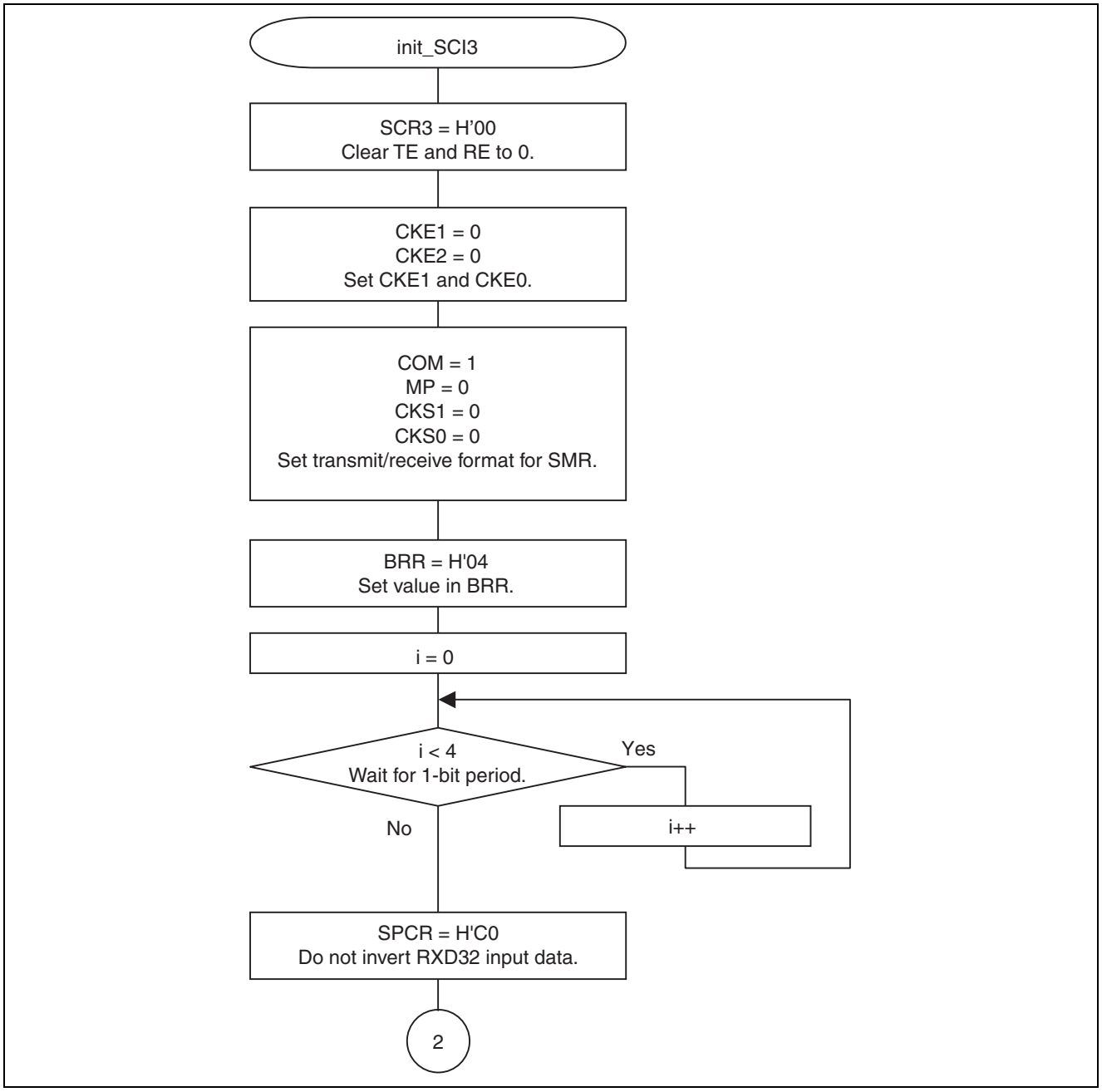
5. Flowchart

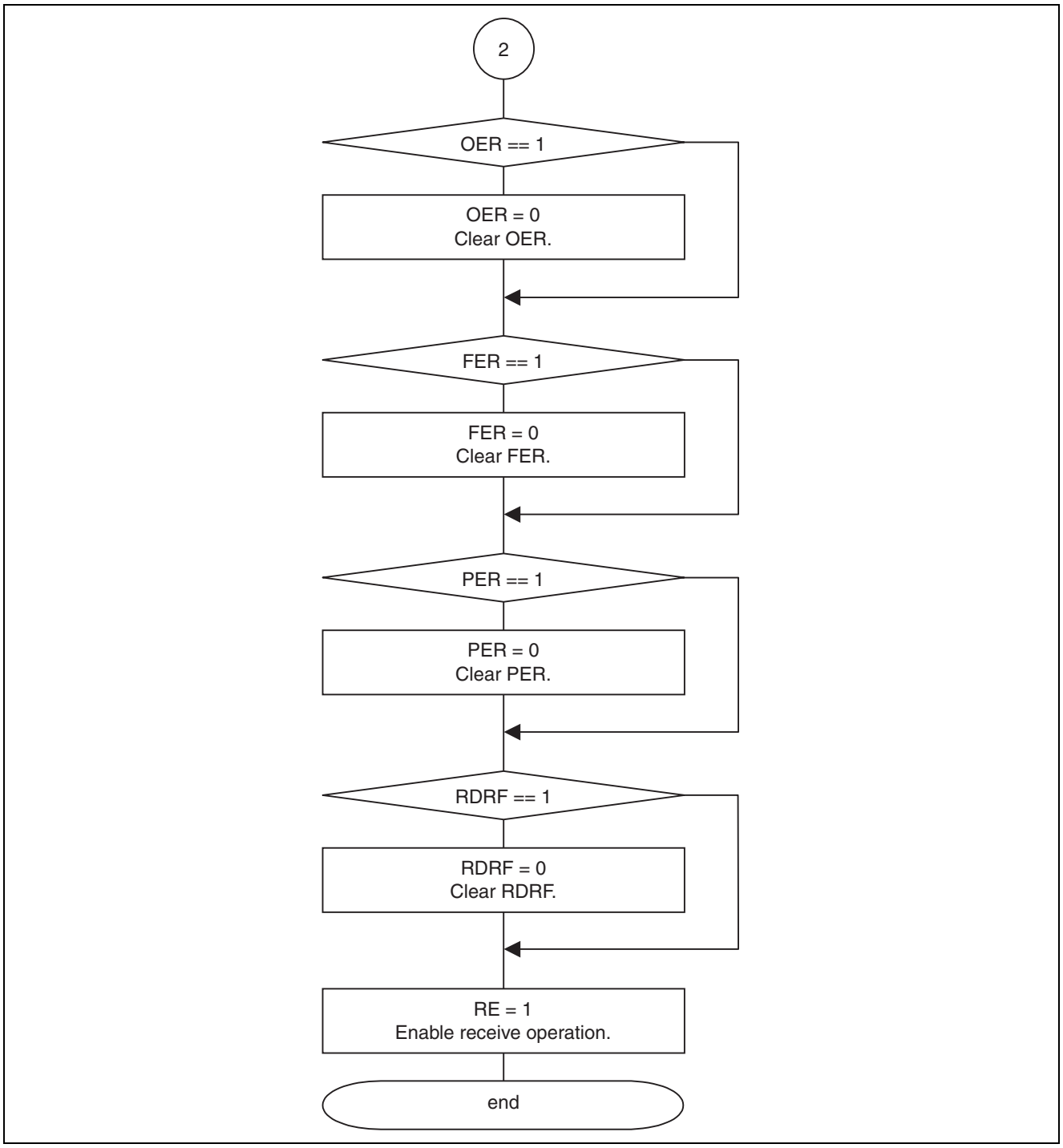
5.1 main



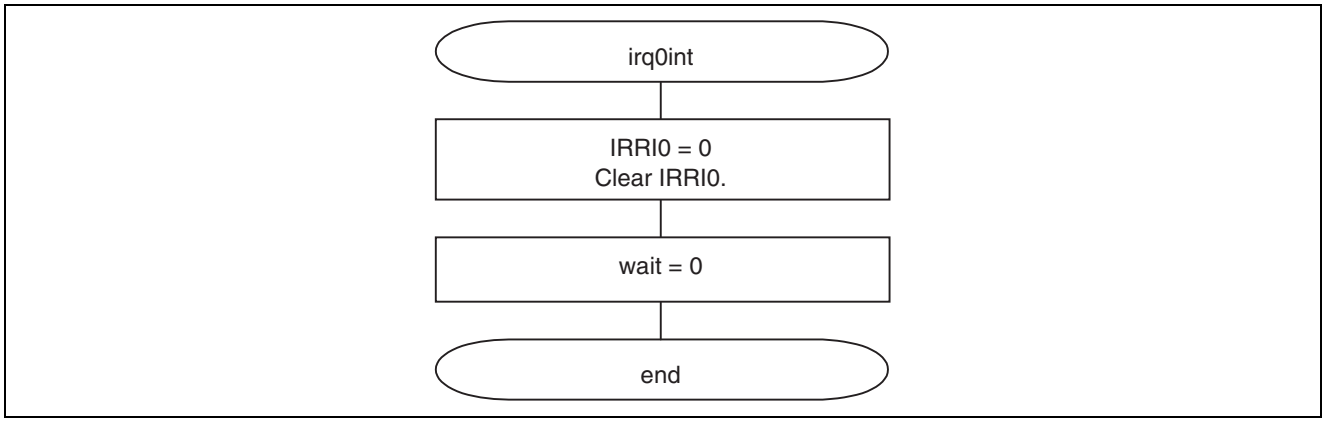

1
i = 0
i < 4
Yes
No
OER == 1
Overrun error?
No
Yes
RDRF == 0
Yes
No
SRD[i] = RDR
Store received data.
i++
OER = 0
SRD[0] = H'FF
SRD[1] = H'FF
SRD[2] = H'FF
SRD[3] = H'FF
Handle received data error.
RE = 0
Disable receive operation.

5.2 init_SCI3


init_SCI3
SCR3 = H'00
Clear TE and RE to 0.
CKE1 = 0
CKE2 = 0
Set CKE1 and CKE0.
COM = 1
MP = 0
CKS1 = 0
CKS0 = 0
Set transmit/receive format for SMR.
BRR = H'04
Set value in BRR.
i = 0
i < 4
Wait for 1-bit period.
Yes
No
i++
SPCR = H'C0
Do not invert RXD32 input data.
2


2
OER == 1
OER = 0
Clear OER.
FER == 1
FER = 0
Clear FER.
PER == 1
PER = 0
Clear PER.
RDRF == 1
RDRF = 0
Clear RDRF.
RE = 1
Enable receive operation.
end

5.3 irq0int



5.4 Link Addresses

Section Name	Address
CV1	H'0000
CV2	H'0008
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Jul.16.04	—	First edition issued

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