

#### Description

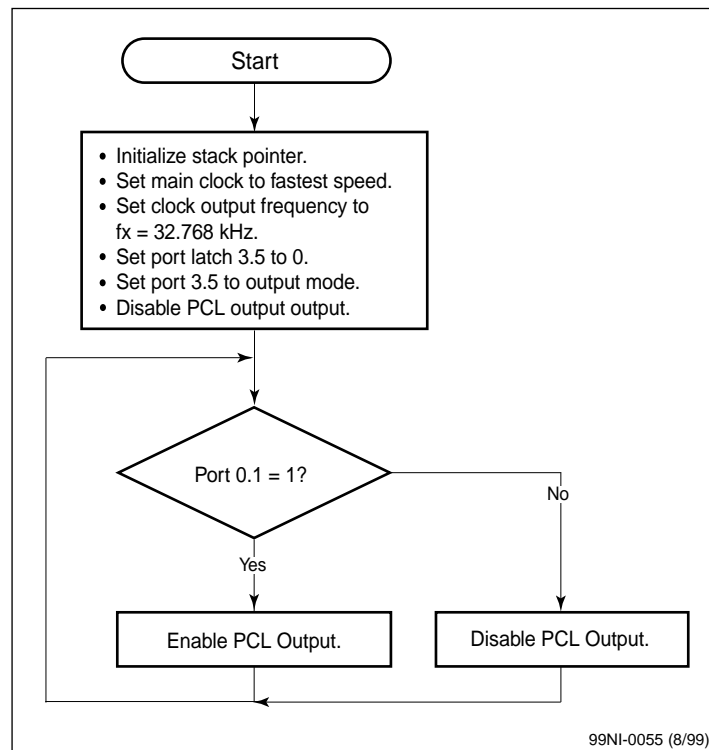
The clock output control circuit in the  $\mu$ PD7805x/78005x subseries is intended for carrier output during remote controlled transmission and clock output for supply to peripheral LSI. Clocks selected with timer clock select register 0 (TCL0) are output to clock output pin (PCL/P35).

Applying a high level at port 0.1 causes the example program to output the subclock frequency (32.768 kHz) to pin PCL/P35. If the level at port 0.1 is low, the output is disabled.

#### Program Specifications

- ❑ Clock output frequency:  $f_{xt} = 32.768$  kHz (subsystem clock)
- ❑ Output enable: port 0.1 enables or disables the output
- ❑ Pins used in program:
  - PCL/P35: output of the subsystem clock frequency
  - P01/INTP1/TI01:
    - P01 = 1: output frequency enabled
    - P01 = 0: output frequency disabled

#### Flowchart



## Assembly Language Program

```

;*****
; Date:      05/08/1999
;
; Parameters: - Fastest CPU clock
;              (fx = 5 MHz; 1 CPU clock cycle = 200ns)
;              - Pulse frequency is sub-system clock (32.768 kHz)
;              - Pulse output at pin PCL/P35
;              - Port 0.1 enables or disables the frequency output
;*****

;=====
;   Specify Interrupt Vectors           =
;=====

Res_Vec CSEG      AT 0000h              ; Set main program start vector
        DW        Start

;*=====
;               Main Program           =
;=====

MAIN     CSEG
Start:   DI                    ; Disable interrupts
        MOVW       AX, #0FE20h        ; Load SP address
        MOVW       SP, AX             ; Set Stack Pointer
        MOV        OSMS,#01h          ; Don't use scaler
        MOV        PCC, #00h          ; Main system clock at fastest setting
        MOV        TCL0,#00           ; Set PCL output clock to subsystem clock
        CLR1       P3.5               ; Set port 3.5 to low
        CLR1       PM3.5              ; Set port 3.5 to output mode
Loop:    BF         P0.1,$Main10       ; Test port 0.1 state
        SET1       CLOE               ; Enable PCL output
        BR         Loop               ; Branch back to Loop
Main10:  CLR1       CLOE               ; Disable PCL output
        BR         Loop               ; Branch to Loop

        END

```

### C Language Program

```

/*****
; Date:      05/08/1999
;
; Parameters: - Fastest CPU clock
;              (fx = 5 MHz; 1 CPU clock cycle = 200ns)
;              - Pulse frequency is sub-system clock (32.768 kHz)
;              - Pulse output at pin PCL/P35
;              - Port 0.1 enables or disables the frequency output

;*****/
/* extension functions in K0/K0S compiler */
#pragma sfr      /* key word to allow SFR names in C code */
#pragma asm      /* key word to allow ASM statements in C code */

/*=====
;          Constants/Variables      =
;=====*/

#define TRUE     1
#define FALSE    0

/*=====
;          Main Program              =
;=====*/

void main(void)
{
    OSMS = 0x01;    /* Don't use scaler */
    PCC = 0x00;     /* Main system clock at fastest setting */
    TCL0 = 0x00;    /* Set PCL output clock = 32.768 kHz */

    P3.5 = 0;       /* Set port 3.5 to low */
    PM3.5 = 0;      /* Set port 3.5 to output mode */
    while(TRUE)
    {
        if(P0.1 == TRUE )    /* Test port 0.1 state */
            CLOE = 1;        /* Enable PCL output */
        else
            CLOE = 0;        /* P0.1 = LOW, Disable PCL output */
    }
    /* end of while loop */
    /* end of function main() */
}

```



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