Choosing the Right Crystal for Clocking Devices

This application note describes the criteria for selecting a crystal for providing a clock signal to clock synthesizer and timing integrated circuits.

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1. Introduction

The selection of a crystal for providing a clock signal involves several choices that can affect the accuracy and performance of the final application. It is important to consider several criteria when selecting a crystal, such as the nominal frequency, frequency tolerance, crystal load capacitance, Equivalent Series Resistance (ESR), operating temperature, drive level rating and aging tolerance. This application note describes how to select the right crystal based on those parameters.

2. Frequency Selection

The first requirement is to select a crystal with a fundamental frequency within the allowed range of the device. The frequency chosen for the application depends on the mode of operation of the device and the amount of noise (jitter) that can be tolerated by the application. A clock synthesizer will have a different set of requirements for the crystal's frequency than a jitter attenuator. Selecting a sub-optimal crystal frequency can result in spurs that may impact the performance and even the functionality of the application. The following sections provide more details.

2.1 Clock Synthesizer vs Jitter Attenuator

A clock synthesizer generates one or more clock signals, each of which have a fixed but programmable frequency. For best performance, the output frequency should be integer related to the crystal frequency.

A jitter attenuator takes an input clock signal and cleans up the jitter to produce an output clock signal with better performance. The latest generation of Renesas jitter attenuators uses a fractional-feedback PLL (see Figure 1). This fractional-feedback PLL employs a Sigma-Delta Modulator (SDM) to generate an output frequency (f_{OUT}) that is a non-integer multiple of the input reference frequency (f_{IN}). The SDM can have noise related to integer boundaries. For more details, see section 2.2.

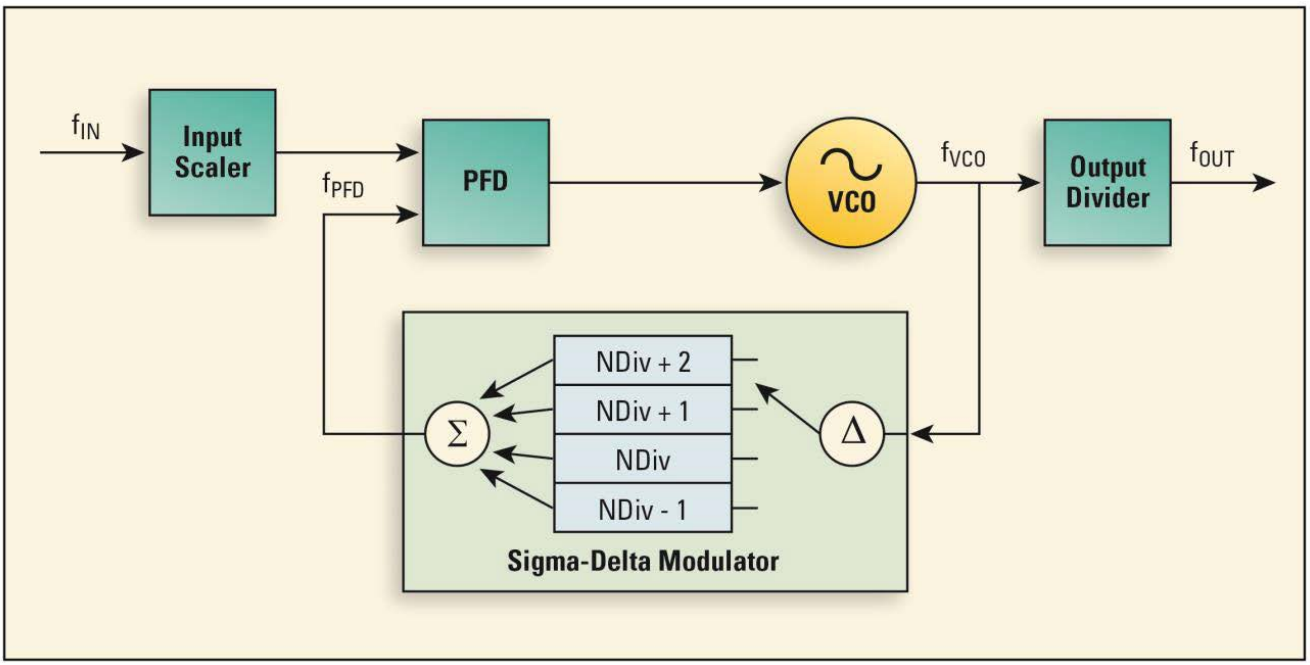

Figure 1. Fractional-Feedback PLL

2.2 Integer Boundary Spurs

The ability of fractional-feedback PLLs to produce an output frequency that is a non-integer multiple of the input frequency involves a number of sub-systems such as the SDM, phase frequency detector (PFD), and the VCO. The interaction between these sub-systems can produce spurs that show up in a frequency spectrum plot of the output signal. Integer boundary spurs can occur when the PLL feedback loop fractional divide ratio is programmed to a value very close to an integer. Fractional spurs are a subset of integer boundary spurs.

In general, integer boundary spurs are more difficult to mitigate than fractional spurs. To avoid integer boundary spurs, it is recommended that the ratio of crystal frequency verses output frequency should not have an integer relationship and should not have a fractional component close to 0 or 1 and should not be equal to 0.5 (i.e., xxx.999, xxx.001, xxx.5). For more details, see the Integer Boundary Spurs in Fractional-Feedback Phase-Locked Loops (PLLs) white paper.

2.3 Selecting a Crystal Frequency for a Clock Synthesizer

When selecting a crystal for a clock synthesizer application, it is best to choose a crystal frequency that is an integer relationship to the desired output frequency in order to minimize the output jitter. For example, if a clock synthesizer is required to output 100MHz and 150MHz, a 50MHz crystal would be an appropriate choice.

2.4 Selecting a Crystal Frequency for a Jitter Attenuator

When selecting a crystal for a jitter attenuation application, avoid a simple ratio (1:1, 1:2, 1:4, etc.) as well as fractional values close to 0, 0.5, and 1 between the crystal frequency and output frequency (see section 2.2). Having these relationships between the crystal frequency and the output frequency can produce integer boundary spurs.

3. Performance vs Frequency

The PFD of the fractional-feedback PLL is based on a time-to-digital converter (TDC) which is based on the frequency of the crystal. A higher crystal frequency allows the TDC to measure a period with greater precision that reduces the jitter on the output signal.

Figure 2 illustrates the performance of a clock synthesizer over the frequency spectrum of the output signal using the Renesas 8A34001 System Synchronizer for IEEE 1588 as the clock synthesizer. The phase noise of the output dependent on the 25MHz crystal is higher than the output dependent on the 50MHz crystal. The difference in the close-in frequency offset (100Hz to 10kHz) between the two crystal frequencies is due to the differences between the two crystals. The offset at 100kHz is due to the difference in the bandwidth of the fractional-feedback PLL closed loop for each crystal frequency. Selecting a higher frequency crystal will improve the close-in frequency offset phase noise of the application.

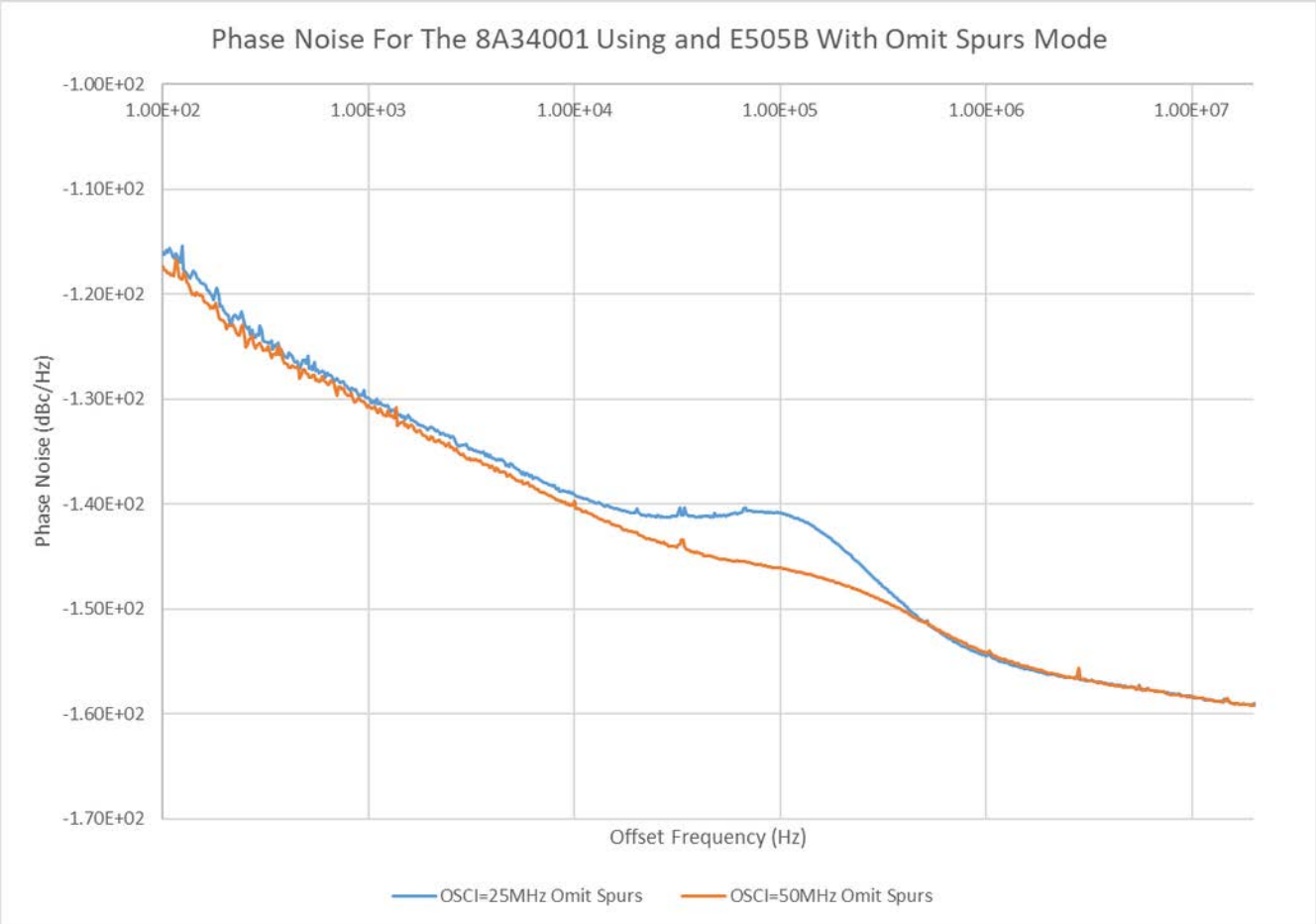

Figure 2. Phase Noise Plots of a Clock Synthesizer using a 25MHz Crystal Compared to a 50MHz Crystal

4. Crystal Parameters

4.1 Load Capacitance

When selecting the value for the load capacitance (C_L), it is important to refer to the datasheet of the device to determine the device's ESR specifications for a given C_L value. The ESR requirements of the device are affected by the value of the load capacitance and the crystal's fundamental frequency (see section 4.2). If the total capacitive load on the crystal is less than the specified C_L, it will cause the crystal to oscillate at slightly higher frequency and vice-versa an extra load capacitance will slightly decrease the frequency. For assistance in calculating the load capacitance, it is recommended that the PC Clock Tools (MS Excel Spreadsheet) is downloaded. The "XtalCL" tab contains fields that can be filled out from information referenced from the datasheets of the crystal and the device and returns an ideal value for the load capacitance.

The load capacitance is also important to ensure reliable start-up of the crystal oscillator. It is recommended that a load capacitance of 8pF or greater is used due to the difficulty of designing a printed circuit board with a stray capacitance of 6pF or less. A load capacitance of 8pF ensures there is some margin for fine-tuning the capacitance using external tuning capacitors. For crystal frequencies greater than 40MHz, the recommendation is that the load capacitance be kept less than 18pF. A higher load capacitance will lead to higher drive levels.

4.2 Equivalent Series Resistance (ESR)

When selecting a crystal for a device, it is important to refer to the datasheet of the device for guidance on ensuring that the ESR of the crystal falls within the specifications of the device. If a crystal's ESR exceeds the specifications of the device, there could be an issue with the start-up of the crystal oscillation. The size of the crystal will influence the crystal's ESR, with smaller package crystals having a higher ESR.

4.3 Total Frequency Variation

The total frequency variation of a crystal is due to the combination of the frequency tolerance, frequency stability, and aging of the crystal. These parameters are customer/application dependent, and the customer is free to adjust these parameters to their requirements. The equation is:

Target Frequency Variation = Frequency Tolerance + Frequency Stability + Aging

For example, if the application requires a maximum of ±50ppm Total Frequency Variation, then the following specifications will allow that crystal to meet the spec:

- Frequency tolerance = ±20ppm
- Frequency stability = ±20ppm over the operating temperature
- Aging = ±10ppm

The following sections provide descriptions of those specifications.

4.3.1. Frequency Tolerance

The frequency tolerance is the accuracy of the nominal frequency typically when the crystal is operated at 25°C. Select a manufacturing tolerance that will be acceptable for the application.

4.3.2. Frequency Stability and Operating Temperature

Select an operating temperature range for the crystal appropriate to the operating temperature range of the application. Operating the crystal outside this range will cause the frequency to exceed the published stability range, and it may prematurely age the crystal (increased ppm frequency change over time) or damage the housing of the crystal.

The frequency stability of the crystal is a measure of the frequency shift over the operating temperature of the crystal. When tight frequency tolerances (±10ppm) over the operating temperature range are a requirement, it may be necessary to use a TCXO (temperature compensated crystal oscillator) or an OCXO (oven-controlled crystal oscillator) instead.

4.3.3. Aging Tolerance

Confirm that the crystal aging tolerance (ppm per year) meets the application requirements. Over-driving the crystal, shock and vibration, and operating the crystal outside of its specified temperature range will accelerate aging. If the crystal will experience shock or vibration in its application, consider an oven-controlled SC-cut crystal, which is more tolerant of vibration.

4.4 Drive Level

The drive level of the crystal is the power the crystal dissipates during oscillation. Confirm that the maximum drive level rating of the crystal is greater than the maximum drive level of the device. For example, a standard crystal may have a typical drive level rating of 10µW and a maximum of 100µW. However, some devices may require a rating of 300µW. In such case, a crystal with a 300µW rating would be necessary. If the drive level of the crystal is exceeded, it can lead to premature aging of the crystal and possible damage to the crystal housing. Exceeding the drive level can also excite undesired harmonics inside the crystal, leading to spurs in the application.

5. Revision History

Revision	Date	Description
1.00	Oct 31, 2022	Initial release.

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