Capacitive Sensor Microcontrollers

CTSU Capacitive Touch Electrode Design Guide

Introduction

This application note describes how to design electrode patterns, with sample patterns for reference, for MCUs embedding the Capacitive Touch Sensing Unit (CTSU).

For information on the power supply design and layout of microcontrollers, refer to the following application notes.

- Capacitive Sensor MCU Capacitive Touch Ripple Noise Prevention Guide

Target Device

RX Family, RA Family, and RL78 Family MCUs and Renesas Synergy™ embedding the CTSU

(CTSU indicates CTSU2, CTSU2L, CTSU2SL, etc.)

In addition, refer to CTSU2 for CTSU2L/CTSU2La/CTSU2SL/CTSU2SLa after the next page.

Contents

1. Outline

Capacitive touch button sensitivity and anti-noise performance are both influenced by the shape and size of the touch electrode pad (herein referred to as “electrode”), wire routing, patterns surrounding the electrode, overlay panel thickness, inclusion of air gap, internal configuration of product housing, and other factors. All of these factors need to be taken into consideration when designing the electrode as well as the surrounding area.

This application note describes how to design electrode pads and wiring as well as how to deal with related issues and potential problems when using the Renesas Touch Capacitance Sensor Unit (CTSU). It also provides recommended applications.

2. Self-capacitance Method Buttons: Electrode Layout Patterns

2.1 Outline of Design Recommendations

The following provides reference information for designing self-capacitance method buttons on a two-sided printed board We recommend using a 2- or more layer board and placing a shield guard of a cross-hatched GND pattern (referred to as “cross-hatched GND shield” herein) around the touch electrodes and on the area directly underneath the touch electrodes to suppress parasitic capacitance fluctuations due to the surrounding environment and noise factors as well as a measure to handle external noise. We also recommend using an ESD countermeasure by shielding the outer circumference of the board with a solid GND pattern. The numbers listed here correspond to the numbers in Figure 2-1, excluding numbers ⑨ and ⑩. Each item is described in detail later.

① Electrode shape: square or circle
② Electrode size: 10mm to 15mm
③ Electrode proximity: Electrodes should be placed with ample distance so that they do not react simultaneously to the target human interface, (referred to as “finger” in this document); suggested interval: button size x 0.8 or more
④ Wire width: approx. 0.15mm to 0.20mm for printed board
⑤ Wiring length: Make the wiring as short as possible. On corners, form a 45-degree angle, not a right angle.
⑥ Wiring spacing:
 (A) Make spacing as wide as possible to prevent false detection by neighboring electrodes.
 (B) 1.27mm pitch
⑦ Cross-hatched GND pattern width: 5mm
⑧ Cross-hatched GND pattern and button/wiring spacing
 (A) area around electrodes: 5mm (B) area around wiring: 3mm or more
 Cover the electrode area as well as the wiring and opposite surface with a cross-hatched pattern. Also place a cross-hatched pattern in the empty spaces, and connect the 2 surfaces of cross-hatched patterns through vias.
 Refer to section “2.5 Anti-Noise Layout Pattern Designs” for cross-hatched pattern dimensions, active shield (CTSU2 only), and other anti-noise countermeasures.
⑨ Electrode + wiring capacitance: See Table 2-1 and Table 2-2.
 For other conditions, see 4.2 Base Clock Frequency/Sensor Drive Pulse Frequency Settings.
⑩ Electrode + wiring resistance: 560Ω to 1kΩ (including damping resistor with reference value of 560Ω)
 Place the damping resistor as close as possible to the TS pin.

For additional noise countermeasures such as ⑦ Cross-hatched pattern dimensions and ⑧ Active shield (CTSU2 only), refer to 2.5 Anti-Noise Layout Pattern Designs.

For cautions when exceeding the recommended values of ⑨ and ⑩, refer to 2.4 Electrode Pattern Design.

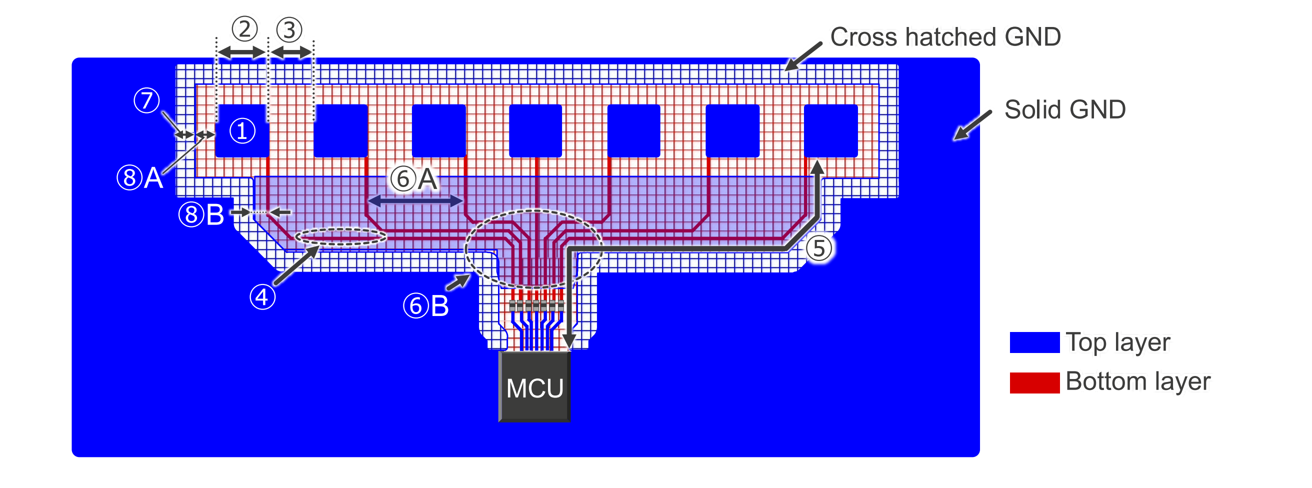


Figure 2-1. Example of Anti-noise Layout Pattern for Self-capacitance Method Buttons

Table 2-1 lists the classification of products and types with capacitive Sensors. Table 2-2 lists the List of recommended values for capacitive sensor types and parasitic capacitance (unit: pF) of TS pins. Select the category from Table 2-1 from the device to be used and the CTSU operation mode, and design the pattern so that the parasitic capacitance is less than the recommended value according to the total resistance value of the TS pin from Table 2-2. The recommended parasitic capacitance includes the terminal capacitance of the overlay panel and the TS terminal. The recommended value is that the sensor drive pulse frequency is set to 1MHz or more by the automatic adjustment of QE for Capacitive Touch so that the sensitivity of the button can be obtained sufficiently. For TS pin conditions other than the recommended values that valid range and deprecated range, refer to "4.2 Base Clock Frequency/Sensor Drive Pulse Frequency Settings."

Table 2-1 Classification of Products and Types with Capacitive Sensors

Capacitance Sensor Type		**CTSU1**			**CTSU2**	
Product Category/Family	RL78	RL78/G16	-	-	RL78/G22, RL78/G23 RL78/L23	
					RL78/F22, RL78/F25	
	RX	RX113, RX130 RX230, RX231, RX23W		RX671	RX140 RX260, RX261	
	RA	RA2A1, RA4M1, RA4W1		RA4M2, RA4M3 RA6M1, RA6M2, RA6M3, RA6M4, RA6M5	RA0L1 RA2E1, RA2L1 RA4L1	
CTSU Operating Mode		Normal Operation	Low voltage	Normal Operation	Normal Operation	Low voltage
Category (Note)		A	B	C	D	E

Note: The Category is specific to this application note.

Table 2-2 List of Recommended Values for Capacitive Sensor Types and Parasitic Capacitance (Unit: pF) of TS Pins

Category		**A**	**B**	**C**	**D**	**E**
Total Resistance (Ω)	560	39	22	46	49	36
	620	38	21	44	46	35
	680	36	21	44	44	34
	750	35	20	42	42	33
	820	33	20	40	40	32
	910	32	19	38	37	30
	1000	30	19	36	35	29

2.2 Self-capacitance Method Overview

Figure2-2 shows the self-capacitance generated in the electrode. A single electrode connected to the capacitive sensor in the self-capacitance method button measures capacitance C. The value of C is a composite of parasitic capacitance Cp formed by the electrode and surrounding conductors and parasitic capacitance Cf formed by the electrode and the finger. The size of the capacitance can be considered in the capacitor equation $C = \varepsilon \frac{S}{d}$ (see note). Cp is constant as the surrounding devices are static, but Cf increases as the finger gets closer. By setting a threshold for the amount of increase in Cf, you can determine whether the touch button is ON or OFF. Note that if the finger actually touches the electrode, it will short and no longer be able to measure capacitance. Normally, there is an overlay panel of a few mm between the electrode and the finger.

Note : C: capacitance, ε : Relative permittivity, S: electrode facing area, d: inter-electrode distance

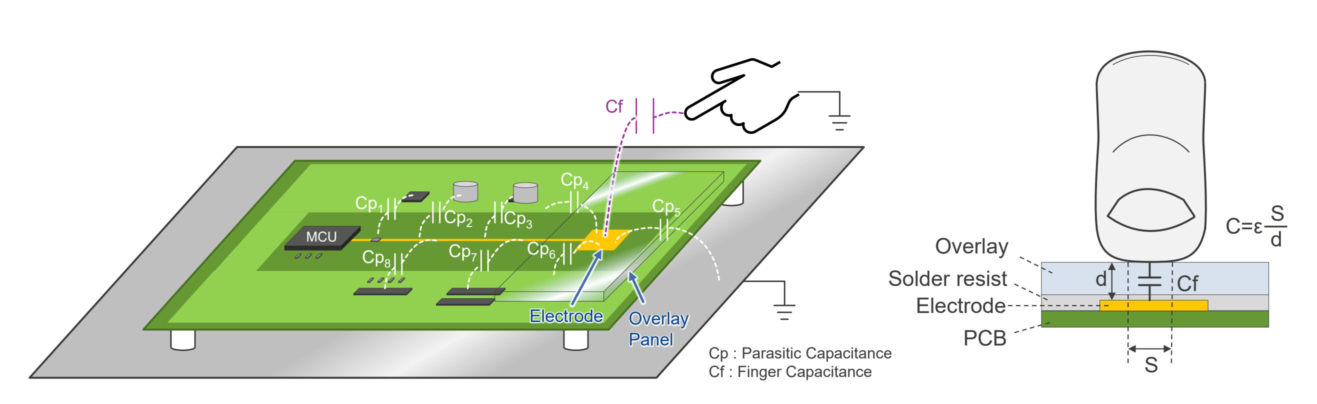


Figure2-2. Image of Self-capacitance Generated in the Electrode

The sensitivity of the touch button is defined by SNR (Signal-to-Noise-Ratio). Figure2-3 shows Button Sensitivity (SNR) Derivation Method. SNR is calculated by taking the difference in measurement values between the touch button ON and OFF (touch/non-touch) states as the signal value, and calculating its ratio to the noise value. Noise can originate from within the MCU or it can be received externally by patterns on the board. A higher SNR results in higher touch button sensitivity. This formula shows a Coefficient as part of the calculation. Recommend referencing Figure 5-1 for the for the value and 5.1 for the calculation examples.

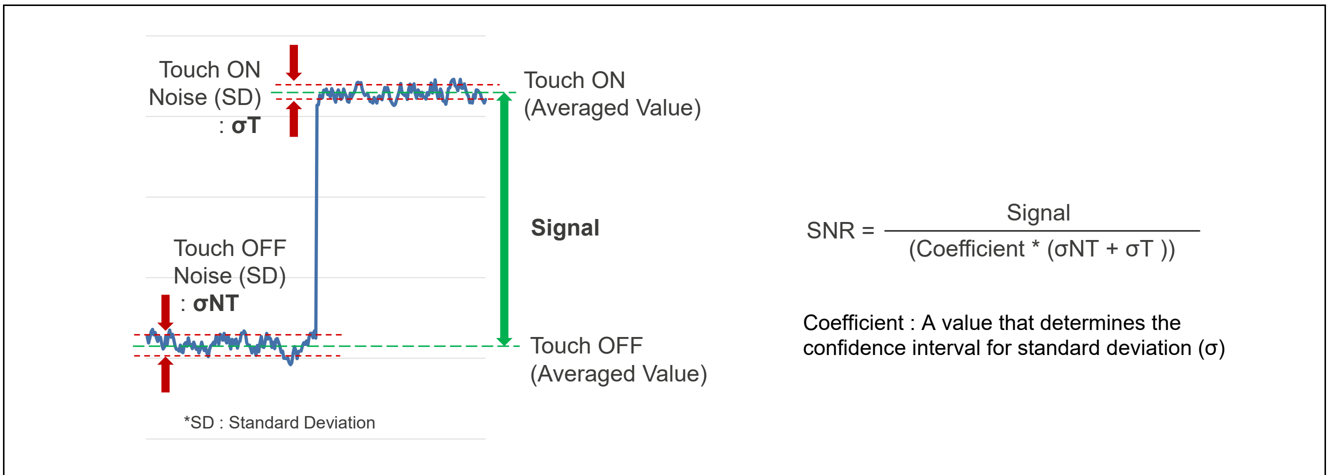


Figure2-3. Button Sensitivity (SNR) Derivation Method

2.3 Principle of CTSU Self-capacitance Method Detection

Figure2-4 shows an overview of the CTSU internal configuration for the self-capacitance method. The CTSU outputs a digital count value proportional to capacitance C of the connected electrode, and determines whether the touch button is ON or OFF by software. When the electrode is connected to the CTSU, it performs as a switched capacitor controlled by the sensor drive pulse frequency and estimates capacitance from the charge/discharge current to C. The CTSU measurement block has a current-frequency conversion function which inputs a current equivalent to the charge/discharge current and outputs a frequency signal proportional to the amount of current. The frequency signal is measured for a fixed period according to the sensor drive pulse output. It is stored in the sensor counter register. For details on the detection principle, refer to the application note "Capacitive Sensor Microcontrollers CTSU Capacitive Touch Introduction Guide."

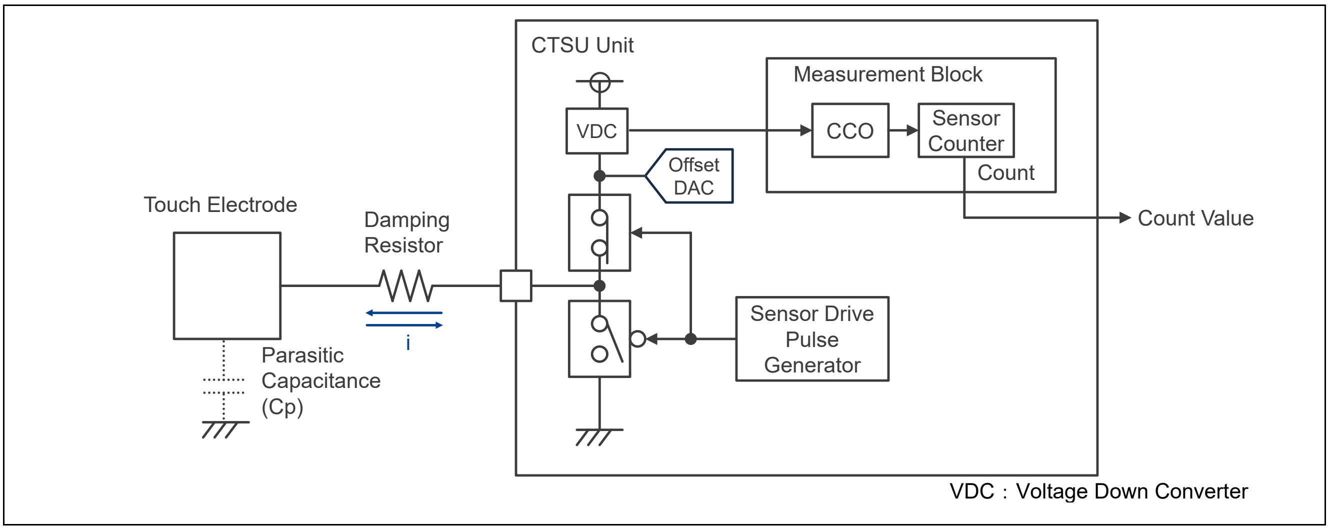


Figure2-4. Internal Configuration Overview of Self-capacitance CTSU

Figure2-5 shows an image of CTSU measurement. When one cycle of the sensor drive pulse frequency is shorter than the C charge/discharge time and the charge/discharge is insufficient, not enough current flows to C and the count value is smaller than the ideal value. In this situation, you can lengthen the charge/discharge time of 1 cycle by lowering the sensor drive pulse frequency; this will result in sufficient charge/discharge even for hardware with large parasitic capacitance. However, when lowering the sensor drive pulse frequency, the charge/discharge count (number of measurements) per unit time also decreases, resulting in a smaller measurement value.

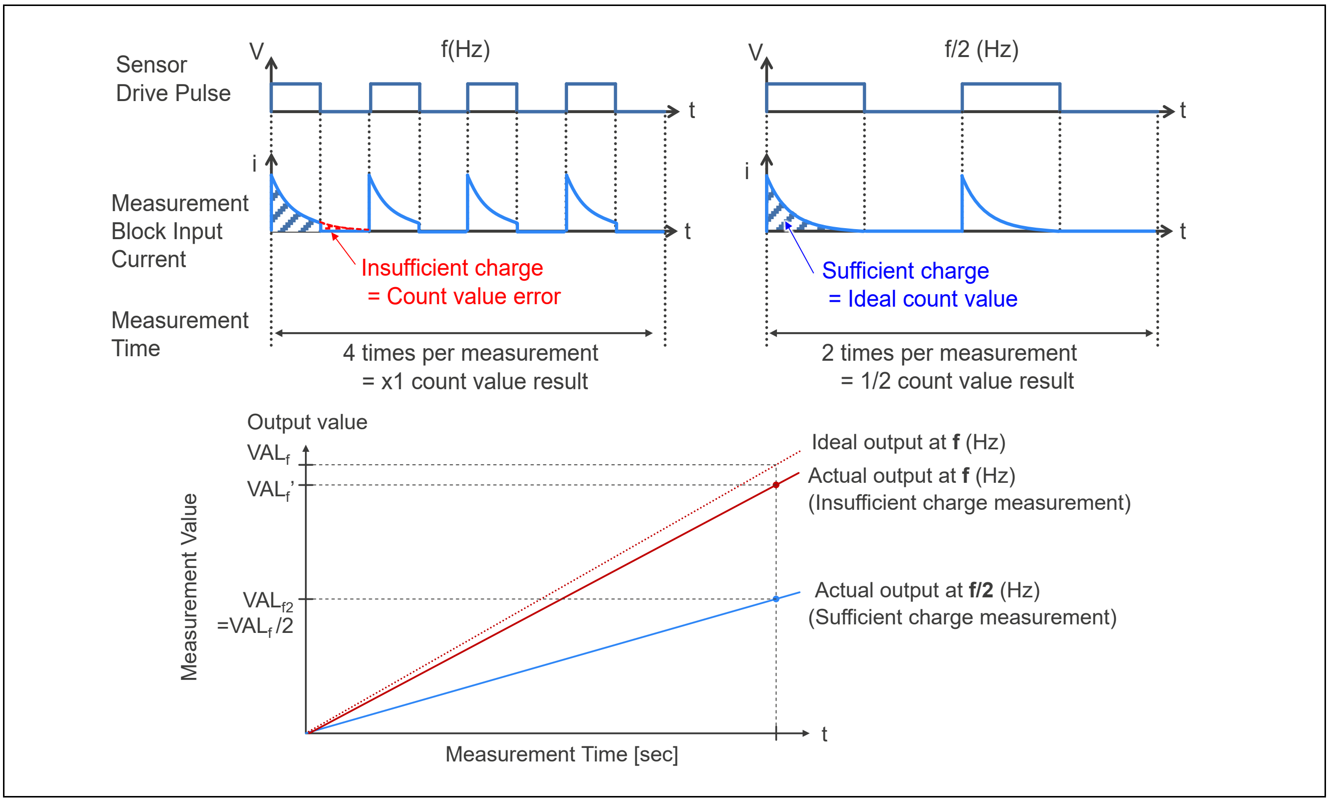
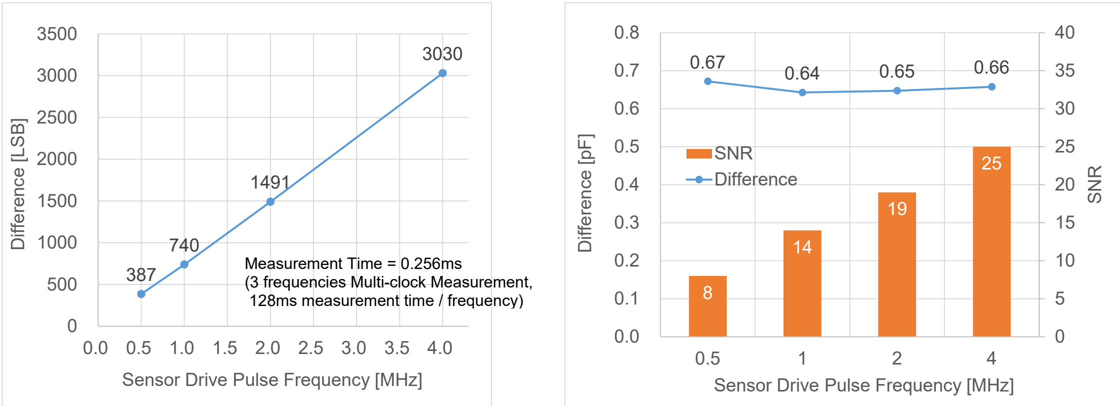


Figure2-5. Image of CTSU Measurement

Figure2-6 shows the relationship of sensor drive pulse frequency and sensitivity. Figure2-6 (a) shows the measured difference between touch ON and OFF for each sensor drive pulse frequency, which is proportional to the sensor drive pulse frequency. In the same manner as the detected capacitance at touch (Signal Value [pF]) shown in Figure2-6 (b), when the measured value is converted to a capacitance value, it remains constant regardless of sensor drive pulse frequency. On the other hand, the SNR improves in proportion to the sensor drive pulse frequency. The lower the sensor drive pulse frequency, the higher the amount of noise per count, and the SNR tends to decrease. Accordingly, to achieve highly sensitive buttons, set the parasitic capacitance of the electrode circuit to low in the hardware design stage, allowing selection of a high sensor drive pulse frequency.



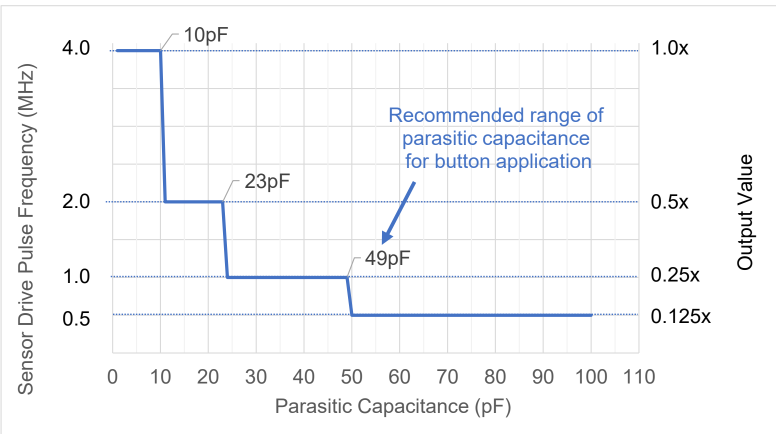
(a)Sensor drive pulse frequency and measured values

(b)Detected capacitance and SNR at touch

Figure2-6. Relationship of Sensor Drive Pulse Frequency and Sensitivity

Note: The following instructions apply only if you are using QE for Capacitive Touch V4.1.0 or earlier.
The sensor drive pulse frequency of the CTSU affects both the capacitance measurement range as well as the SNR. Figure2-7 shows a . Setting Example for Parasitic Capacitance and Sensor Drive Pulse Frequency. The conditions for this example are as follows: the MCU is RA2L1, supply voltage (VCC) is 5.0V, and damping resistance value is R=560Ω. Damping resistance value of 560Ω is recommended to protect the pins from external noise and limit the output current from pins. The QE for Capacitive Touch auto-tuning function selects the sensor drive pulse frequency from 4.0, 2.0, 1.0, and 0.5 MHz. The setting values differ according to the MCU and hardware design used.

For self-capacitance method button applications, when using RA2L1, the recommended range of parasitic capacitance for button electrodes, including the overlay panel and MCU pins, is up to 49pF.-The recommended range is that the sensor drive pulse frequency is set to 1MHz or more by the automatic adjustment of QE for Capacitive Touch so that the sensitivity of the button can be obtained sufficiently. For TS pin conditions other than the recommended values that valid range and deprecated range, refer to "4.2 Base Clock Frequency/Sensor Drive Pulse Frequency Settings." If the range exceeds the recommended range, the drive pulse frequency will be lower, which may result in insufficient SNR.



Conditions:
MCU = RA2L1, Vcc = 5.0V,
R = 560Ω

Note:
The frequency range may differ according to the MCU and hardware design used.

Figure2-7. Setting Example for Parasitic Capacitance and Sensor Drive Pulse Frequency

Note: The following instructions apply only if you are using QE for Capacitive Touch V4.2.0 or later.
The auto-adjustment function in QE for Capacitive Touch V4.2.0 or later improves the setting resolution for the sensor drive pulse frequency exclusively on CTSU2-embedded MCU. The upper limit of the optimal sensor drive pulse frequency is determined by the combination of parasitic capacitance and damping resistor. Refer to the section for QE for Capacitive Touch V4.2.0 or later in “4.2 Base Clock Frequency/Sensor Drive Pulse Frequency Settings” for the relationship between the recommended values for CTSU2's parasitic capacitance and damping resistor and the sensor drive pulse frequency. For microcontrollers equipped with CTSU1, the sensor drive pulse frequency varies depending on the parasitic capacitance, damping resistor, and CTSU operating clock (PCLKB or f_{CLK}). For the relationship between the recommended values for CTSU1 parasitic capacitance and damping resistor and the sensor drive pulse frequency, refer to the entries for QE for Capacitive Touch V4.1.0 or earlier in the “4.2 Base Clock Frequency/Sensor Drive Pulse Frequency Settings”.

If the parasitic capacitance cannot be reduced due to hardware restrictions, causing the sensor drive pulse frequency to be low and the sensitivity insufficient, the sensitivity can be enhanced by increasing the measurement count/measurement time in the advanced mode settings of QE for Capacitive Touch. However, this may cause an increase in the time required to complete the measurement or an overflow of the measurement value. For details regarding how to adjust the measurement count/measurement time, see Capacitive Sensor MCU QE for Capacitive Touch Advanced Mode Parameter Guide.

2.4 Electrode Pattern Design

2.4.1 Electrode circuit configuration

Figure2-8 shows a self-capacitance electrode circuit. The configuration of the touch electrode circuit that connects to the TS pin comprises the touch electrode, electrode wiring, and damping resistor. The touch electrodes and wiring are created using patterns on the printed circuit board. The reference value of the damping resistor is 560Ω. Place the damping resistor as close as possible to the TS pin to prevent noise mixing in from the wiring between the TS pin and the resistor.

When designing a self-capacitive touch electrode circuit, design the pattern and select the materials so that the following recommended conditions are met.

① Parasitic capacity C: See Table 2-1 and Table 2-2.
② Resistance value R: 560Ω to 1kΩ (including damping resistor)

Keep in mind that the electrostatic capacitance C of the entire electrode circuit also includes parasitic capacitance with objects around the board, such as the board’s GND pattern, the overlay panel, and the body chassis. By keeping C low in the design, the touch ON/OFF measurement value difference (signal value) will increase, and the SNR will improve when selecting a high frequency for the CTSU sensor drive pulse frequency. The total capacitance for each TS pin can be confirmed using QE for Capacitive Touch.

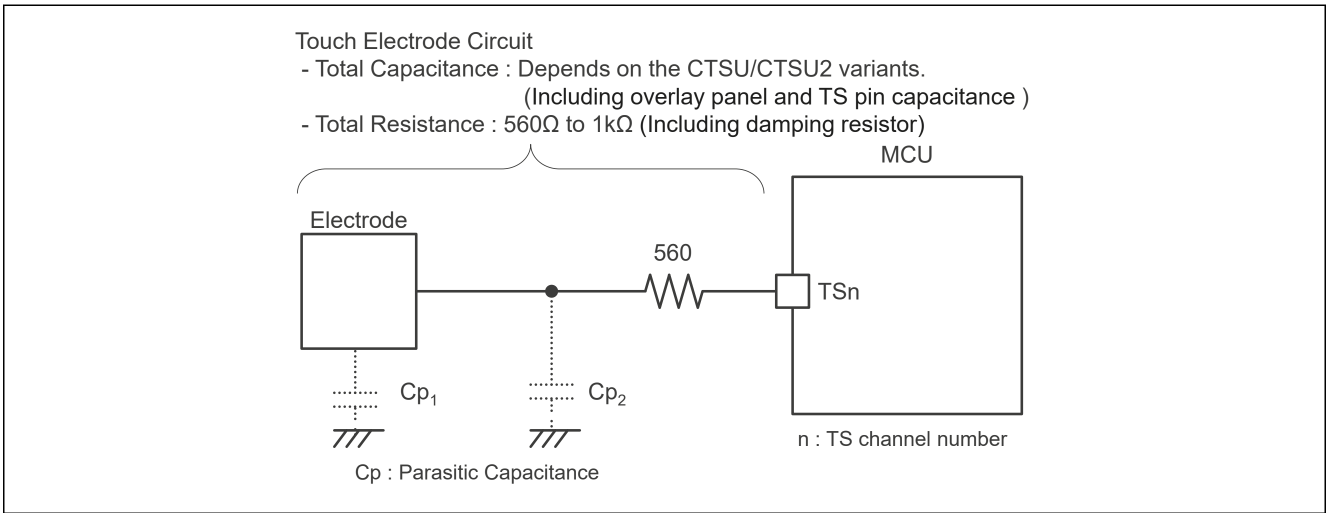


Figure2-8. Self-capacitance Method Electrode Circuit

2.4.2 Electrode pads and wiring

The following offers recommended shapes for button electrodes and wiring conditions.

- Shape: square or circular plane patterns
- Size: 10 x 10 to 15 x 15mm
- Electrode interval: To avoid crosstalk(Note), use an interval wide enough to prevent simultaneous response by adjacent electrodes based on finger or other touch interface
  Target interval size: electrode button size x 0.8 or more
- Interval between electrode and GND pattern: 5mm or more
- Do not place wiring or a pattern for another function, or a GND plane pattern, directly under an electrode. Noise emitted from wiring directly under the electrode can cause the electrode potential to fluctuate, which can affect the CTSU measurement value. A solid GND pattern tends to increase parasitic capacitance, which may exceed the measurement range of the CTSU. When a GND pattern is necessary as an anti-noise countermeasure, place a cross-hatched GND pattern.

Note: Crosstalk refers to capacitive coupling between adjacent electrodes or capacitive coupling between a finger and adjacent electrodes when the target electrode is touched. For more details, see section “2.6 Effect of Panel Thickness.”

Figure2-9 shows the recommended electrode shapes and size. Shapes and sizes are fairly flexible and can be determined based on the button design of the panel on the final product. Make sure that the size is not extremely large or extremely small with respect to the part of the human body (finger, etc.) that will be operating the product. If the size is extremely large the parasitic capacitance will increase, requiring a lower CTSU sensor drive pulse frequency setting which may in turn reduce button sensitivity. If the size is extremely small, the contact area between the finger and the electrode pad will be limited, which will reduce the change in capacitance and may prevent touch detection. If the pad is square, round the corners of the electrode with a radius of 0.5 to 1.0 mm to reduce the effects of noise.

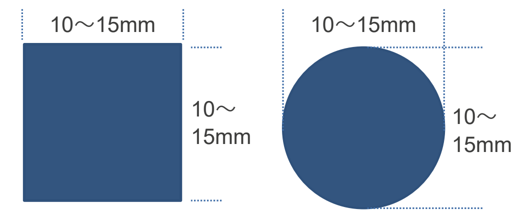


Figure2-9. Recommended Electrode Shapes and Size

Figure2-10 shows shapes that are not recommended for electrodes—triangles with angles of 90 degrees or less and E-shapes with narrow line width and long total length. These shapes are not recommended as they tend to perform as antennas and degrade the RF noise immunity.

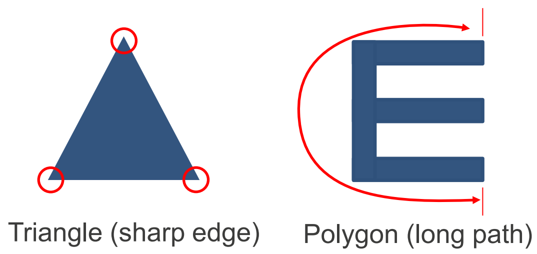


Figure2-10. Unsuitable Electrode Shapes

2.4.3 Wiring

Recommended layout and dimensions of wiring are listed below.

- Wiring width: 0.15mm (the thinnest wire achievable through mass production)
- Wiring spacing: 1.27mm pitch
  However, leave at least 5mm, more if possible, around the electrode pad circumference (about twice the length of the electrode pad)
- Cross-hatched GND pattern width: 5mm
- Wiring and cross-hatched GND pattern spacing: 3.0mm
- Wiring and GND pattern spacing: 3mm or more (when not using a cross-hatched GND shield)

Make sure the design satisfies the following wiring requirements as well.

- Keep the wiring as short as possible, as parasitic capacitance increases in proportion to the wiring length. In addition, The longer the wiring length, the more susceptible it is to external noise. Keep this in mind when planning to use the device in environments with RF frequency noise.
- Try to have as few corners in the wiring as possible; make corners 45 degrees or rounded. This reduces noise radiated from the wiring.
- Drill vias at the edge of the electrode pad and layout wiring on the back side. This helps reduce malfunctions when wires are touched. However, keep the number of vias at a minimum as they tend to increase parasitic capacitance.
- As an anti-noise countermeasure, place a cross-hatched GND pattern directly under (the back layer of wiring) the electrode and wiring.
- The wire routing extending from the electrode is vulnerable to noise as there is no cross-hatched GND pattern directly under the wiring. Bring the cross-hatched GND as close as 0.5mm to this part.
- Do not place wiring other than that used for the touch function directly under the electrode wiring. If you must do so, make the wiring orthogonal and minimize the facing area. This reduces the effects of noise caused by capacitive coupling between wires.

The wiring part of the electrode has a small parasitic capacitance and is easily affected by external noise. Noise immunity can be improved by suitably arranging the GND shield. In addition, since the non-measurement TS pins of the CTSU are fixed to the GND level, the wiring connected to the TS pins also functions as a shield(Note). the GND shield to the wiring and the shorter the distance between the wiring of each TS pin, the greater the parasitic capacitance of the TS pins, the greater the parasitic capacitance of the TS pins. Therefore, adjust the GND shield placement and wiring spacing so that total parasitic capacitance conditions are satisfied.

Note: Applies if you are using the CTSU or if the Active Shield function of the CTSU2 is disabled.

Figure2-11 shows an example of the wiring section of a double-layer board layout example.

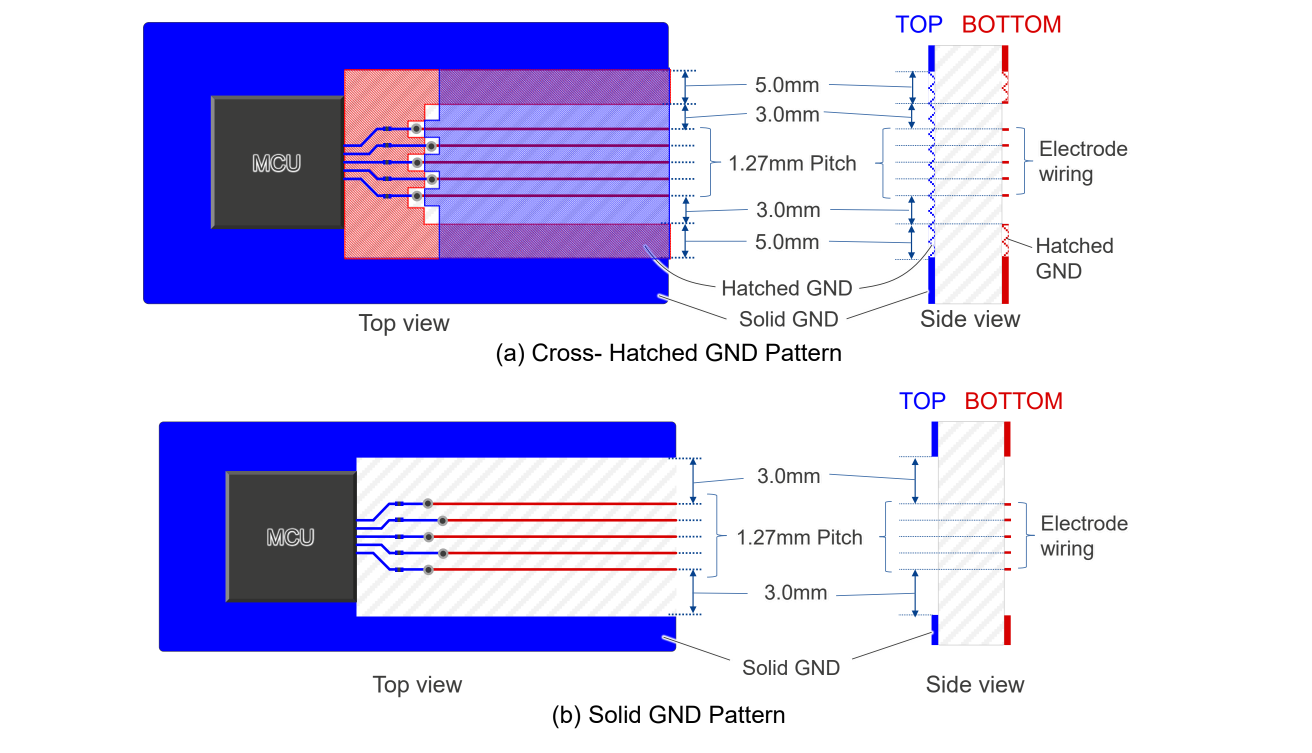


Figure2-11. Double-Layer Board Layout Example (wiring section)

Figure2-12 shows an example of the electrode section of a double-layer board layout.

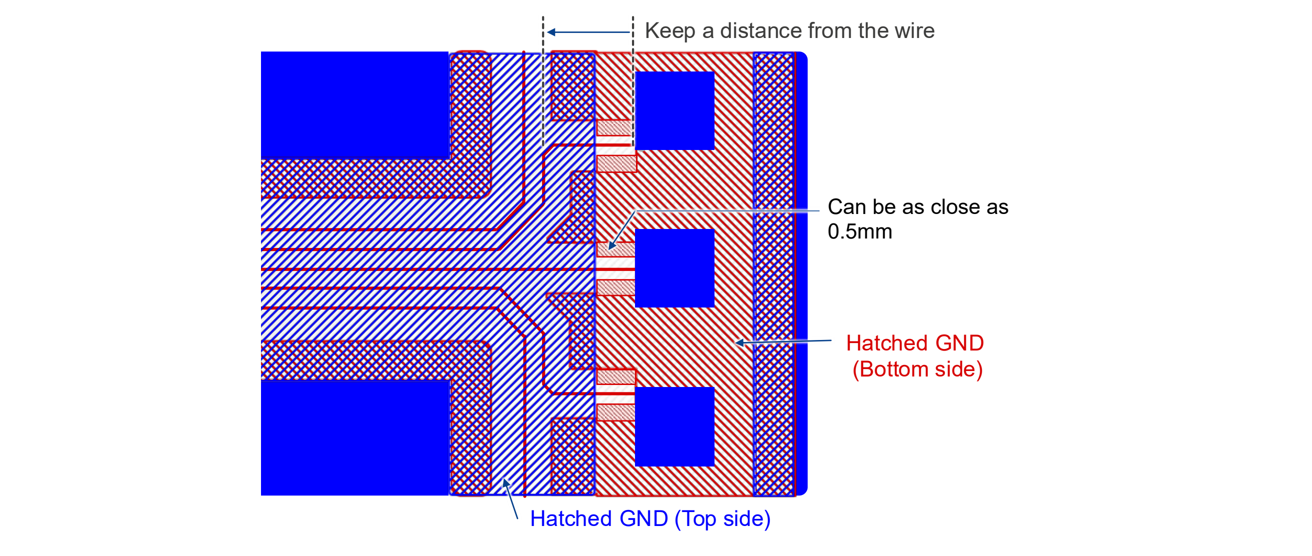


Figure2-12. Double-Layer Board Layout Example (electrode section)

Figure2-13 and Figure2-14 show layout examples for each layer.

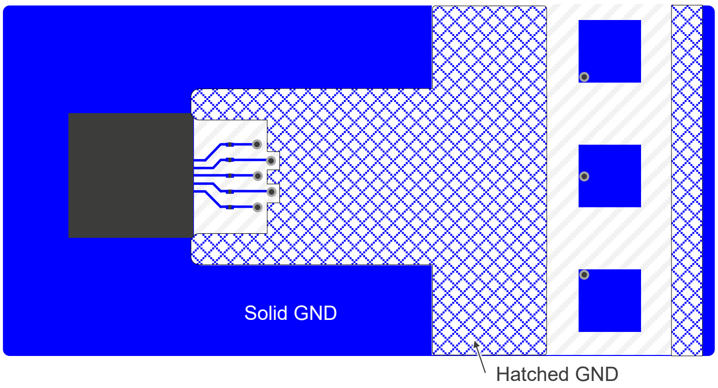


Figure2-13. Top Layer Layout Example

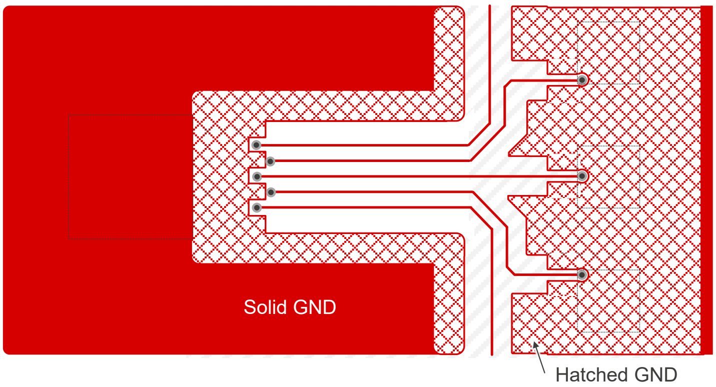


Figure2-14. Bottom Layer Layout Example

Figure2-15 shows an example of high-density wiring. When you have limited board size and need to increase the wiring density, shift the wiring by a half pitch and lay out the wiring on both sides of the board. For 4-layer boards, make sure to place a cross-hatched GND on the inner layers.

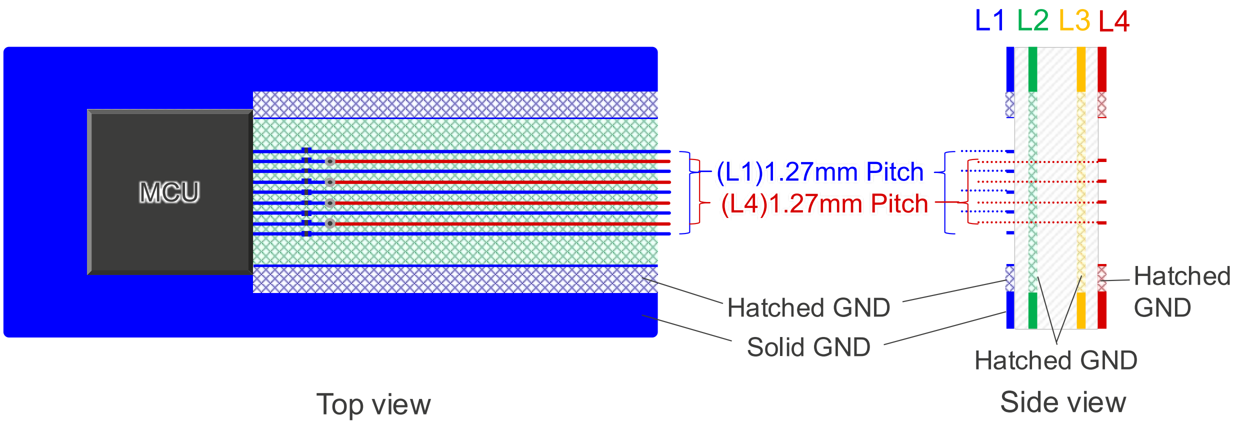


Figure2-15. High-density Wiring

2.5 Anti-Noise Layout Pattern Designs

The electrode circuit configuration allows the circuit to act as an antenna (the MCU pin is open only for capacitive coupling) and makes it vulnerable to electromagnetic field noise. Renesas Touch MCUs employ several anti-noise countermeasures to ensure high noise immunity. However, an MCU alone cannot prevent influence from all noise. Hardware countermeasures are indispensable when using the MCU in a severe noise environment. The following are a few examples of how to protect the system from external noise.

In general, the longer the wiring length, the more susceptible it is to external noise. Make sure the wiring between button electrodes and the touch MCU is kept as short as possible.

The CTSU2-embedded MCU is equipped with an active shield function that drives a shield at the same potential and in the same phase as the touch electrode circuit. In this section, the shield at the GND level is described as a “GND shield” to distinguish it from an active shield.

For details regarding anti-noise measurements for the IEC61000 series, see Capacitive Sensor MCU Capacitive Touch Noise Immunity Guide.

2.5.1 Shield pattern

2.5.1.1 Shield design

To prevent touch button malfunctions caused by external noise, place a GND level shield around the touch button and wiring. Placing a GND shield around the touch electrode circuit releases external noise to GND from the path created by the capacitive coupling, stabilizing the potential of the touch electrode circuit and reducing the effect of noise appearing in the CTSU measurement value. We recommend a hatched-pattern shield to reduce the increase in parasitic capacitance of the electrode pattern. Figure2-16 shows an image of GND patterns and parasitic capacitance. When using a printed board, place a GND plane pattern directly under the wiring pattern as a general anti-noise countermeasure. In the self-capacitance button, the parasitic capacitance Cp_{GND} generated by the electrode and GND plane pattern is much larger than Cf and exceeds the measurement range of the CTSU. So, when designing the self-capacitance button, do not place a GND plane pattern directly under the electrode. If an anti-noise countermeasure is needed, use a cross-hatched GND pattern to reduce the increase in parasitic capacitance.

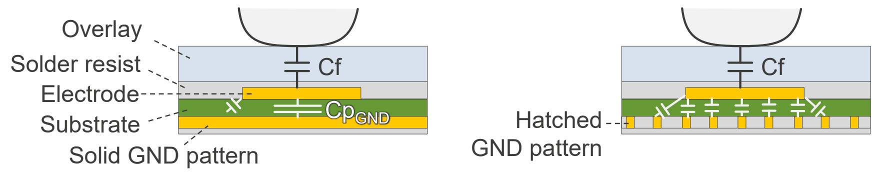


Figure2-16. Image of GND Pattern and Parasitic Capacitance

Figure 2-17 shows the cross-hatched pattern dimensions. Shielding the electrode and electrode wiring serves as an effective EMC noise countermeasure. A shield guard can be placed directly under the electrode or electrode wiring on a multi-layer board but the GND plane pattern has a large coupling capacity which will prevent the electrode from detecting capacitance fluctuation when touched. Therefore, a cross-hatched pattern shield-should be used. Reducing the pitch and wiring spacing from the recommended dimensions will improve noise immunity but keep in mind that the parasitic capacitance of the electrode circuit will increase as the GND pattern ratio per unit area increases. In addition, the cross-hatched pattern is tilted 45 degrees depending on the wiring direction in order to reduce the capacitive coupling with the electrode wiring.

Item	Dimension
Pitch	1.5 mm
Line Width	0.15 mm
Line Space	1.35 mm

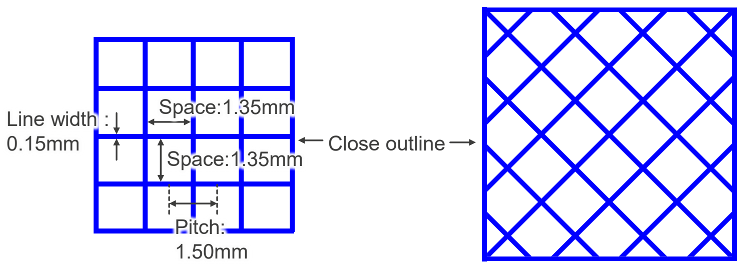


Figure 2-17. Cross-hatched Pattern Dimensions

2.5.1.2 GND shield

The GND shield is a noise countermeasure that can be achieved with the board pattern, and the GND shield should generally be located as close as possible to the digital signal line. When designing a capacitive touch button, the closer the GND shield is to the touch electrode circuit, the higher the parasitic capacitance. In this case, it is necessary to set the sensor drive pulse frequency of the CTSU to a lower value, which reduces the sensitivity of the button. Also, in board designs with long wiring, the longer the parallel run distance between the electrode circuit wiring and the GND shield, the higher the parasitic capacitance. Careful consideration is required for placement spacing throughout the entire pattern.

The following are recommended shape and wiring conditions for the top layer. These recommendations assume the electrode pads are placed on the top layer.

① Board layer configuration: 2 or more layers to block external noise
② Pattern shape: cross-hatched pattern
See 2.5.1.1 Shield design for dimensions.
③ Distance between touch electrode and cross-hatched GND shield: 5mm
④ Distance between touch electrode wiring and cross-hatched GND shield: 3mm
⑤ Width of cross-hatched GND shield: 5mm or more
Make sure to connect the cross-hatched GND pattern and GND plane.
Cover the area directly under the electrode and wiring with the cross-hatched GND pattern.

Figure2-18 and Figure2-19 show an example of a GND shield pattern for a multi-layer board.

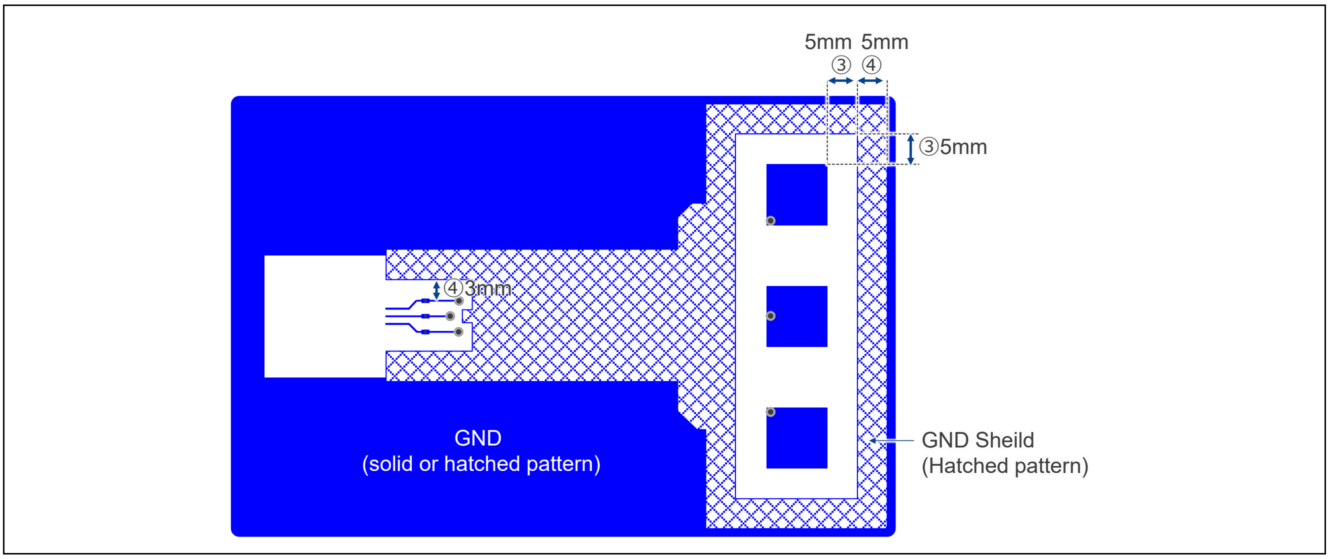


Figure2-18. GND Shield Pattern Example for Multi-layer Board (top layer)

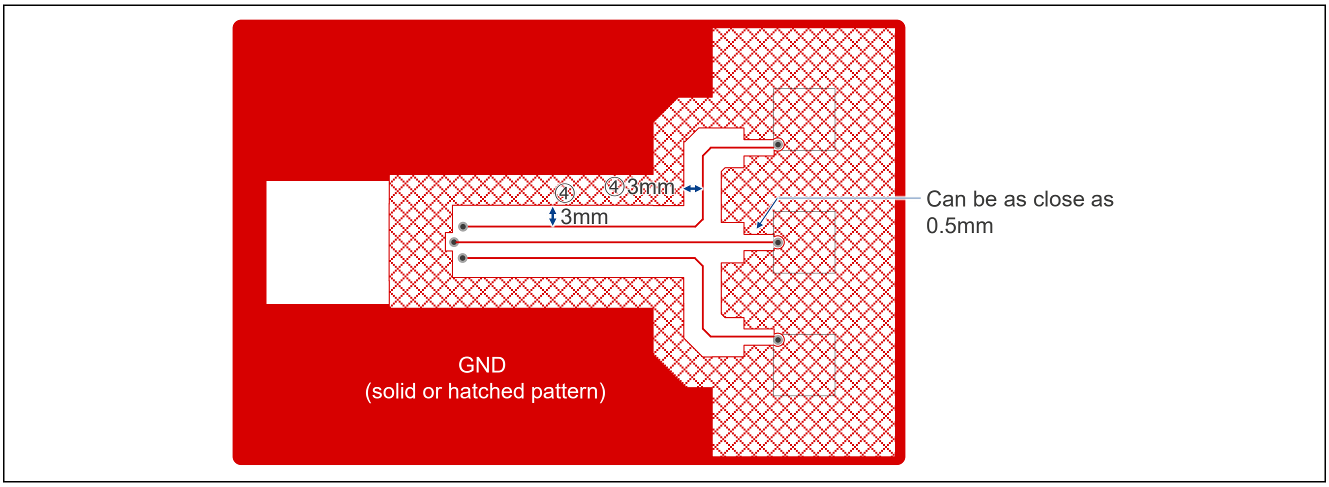


Figure2-19. GND Shield Pattern Example for Multi-layer Board (bottom layer)

2.5.1.3 Active Shield (CTSU2 function)

This function is provided for MCUs embedded with CTSU2.

The active shield function drives the shield with signals of the same potential and phase as the electrodes. Using the active shield will reduce capacitance coupling between the electrode and shield guard as well reduce noise interference. This is mainly used to improve the water resistance of touch buttons.

Figure2-20 shows an image of how an active shield reduces the effects of parasitic capacitance. The figure shows a water droplet adheres to the overlay panel during touch measurement, forming a conductive bridge between the touch electrode and the shield pattern. Parasitic capacitance Cp occurs between the touch electrode and the shield, and when water adheres to it, a new parasitic capacitance indicated by Cpw occurs. The relative dielectric constant of water is 80 times that of air, so if Cp is 1pF, a simple calculation gives a parasitic capacitance of Cpw as 80pF. When the touch button is pressed with a finger, the change in capacitance is approximately 1pF, depending on the hardware conditions.

In the figure, (a) shows an example using a GND shield. During touch measurement, the potential difference between the touch electrode and the shield is the sensor drive pulse voltage Vd, and Cp and Cpw are charged. Since the charging current of Cpw is also added to the CTSU measurement value, the value may exceed the touch threshold and falsely detect touch ON.

Example (b) shows use of an active shield. Since the same voltage Vd as the touch electrode is applied to the active shield, both ends of Cp and Cpw are at the same potential and are not charged. Therefore, the CTSU measurement value does not change from the state where a drop of water is adhered to the electrode, and the touch OFF state is continually detected.

Example (c) shows the touch button pressed under the same conditions as in (b). However, since the finger is connected to GND, its parasitic capacitance Cf causes a potential difference on the touch electrode, resulting in it being charged. As Cp and Cpw are not charged, the CTSU detects only the change in Cf, enabling touch detection (touch ON) even when water is adhered to the button

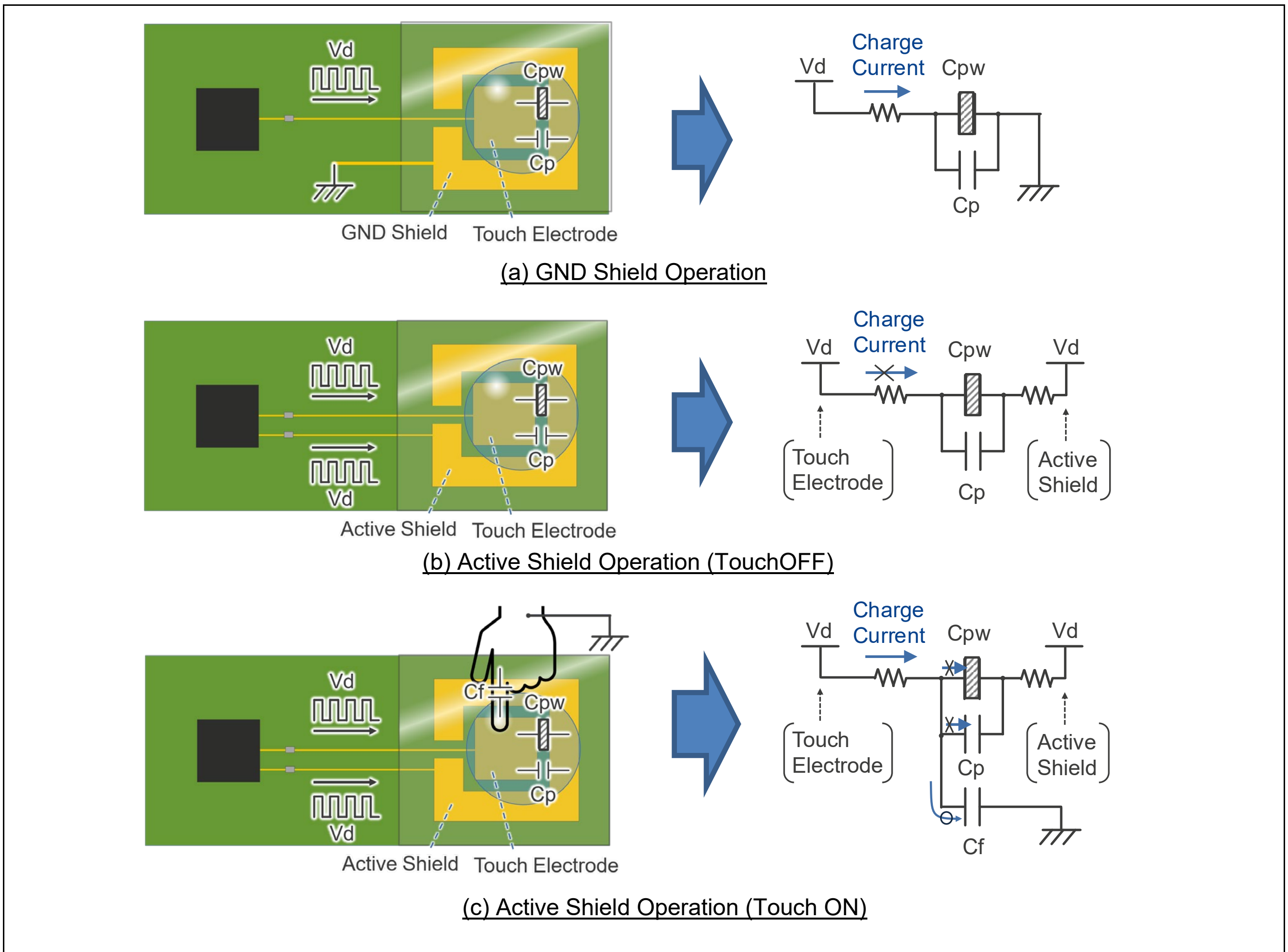


Figure2-20. Image of How an Active Shield Reduces the Effects of Parasitic Capacitance

Figure2-21 shows an example of a shield electrode circuit. The active shield is connected to the TS pin, in the same manner as a touch electrode. Since one shield pin can be combined with multiple TS pins of button electrodes, design the shield pattern by grouping the button electrodes that you want to apply the active shield.

The active shield is driven by the sensor drive pulse in the same way as the touch electrode. When designing the circuit, be aware that a significant difference between the parasitic capacitance of the shield pattern and that of the touch electrode can cause a phase shift in the sensor drive pulse, reducing its effectiveness. We recommend keeping the total parasitic capacitance of the TS pin connecting the shield pattern at 49pF or less. As the number of button electrodes increases, the area of the shield pattern will increase, as will the parasitic capacitance. The shield pattern should be designed as a cross-hatched pattern to suppress parasitic capacitance. See 2.5.1.1 Shield design for recommended cross-hatched dimensions.

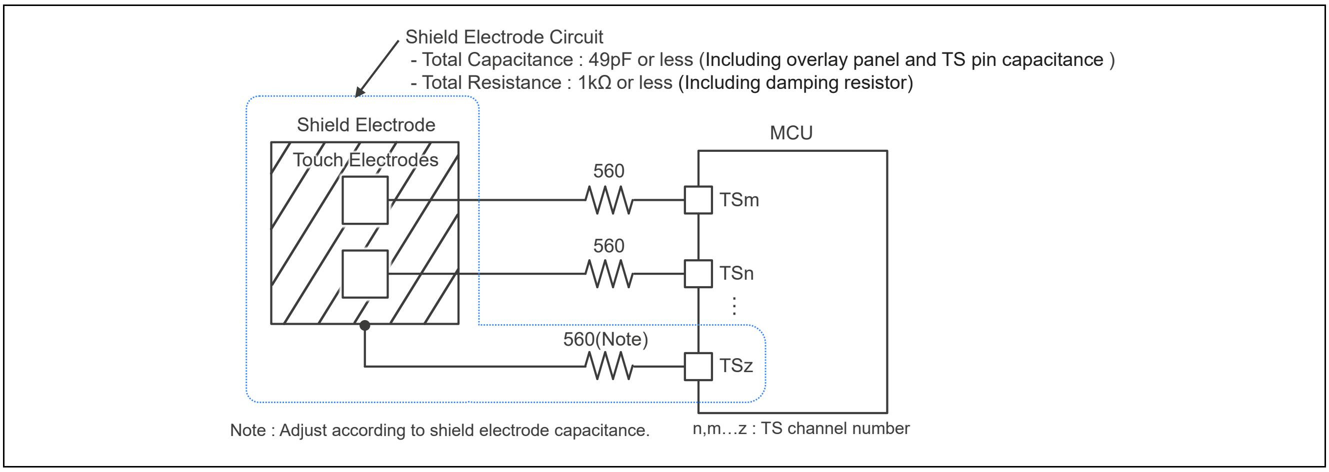


Figure2-21. Shield Electrode Circuit

If the circuit hosts many button electrodes and the parasitic capacitance per shield pattern is large, the parasitic capacitance can be reduced by dividing the button electrodes and active shields into groups. Note that when grouping electrodes and shields, the groups that are not being measured are fixed to low output. Therefore, if the measurement group and the non-measurement group are close to each other, parasitic capacitance charging/discharging may occur between electrode groups, which may affect the measurement value. In particular, false reactions can be caused by water adherence, so when considering water resistance and usage environments, be sure to separate electrode groups far enough apart so they will not be bridged by water.

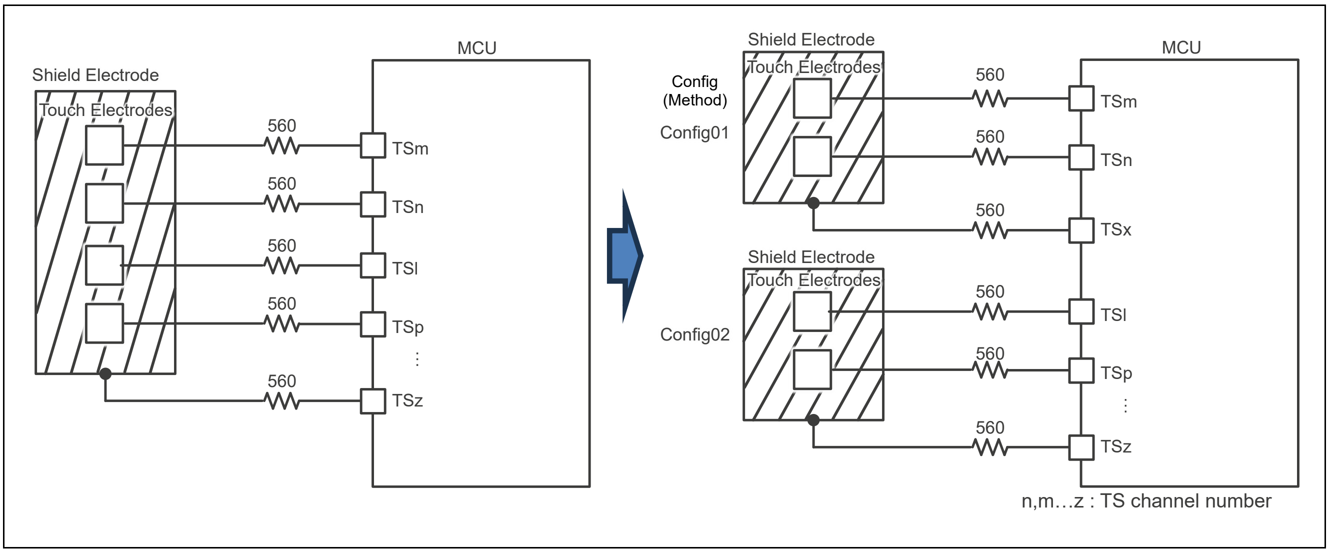


Figure 2-22. Example of Dividing of Shielded Electrode Circuits

QE for Capacitive Touch supports up to 8 groupings (configuration (method)). For details on the configuration (method), refer to the help file of QE for Capacitive Touch. As a guideline, grouping should be 4 buttons or less per active shield pin (assuming the active shield pin damping resistance is 560Ω and the button size is 10 mm square). For more than 4 buttons, consider dividing the grouping again to avoid exceeding 49pF. Refer to section 5.3.5.1 Active Shield Area for reference values of parasitic capacitance changes due to number of buttons and active shield area.

Table 2-3shows the recommended designs for active shield electrodes. The items listed below assume the electrode pads are placed on the TOP layer. For design items not listed in the table, refer to section 2.1 Outline of Design Recommendations.

Table 2-3 Design Recommendations for Active Shield Electrodes

No	**Design Parameter**	**Recommended Value**	**Cautions**
①	Board layer	2 layers	To prevent noise, cover the area directly below electrodes and wiring with active shield electrodes Single-sided boards offer less noise immunity because shields cannot be placed directly under electrodes. When using 3 or more layers: See Note 1
-	**Space around touch electrodes**		
②	Pattern shape	Cross-hatched pattern	For dimensions, see 2.5.1.1 Shield design For solid pattern: Note 2
③	Pattern width	3.0mm	For wider width: Note 2 For narrower width: Note 3
④	Interval between touch electrode pads	3.0mm	For wider interval: Note 3 For narrower interval: Note 2
⑤	Spacing between shield pattern and solid GND	3.0mm	For wider spacing: Note 3 For narrower spacing: Note 2
-	**Space around wiring**		
⑥	Pattern width (shield pattern adjacent to touch electrode wiring)	0.5mm	Use 0.5mm wiring For wider width: Note 2 For narrower width: Note 3
⑦	Touch electrode wiring spacing	1.27mm	For wider interval: Note 3 For narrower interval: Note 2
⑧	Touch electrode wiring spacing (near touch electrode pad)	0.3mm	Use this to improve shielding in the gap between the electrode pad and the shield pattern. If the distance is about the width of the shield pattern, the effect on parasitic capacitance is negligible. If the distance between narrow spacing is long: Note 2
-	**Common parameters**		
⑨	Spacing between shield pattern and solid GND	3.0mm	For wider spacing: Note 3 For narrower spacing: Note 2
⑩	Total capacitance	49pF or less (including overlay panel and TS pin capacitance)	If parasitic capacitance or total resistance exceeds recommended values, see section 4.2 Base Clock Frequency/Sensor Drive Pulse Frequency Settings and consider changing the design settings so that the both values satisfy the measurable sensor drive pulse frequency.
⑪	Total resistance	560Ω to 1kΩ (including damping resistor)	

Note 1: Place the shield pattern on the top and bottom layers and do not place other patterns on the inner layers.

Note 2: Parasitic capacitance may increase, potentially breaching the CTSU sensor drive pulse lower limit.

Note 3: This may cause a decrease in noise immunity.

Figure2-23 and Figure2-24 show an example of the active shield pattern for multiple-layer boards. For board configurations with more than two layers, do not place other patterns on the inner layers within area ⑥ as the CTSU measurement values may be affected by noise.

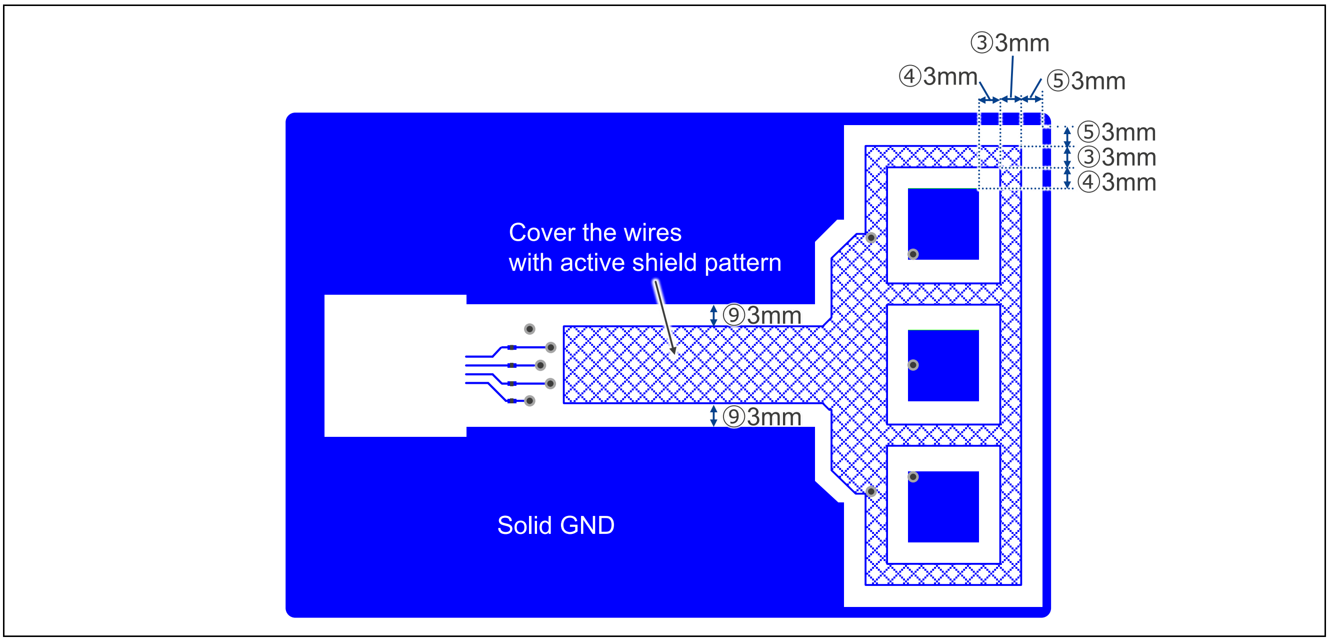


Figure2-23. Example of Active Shield Pattern for Multiple-Layer Board (top layer)

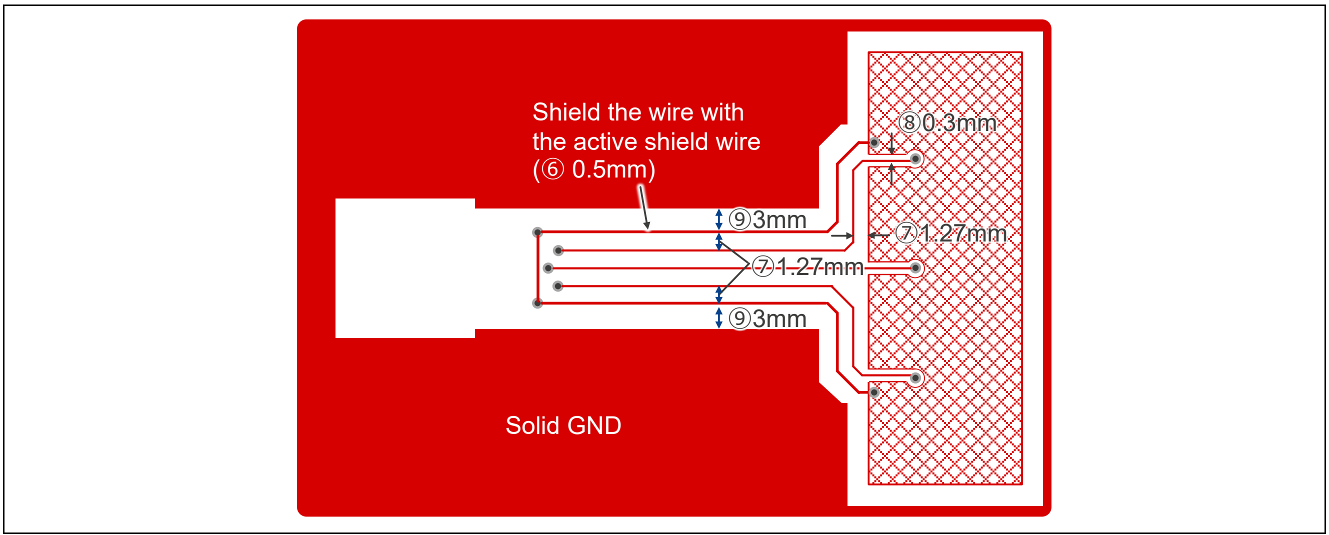


Figure2-24. Example of Active Shield Pattern for Multiple-Layer Board (bottom layer)

2.6 Effect of Panel Thickness

The self-capacitance method detects the capacitance generated when there is contact between the human body and a button electrode, where the relationship of capacitance is $C = \varepsilon\frac{S}{d}$. In touch detection using the self-capacitance method, the capacitance of the parallel plate capacitor formed between the human body and the button electrode is detected, based on the relationship of capacitance C=ε S/d. Therefore, the larger the area (S) of the button electrode and part of the human body facing each other, and the smaller the distance (d) between them, the greater the capacitance when the panel is touched. This increase in capacitance enhances the sensitivity of touch ON-OFF detection. As the maximum touch surface size of the button electrode is limited (10mm to 15mm), the distance, or panel thickness, is the key factor in adjusting sensitivity.

2.6.1 Relationship of panel thickness and touch sensitivity

Figure2-25 shows the relationship of the amount of capacitance change and sensitivity distance in the self-capacitance method. This diagram uses an overlay panel with a dielectric constant of 2.4 (acrylic), and the capacitance is standardized to 1.00 when touching an overlay panel with a thickness of 2.0 mm. This shows that, if the sizes of the finger and button electrode are constant, the thinner the overlay panel, the greater the capacitance when touched. Since the CTSU has an upper limit (measurement range) for capacitance measurement, there is a limit to how thin the overlay panel can be. Renesas assumes the use of an overlay panel with a thickness of 2 to 3 mm. If a material with a relative dielectric constant of 4.5 (glass) is used as the overlay panel material, the capacitance increases by 1.88 times even at the same thickness, and if the relative dielectric constant is 1.0 (air), the capacitance decreases to 0.42 times. The capacitance at touch also increases or decreases depending on the dielectric constant of the panel material. Note that, even with the same distance (panel thickness), materials with a high dielectric constant may exceed the CTSU measurement range. To use a material with a high dielectric constant for the overlay panel, you can avoid exceeding the CTSU measurement range by reducing the material thickness or by intentionally inserting an air gap or spacer with a low dielectric constant between the overlay panel and the touch electrode pattern, which will lower the composite value of the dielectric constant. To increase the sensitivity of the touch buttons, try using a material with a higher dielectric constant, or fix the overlay panel and touch electrode pattern with double-sided tape or resin to eliminate the air gap.

In this method, the capacitance increases or decreases depending on the distance between the finger and the electrode, allowing touch detection over a broad range (distance) by adjusting the touch threshold. However, if the touch threshold is set too low compared to the capacitance change, touch detection may occur before the finger actually has contact with the panel.

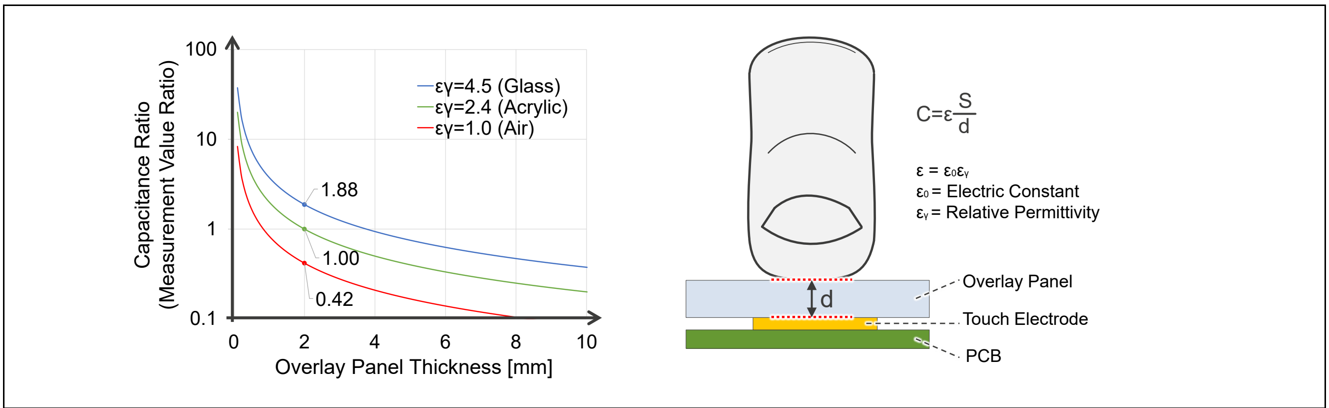


Figure2-25. Relationship of Capacitance Change and Sensitivity Distance

Table 2-4. Relative Permittivity of Each Material

Dielectric Material	Dielectric constant ε
Acrylic	2.4-4.5
Glass	4.5-7.5
Nylon Plastic	3.0-5.0
Flexible Vinyl Film	3.2
Air	1.0
Water	80

2.6.2 Relationship of panel thickness and crosstalk

Figure2-26 shows the relationship of the inter-electrode distance and panel thickness in the self-capacitance method. If the button electrodes are placed too close together, they may cause neighboring button electrodes to turn ON erroneously (left side of figure). To prevent false detections (crosstalk), among neighboring button electrodes by changing the overlay panel thickness from 2 to 3mm, the recommended distance between button electrodes is 0.8 times wider than the button size.

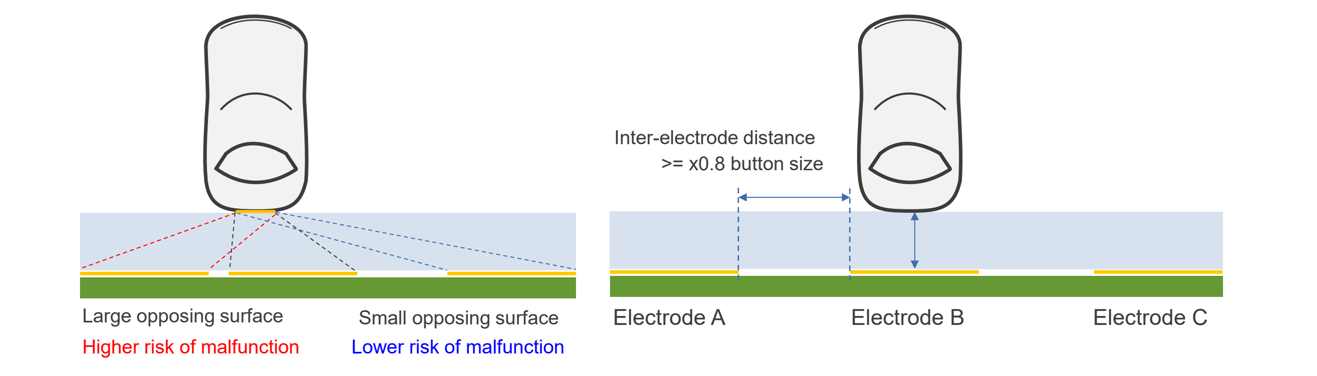


Figure2-26. Relationship of Inter-electrode Distance and Overlay Panel Thickness for Self-capacitance Method

When keeping the inter-electrode distance at 0.8 times the touch electrode size or less, you can reduce the effects of crosstalk by considering the overlay panel thickness, electrode size, and the tolerance for touch position misalignment.

Figure 2-27 shows the relationship between inter-electrode distance and the risk of crosstalk. In the figure, (a) is the distance from the finger to the center of the touch electrode to be pressed, and (b) is the distance to the center of the adjacent touch electrode. Even if the finger's touch position is slightly offset from the target touch electrode, the target button still detects the touch ON state. If thickness (d) of the overlay panel remains constant, a shorter inter-electrode distance makes point (b) closer to point (a). This increases The capacitance of the adjacent touch electrode, making a touch ON state more likely to be detected. In addition, when the touch ON threshold value is close to the CTSU measurement value of an adjacent touch electrode, there is a higher possibility that external noise may cause fluctuations in the measurement value, resulting in false detections.

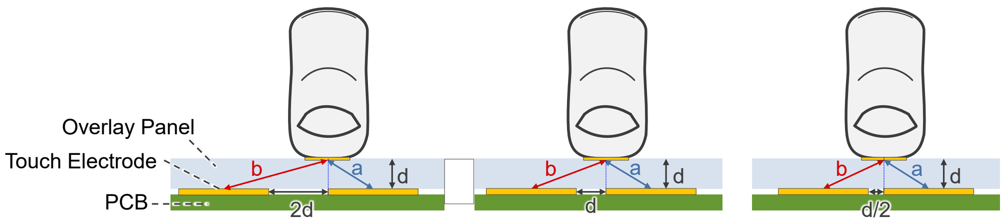


Figure 2-27. Changes in Distance between Electrodes and Finger to Touch Electrode

In addition, due to design differences such as the wiring length of the touch electrode circuit, the sensor drive pulse frequency for each electrode differs and the sensitivity varies, or if an overlay panel with a high dielectric constant is used, or if the electrode size is large and the capacitive coupling with the finger through the air is large, crosstalk is likely to occur. In all these cases, sufficient electrode spacing can be used to prevent problems.

2.7 Electrode Application Examples

2.7.1 Example of slider electrode layout pattern design

Figure2-28 shows the recommended pattern for a slider electrode in the self-capacitance method. This pattern is designed for finger touch and ensures that 3 electrodes respond when the slider is touched anywhere other than the two ends. To change the size of the slider, adjustments must be made by adding or removing electrodes rather than expanding or shrinking the pattern.

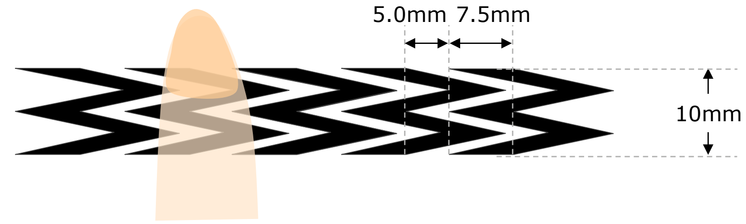


Figure2-28. Recommended Pattern for Slider Electrode for Self-Capacitance Method

2.7.2 Example of wheel layout pattern design

Figure2-29 shows the recommended wheel electrode pattern for the self-capacitance method. This pattern is designed for finger touch and ensures that 3 electrodes respond no matter where the wheel is touched. To change the size of the wheel, adjustments must be made by adding or removing electrodes rather than expanding or shrinking the pattern.

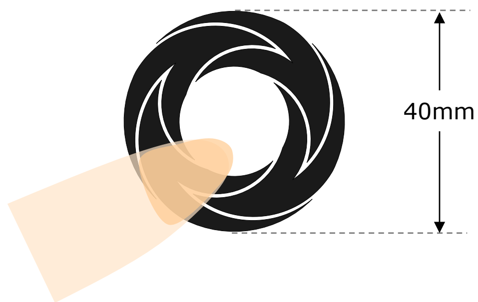


Figure2-29. Recommended Pattern for Wheel Electrode for Self-Capacitance Method

2.7.3 Film-type circuit boards

Film-type circuit boards are thinner and more flexible than printed circuit boards (PCBs) and are increasingly being used for touch electrodes because they enhance the final product design. Film-type boards include flexible printed circuit boards (FPCs), on which patterns are formed with conductive metal (mainly copper foil) on a base film, and film devices for which patterns are printed on a base film with conductive paste. The basic concept of electrode circuit design for capacitive touch buttons, both for FPCs and film devices, is the same as the description in 2.1 Outline of Design Recommendations. The following sections explain precautions and the design recommendations that we suggest you avoid because they are difficult to implement when designing with film-type substrates.

2.7.3.1 Flexible printed circuit boards

FPCs use copper foil for the patterns and can be designed with two or more layers, allowing for layouts similar to the PCB design recommendations. For PCB design recommendations, see 2.1 Outline of Design Recommendations. Precautions and design recommendations that are not appropriate for FPCs are as follows.

When mounting an IC device such as an MCU on an FPC, avoid placing a touch electrode directly beneath the device on the FPC surface. Doing so may lead to increased parasitic capacitance in the touch electrode circuit and make it more susceptible to noise emitted by the IC device.

When placing a shield pattern directly under the touch electrode or wiring, the parasitic capacitance increases because the board is thin and the pattern layers on both sides of the board are close to each other. When shielding the touch electrode or wiring, use a cross-hatched GND pattern. If increased parasitic capacitance is a concern, design the shield pattern for the touch electrode or wiring farther away than the recommended distance, or widen the cross-hatched pattern pitch or space to keep the parasitic capacitance below the recommended conditions for the touch electrode circuit.

CTSU can be measured even if the parasitic capacitance connected to the TS pin exceeds the recommended range, but the sensor drive pulse frequency is 0.5 MHz and the SNR of the button is reduced. If the parasitic capacitance connected to the TS pin is in the deprecated range, measurement errors, overflows, and underflows will occur in the CTSU measurements, and reduced SNR and button detection will not be possible. In that case, consider whether the pitch and space of the hatched shield pattern can be increased to reduce the parasitic capacitance to the recommended range of the touch electrode circuit. In addition, by reducing the total resistance, the upper limit of the parasitic capacitance recommendation range can be raised. If the total resistance value is greater than 560 Ω, consider whether it is possible to reduce the total resistance value by reducing the damping resistance value from the reference value of 560 Ω.

In order to prevent deterioration of external noise immunity and excessive output current of the TS pin, select the damping resistor value so that the total resistance value of the TS pin (the total resistance value of the damping resistor and the FPC) is in the range of 560 Ω to 1 kΩ.

Parasitic capacitance increases when the touch panel is installed in the product housing, due to how it is attached to the hardware or placement space that is narrow and close to other electrodes or wiring. Always design the touch electrode circuit pattern taking this increase into consideration.

2.7.3.2 Film device

Film devices, on which have patterns are printed, can be manufactured at a lower cost than FPCs. They also support transparent patterns, making it easy to place a light source directly under the touch electrode to illuminate the buttons. On the other hand, film device patterns are formed using conductive pastes that use ITO, silver, and carbon, so their resistance is higher than that of copper foil patterns found on FPCs and PCBs. Film devices are typically manufactured with single-layer patterns. While it is possible to manufacture multi-layer patterns, vias cannot be used to connect both sides, resulting in less design flexibility compared to FPC or PCB. Therefore, film devices are generally configured with only touch electrodes and wiring, and then connected with an FPC/FFC connector to the control board on which the CTSU microcontroller is mounted.

Although any conductive material can be used for the electrode, note that materials with high surface resistance—such as transparent electrodes made of ITO and AG materials, or carbon-based electrodes—can reduce the sensor drive pulse frequency of the CTSU and may reduce touch sensitivity. Also, materials with high surface resistance may not be consistently sensitive depending on where the finger is placed. If such a material must be used, lay out the wiring as shown in Figure2-30 (b) arrange wiring as close to the center of the electrode or (c) surround the entire electrode with a material that has low surface resistance so the resistance value is constant regardless of where the surface is touched. When using copper or other sufficiently low surface resistant material, the wiring can even be routed from any point on the button electrode itself, as shown in example (a).

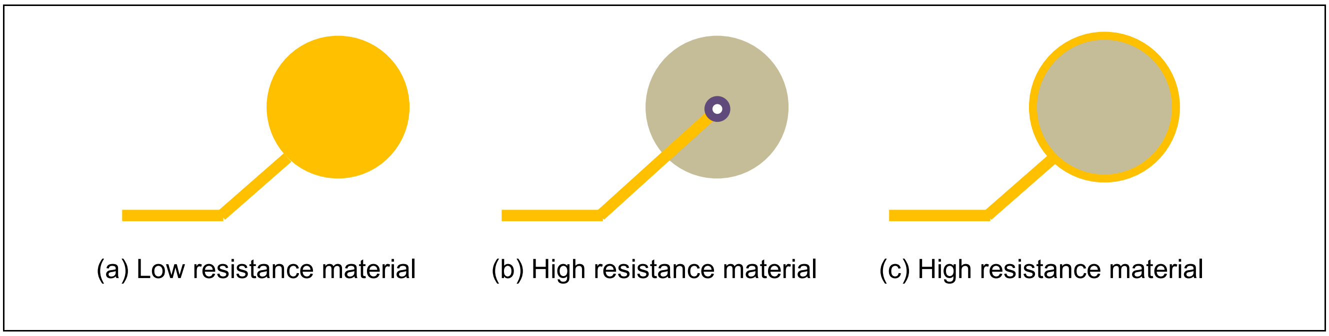


Figure2-30. Button Electrode Wiring Method

The basic design of a film device is the same as that of the PCB design recommendations, as described in section 2.1 Outline of Design Recommendations. Precautions and design recommendations that are not appropriate for film devices are as follows.

Whenever possible, estimate the resistance and capacitance of the touch electrode circuits on the film device and control board at the hardware design stage, and design them so that the CTSU's recommended electrode circuit conditions. Single-sided film devices tend to have longer wiring due to the routing of touch electrode wiring and the wiring from the control board, potentially causing the resistance of the touch electrode circuit to exceed the CTSU recommendation. For designs with longer wiring, consider using a conductive paste with lower resistance or increasing the pattern film thickness during the design stage to reduce overall resistance.

If the total resistance exceeds 1kΩ, and you know the parasitic capacitance when the film electrode is incorporated into the housing of the final product, refer to 4.2 Base Clock Frequency/Sensor Drive Pulse Frequency Settings and calculate a damping resistance value to make the total resistance 1kΩ or less. When using a value other than the recommended 560Ω, use a larger resistance value within the range of the settable sensor drive pulse frequency to prevent a decrease in resistance to external noise and excessive output current from the TS pin. If individual manufacturing differences in the product are expected, select a resistance value one or two levels lower so that it falls within the measurement range of the CTSU based on the worst case.

For single-sided film devices, place as much cross-hatched GND shield as possible on any vacant pattern area around the touch electrode and wiring on the film device to prevent noise. Since there is no shielding layer directly beneath the touch electrode and wiring, avoid placing potential noise-generating devices directly under the film device, and make sure the film device is kept at a distance from the control board.

When placing a shield pattern directly under the touch electrode or wiring on a film device with two or more layers, the parasitic capacitance increases because the substrate is thin and the pattern layers on both sides of the board are close to each other. When shielding the touch electrode or wiring, use a cross-hatched GND pattern. If increased parasitic capacitance is a concern, design the shield pattern for the touch electrode or wiring farther away than the recommended distance, or widen the cross-hatched pattern pitch or space to keep the parasitic capacitance below the recommended value for the touch electrode circuit.

CTSU can be measured even if the parasitic capacitance connected to the TS pin exceeds the recommended range, but the sensor drive pulse frequency is 0.5 MHz and the SNR of the button is reduced. If the parasitic capacitance connected to the TS pin is in the deprecated range, measurement errors, overflows, and underflows will occur in the CTSU measurements, and reduced SNR and button detection will not be possible. In that case, consider whether the pitch and space of the hatched shield pattern can be increased to reduce the parasitic capacitance to the recommended range of the touch electrode circuit. In addition, by reducing the total resistance, the upper limit of the parasitic capacitance recommendation range can be raised. If the total resistance value is greater than 560 Ω, consider whether it is possible to reduce the total resistance value by reducing the damping resistance value from the reference value of 560 Ω.

Parasitic capacitance increases when the touch panel is installed in the product housing, due to how it is attached to the hardware or placement space that is narrow and close to other electrodes or wiring. Always design the touch electrode circuit pattern taking this increase into consideration.

2.7.3.3 Design example

Renesas has released the Touchless Button Demo Solution as a reference design for film-type circuit boards. Design-related information is available at the link below.

Touchless Button Reference Design
https://www.renesas.com/products/microcontrollers-microprocessors/rx-32-bit-performance-efficiency-mcus/touchless-button-ref-touchless-button-reference-design

2.7.4 LED wiring layout

2.7.4.1 Direct lighting example

Figure2-31 shows the electrode pad and LED wiring for the self-capacitance method. We recommend routing the LED around the outer edge of the electrode pad, as shown to the right of the figure. To reduce noise radiated from the LED circuit, cover the LED wiring with a GND shield and, for multi-layer boards, cover the opposite surface with a GND shield as well.

Note that routing the LED wiring in the electrode pad requires a hole to be made in the electrode, reducing the touch-sensitive surface area and bringing the LED wiring in close proximity to the electrode. This increases the risk of weaker sensitivity due to an increased parasitic capacitance.

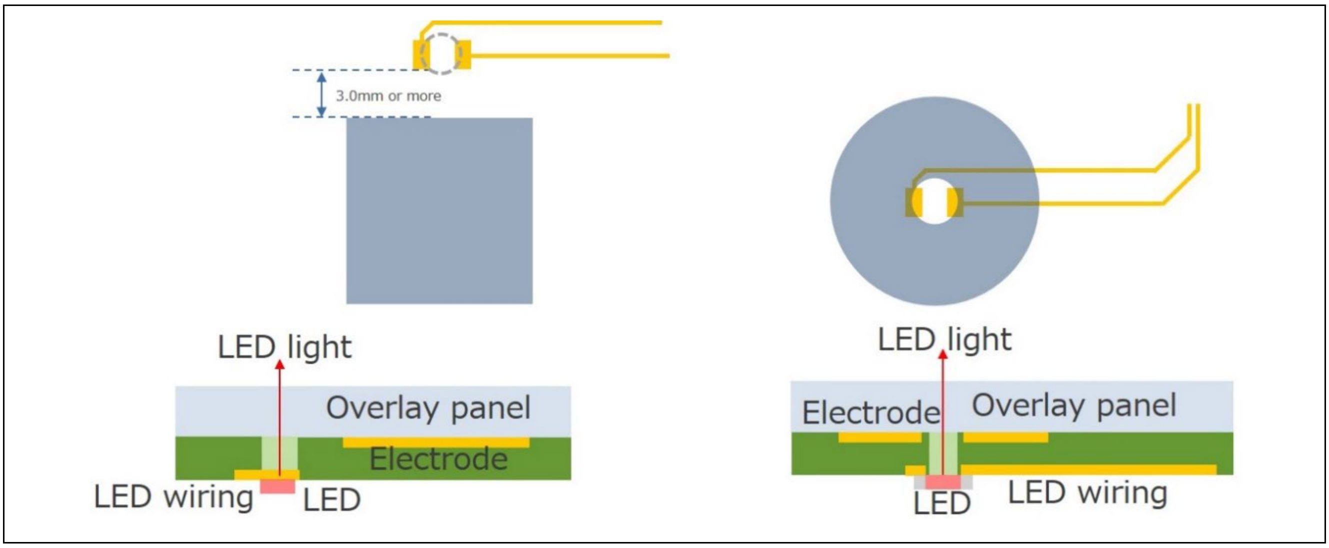


Figure2-31. Electrode Pad and LED Routing Example for Self-capacitance Method

2.7.4.2 Indirect lighting (using light guide plate)

Figure2-32 shows an example of LED routing using an electrode pad and a light guide plate for the self-capacitance method. The LED (the light source) must be a set distance from light-emitting surface to ensure even lighting. Placing multiple LEDs (light sources) in opposing positions helps to eliminate uneven lighting.

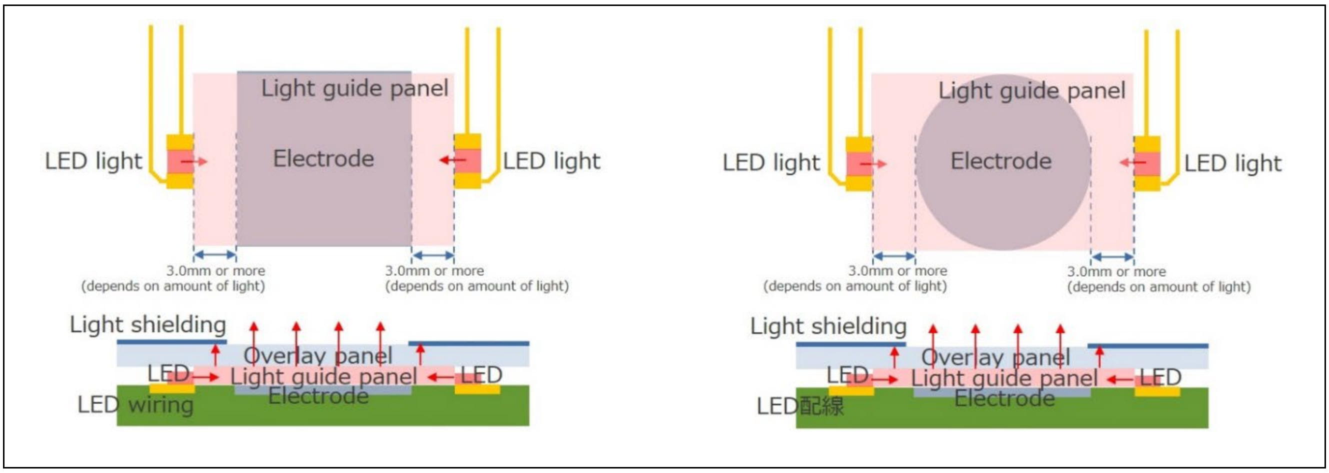


Figure2-32. Example of LED Routing using Electrode Pad Light Guide Plate for Self-capacitance Method

2.7.5 When panel and button electrodes are separated

Figure2-33 shows an example configuration with space between the panel and button electrodes. Although the configuration depends on the size of the button electrode, parasitic capacitance, and other factors, if all conditions are favorable, touch can be detected even with a 2mm air gap between the panel and electrodes. However, the thicker the air gap, the smaller the capacitance change at touch, lowering the SNR of the touch button.

Note that, when dealing with strict noise immunity requirements, if the air gap is larger than 2mm and touch detection is difficult due to other conditions, you may need to extend the button electrodes to the panel, as shown on the right of the figure. For either method, design the layout so that the contact points are electrically connected to the PCB or to the conductive parts corresponding to the touch electrodes on the panel side.

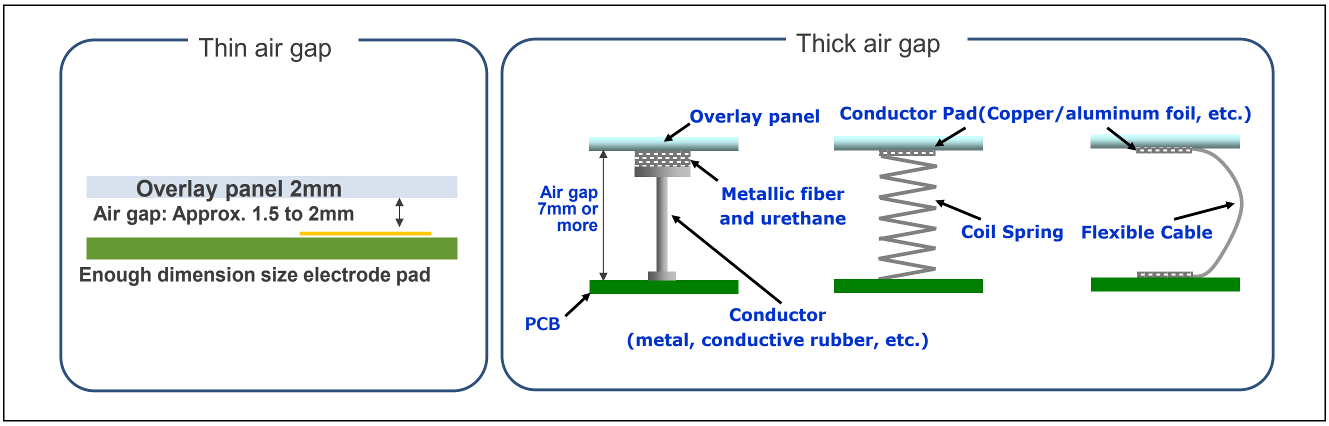


Figure2-33. Example of Air Gap Measure for Auto-capacitance Method

2.7.5.1 Coil spring button design

Using coil springs as self-capacitive touch buttons allows for a wider gap (air gap) between the board and overlay. For example, touch buttons can be placed around tall indicators on the board, such as through-hole type LEDs or 7-segment LCDs, enhancing design flexibility.

Table 2-5 and Table 2-6 list considerations and trends when using coil springs as buttons. For evaluation results, refer to “6. Characteristic Data for Coil Spring Buttons”.

Table 2-5 Coil Spring Button Design Considerations List (1/2)

No	Design project	Description
-	**Coil spring**	
①	Material	Select the appropriate wire material based on the final version of the product's installation environment. Some wire materials may be difficult or impossible to solder onto a circuit board. Consult the spring coil manufacturer and the PCB assembly manufacturer regarding solderability during the design and prototyping stages.
②	Wire diameter	Thin: May deform due to external factors during transport or mounting. Thick: May cause the overlay panel to lift or deform due to increased spring force.
③	Spring shape	Apply compression springs. For touch button applications, cylinder-shaped (Figure2-34) or drum-shaped coil spring (Figure2-35) are typically used.
④	Overlay panel side coil spring diameter /touch button size	The signal value increases as the object size approaches the intended touch size. For a finger, this is approximately 10 to 15 mm. Signal values may decrease if the button size is extremely small or large. For precautions regarding button size, refer to “2.4.2 Electrode pads and wiring”.

Table 2-6 Coil Spring Button Design Considerations List (2/2)

No	Design project	Description
	Coil spring	
⑤	Overlay panel side coil spring tip shape (touch button)	Filling the button area with spiral-shaped wire increases the contact area with the finger, thereby increasing the signal value (Figure2-35). Alternatively, as shown in Figure2-33, installing a coil spring and an electrically conductive pad on the touch area of the overlay panel increases the contact area with the finger, thereby increasing the signal value.
⑥	PCB side coil spring diameter	Filling the button area with spiral-shaped wire increases the contact surface area with the finger, thereby improving the signal-to-noise ratio.
⑦	PCB side coil spring tip shape	When bending pins for through-hole mounting, if the bent portion interferes with the board or through-hole, the spring may be mounted at an angle. To prevent this, either design the spring bend to avoid interference or increase the through-hole diameter to provide clearance for the interfering part.
-	**Board**	
⑧	Spring connection	Mount the coil spring so that it is electrically conductive. For precautions when mounting through-holes, refer to item ⑦ in this table.
⑨	Coil spring and shield spacing	From the maximum coil diameter of the coil spring GND shield: 5mm or more Active shield: 3mm or more
⑩	Other shield pattern designs and dimensions	Refer to Section "2.5.1.1 Shield design"
-	**Overlay Panel**	
⑪	Material	Select the coil spring's spring force considering the final product design. SNR varies depending on the overlay panel material. For the effect of material on sensitivity, refer to "2.6 Effect of Panel Thickness".
⑫	Thickness	As thickness increases, the signal value decreases. The number of coil springs increases the spring force, potentially causing the overlay panel to lift or deform. Design the thickness and panel mounting positions with the final product in mind.

Figure2-34 shows an example of a cylinder-shaped spring coil, and Figure2-35 shows an example of a drum-shaped spring coil. The numbers in the figures correspond to the numbers in Table 2-5.

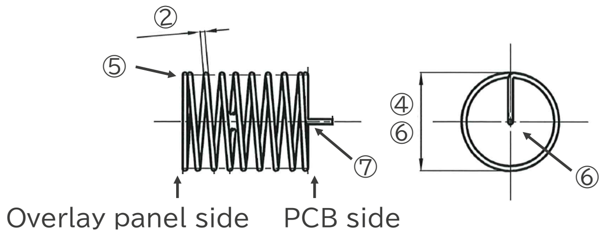


Figure2-34. Example of cylinder-shaped spring coil

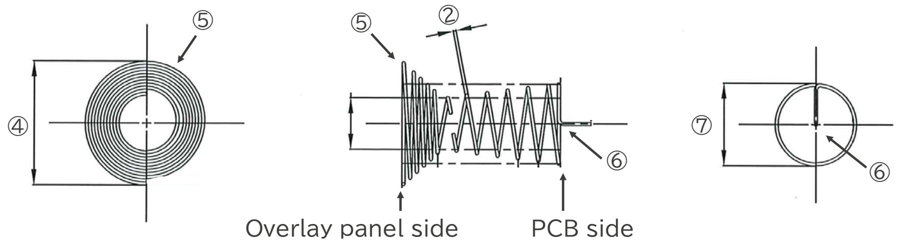


Figure2-35. Example of Drum-shaped spring coil

2.7.6 Self-capacitance Matrix

Self-capacitance matrix configurations in which self-capacitance electrodes are arranged in a grid pattern are not supported by the CTSU driver, middleware, or QE for Capacitive Touch. When using electrodes in a matrix configuration, make sure you use the mutual capacitance method.

2.7.7 Precautions for Using RF Communication Device

Since the CTSU can detect minute changes in the capacitance of the touch electrode circuit, it may be susceptible to noise in the surrounding environment. Radio waves from RF communication devices such as Wi-Fi and Bluetooth® may also affect CTSU measurements. If the antenna of the RF communication device must be placed on the CTSU-embedded MCU board or within the housing, minimize interference by maximizing the distance between the touch MCU/touch electrode circuit and the RF antenna.

2.7.8 Design Example of Metal Overlay Panel

Renesas has released an application note offering a design example using a metal panel as the overlay panel. Design-related information and other details are available at the link below.

Metal Touch Solution Reference Design

https://www.renesas.com/products/microcontrollers-microprocessors/rx-32-bit-performance-efficiency-mcus/metal-touch-ref-metal-touch-solution-reference-design

2.8 Variation and Fluctuation of Parasitic Capacitance

Capacitive touch buttons will experience unintended variations in parasitic capacitance due to changes in the surrounding environment, aging, or assembly variations between the PCB and the overlay panel. Capacitive touch buttons made by Renesas address this through software-based drift correction and offset tuning processes. Software processing alone may not be sufficient in some cases. Therefore, from the step of hardware design, attention must be paid to variations in parasitic capacitance.

This section explains the reasons that cause fluctuations in parasitic capacity and individual changes due to changes of surrounding environment. As for drift correction processing and offset tuning, please refer to the application note "Capacitive Sensor Microcontrollers CTSU Capacitive Touch Introduction Guide (30AN0424)".

2.8.1 Effect of changes in the surrounding environment

Parasitic capacitance fluctuates due to changes in the surrounding environment, particularly when the temperature varies.

Figure2-2 shows the self-capacitance generated at the electrodes; the parasitic capacitance Cp is considered constant for it is static. This is because its change is sufficiently gradual compared to the capacitance Cf that varies with finger operation. Environmental changes alter the substrate and housing, leading to variations in parasitic capacitance Cp.

Figure2-36 shows the parasitic capacitance Cp between the electrode and the shield pattern. The parasitic capacitance Cp varies depending on the relative permittivity of the path of the electric field lines between the electrode and the shield. The left side of the figure shows no overlay panel, with only air present along the electric field line path. In contrast, the right side of the figure places acrylic as the overlay panel. Since acrylic has a relative permittivity of 2.4, which is higher than air's relative permittivity of 1.0, the parasitic capacitance Cp (Acrylic) becomes larger compared to Cp (Air).

The relative permittivity shows temperature characteristics. Therefore, the parasitic capacitance Cp changes according to temperature variations.

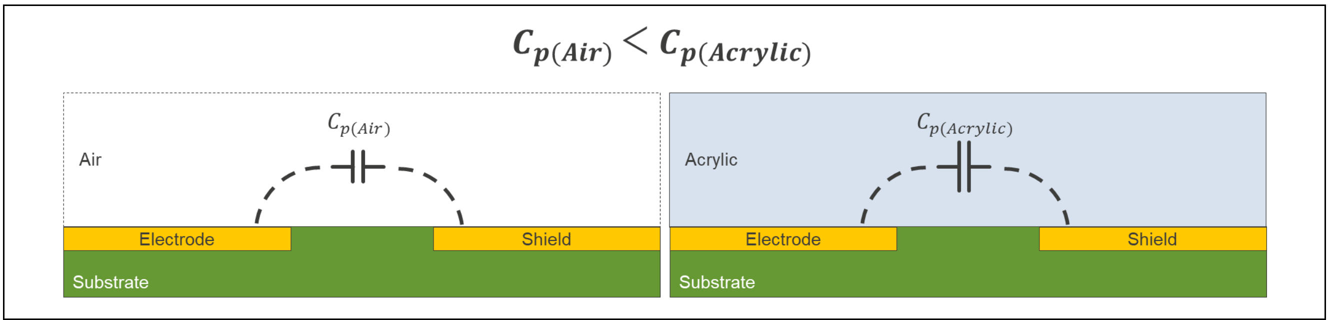


Figure2-36. Image of Parasitic Capacitance between Electrode and Shield

PCBs and enclosures may expand or stretch due to temperature changes. Capacitance changes will occur when thermal expansion happens due to temperature rise. Figure2-37 shows details of an overlay panel expanding due to heat. When acrylic expands, the proportion of the electric field range occupied by acrylic increases. The relative permittivity along the electric field path becomes larger, causing the parasitic capacitance Cp to increase.

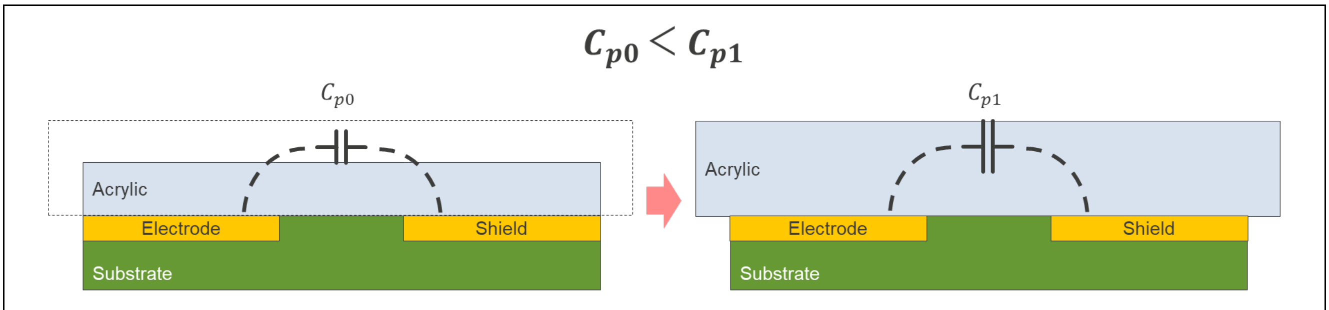


Figure2-37. Image of Overlay Panel Expanding due to Heat

Figure2-38 shows the condition where warping occurs in the substrate or overlay panel due to thermal expansion, resulting in an air gap. Depending on the warping pattern of the substrate or overlay panel, this can cause an air gap between the electrode and the overlay panel. The presence of an air gap along the electric field line path reduces the relative permittivity, leading to a decrease in the parasitic capacitance Cp.

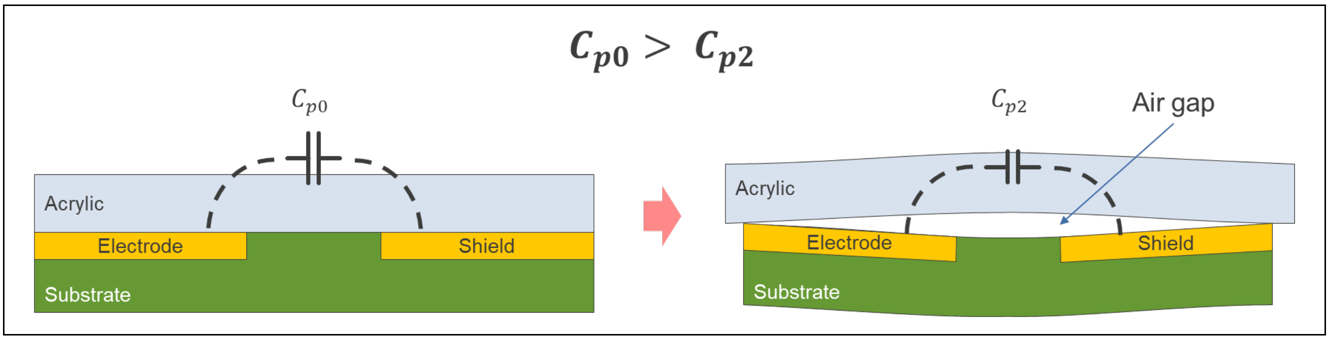


Figure2-38. Image of Air Gap Formation due to Warping

Depending on the materials used for the enclosure and overlay panel, expansion and warping may occur due to humidity changes, potentially causing similar phenomena. Attention should be paid to select appropriate materials suited to the environment and to design the enclosure, considering thermal expansion and warping.

Furthermore, the effects of temperature-dependent dielectric constant changes and warping due to thermal expansion affect not only the parasitic capacitance Cp but also the capacitance Cf between the electrode and the finger. Refer to Section 2.6 for details.

2.8.2 Manufacturing Variations, Individual Differences, and Age-Related Deterioration

In the manufacturing of final products or evaluation prototypes, manufacturing variations may cause fluctuations in parasitic capacitance. Additionally, operational failures may occur due to aging.

Particularly when the PCB pattern is large or when the overlay panel is temporarily fixed during prototype evaluation, an air gap may form between the electrode and the overlay panel. Furthermore, if the overlay panel is secured with adhesive material after product manufacturing, deterioration of the adhesive properties may increase the distance between the electrode and the finger, potentially causing the button to become unresponsive.

To minimize individual variations and performance differences between buttons, it is crucial to ensure the overlay panel is securely fixed to the substrate. Additionally, selecting materials suitable for the application is necessary to minimize the impact of aging.

3. Mutual Capacitance Method: Electrode Layout Patterns

3.1 Outline of Design Recommendations

The mutual-capacitance method boasts button electrodes with superior water-resistance, support based on using matrix structure, and many other functions not available with self-capacitance. However, mutual-capacitance requires complicated button electrode configurations and wire routing, making sensitivity adjustment difficult. The merits and demerits of each method must be taken into account when designing layout patterns. Furthermore, unlike the self-capacitance method, sensitivity is lost when panel thickness falls below a specified level. The designer must carefully consider the button electrode configuration when determining panel thickness.

Always use a multi-layer board of at least two layers for the mutual-capacitance method. This chapter describes a double-layer board as an example.

This section provides reference design information for creating mutual-capacitance method buttons on a printed board. We recommend placing a cross-hatched pattern GND shield guard around the electrodes. We also recommend using an ESD countermeasure by shielding the outer circumference of the board with a GND plane pattern. The numbers listed here correspond to the numbers in each figure, excluding numbers 8 and 9. Each item is described in detail later.

① Electrode shape: square (combined transmitter electrode TX and receiver electrode RX)
② Electrode size: 10mm or larger
③ Electrode proximity: Electrodes should be placed with ample distance so that they do not react simultaneously to the touch object (finger, etc.), (suggested interval: button size x 0.8 or more)
④ Wire width: The thinnest wire achievable through mass production; approx. 0.15mm to 0.20mm for a printed board
⑤ Wiring length: Make the wiring as short as possible. On corners, form a 45-degree angle, not a right angle.
⑥ Wiring spacing:
(A) Make spacing as wide as possible to prevent false detection by neighboring electrodes.
(B) When electrodes are separated: 1.27mm pitch
(C) 20mm or more to prevent coupling capacitance generation between Tx and Rx.
⑦ Cross-hatched GND pattern width: 2mm or more
⑧ Cross-hatched GND pattern (shield guard) proximity
Because the pin parasitic capacitance in the recommended button pattern is comparatively small, parasitic capacitance increases the closer the pins are to GND.
A: 4mm or more around electrodes
We also recommend approx. 2-mm wide cross-hatched GND plane pattern between electrodes.
B: 1.27mm or more around wiring
⑨ Tx, Rx parasitic capacitance: 20pF or less (including overlay panel and TS pin capacitance)
⑩ Electrode + wiring resistance: 560Ω to 1kΩ (including damping resistor with reference value of 560Ω)
⑪ Do not place GND pattern directly under the electrodes or wiring.
The active shield function cannot be used for the mutual-capacitance method.

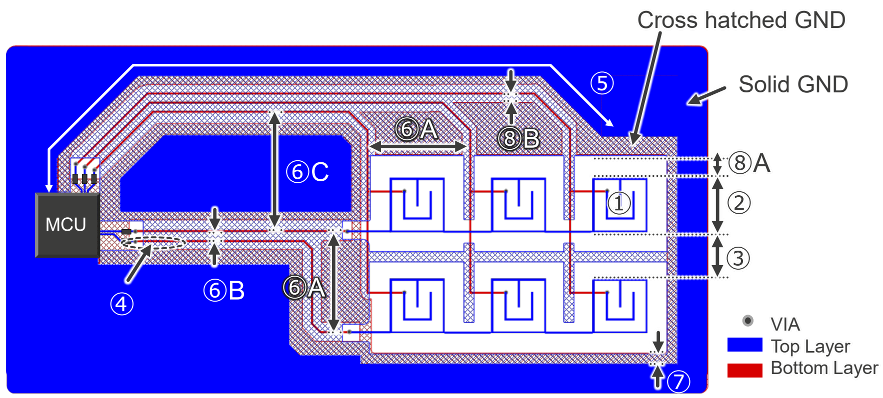


Figure 3-1. Example of Button Pattern for Mutual-capacitance Method

3.2 Mutual-capacitance Method Overview

Figure 3-2 shows the mutual-capacitance generated in the electrode. Mutual capacitance indicates electrostatic capacitance Cm generated by the electric field between two electrodes: transmitter electrode (Tx) and receiver electrode (Rx). When a finger or other body part comes close to the button, a capacitive coupling is created with part of the electric field, causing capacitance Cm to decrease. In the mutual-capacitance method, the CTSU determines whether the button is ON or OFF from the decrease in capacitance Cm caused by the proximity of the finger (body).

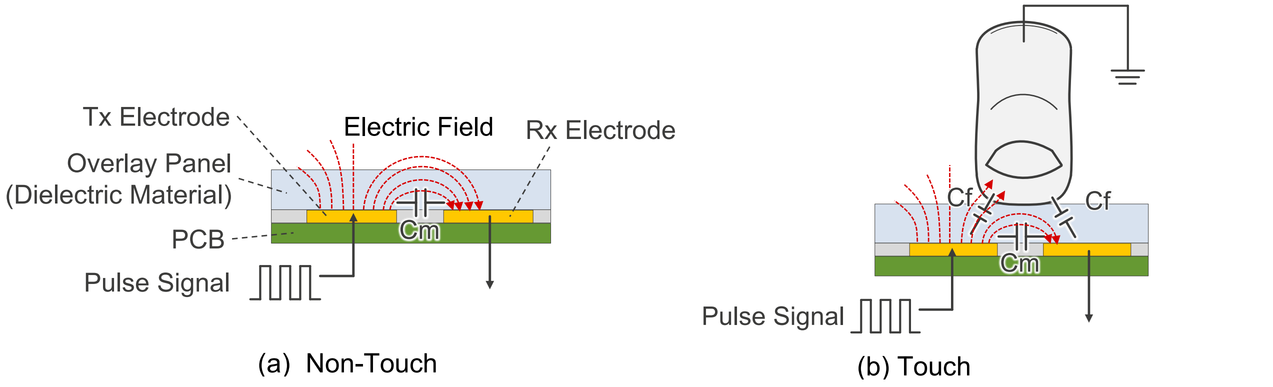


Figure 3-2. Image of Mutual-capacitance Electrodes

3.3 Principle of CTSU Mutual-capacitance Method Detection

Figure 3-3 shows an overview of the CTSU internal configuration for the mutual-capacitance method. The CTSU outputs a digital count that is negatively proportional to the mutual capacitance of Rx and Tx connected to the electrode, and determines whether the touch button is ON or OFF by software.

In order to measure the capacitance Cm existing on the two connected electrodes, the CTSU obtains Cm by inverting the phase relationship between the pulse output and the switched capacitor, measuring the self capacitance twice, then calculating the difference of the two values by software. For more details on the mutual-capacitance detection principle, refer to the application note "Capacitive Sensor Microcontrollers CTSU Capacitive Touch Introduction Guide (R30AN0424)".

The image of CTSU measurement and the relationship between the sensor drive pulse frequency and sensitivity are based on the same concept as the self-capacitance method. For details, see 2.3 Principle of CTSU Self-capacitance Method Detection.

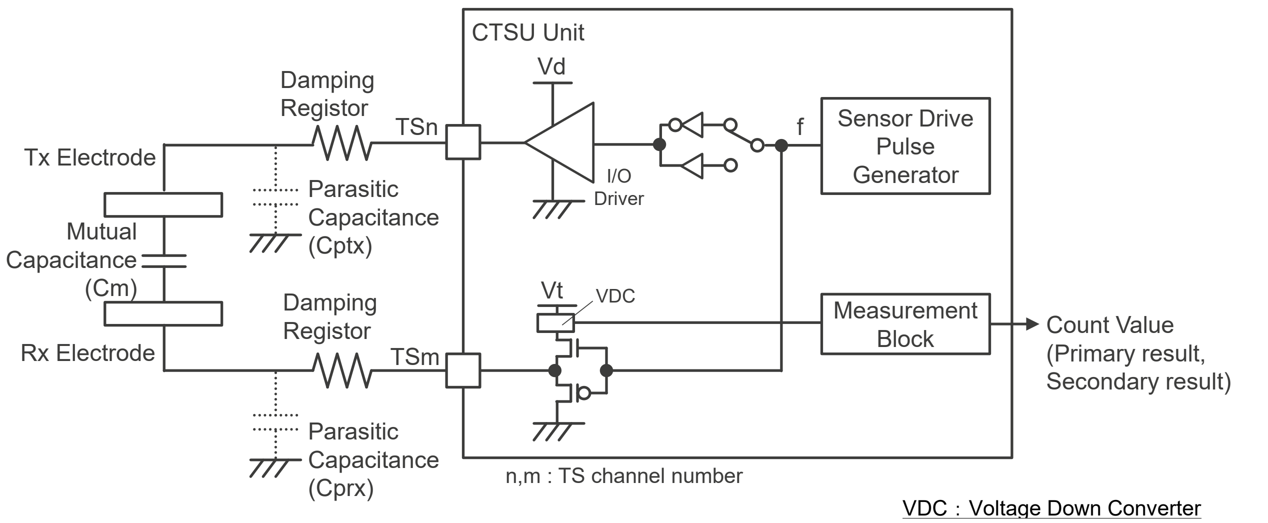


Figure 3-3. Internal Configuration Outline for Mutual-Capacitance Method

3.4 Electrode Pattern Designs

3.4.1 Electrode circuit configuration

Figure3-4 shows an electrode circuit for the mutual-capacitance method. Mutual-capacitance method button electrodes are configured as receiver electrode (Rx) and transmitter electrode (Tx), and include electrode wiring and a damping resistor. The standard value for the damping resistor is 560Ω. Place the damping resistor as close as possible to the TS terminal to prevent noise from mixing in from the wiring between the TS pin and the resistor.

When designing a mutual-capacitive touch electrode circuit, design the pattern and select the materials so that the following recommended conditions are met.

Parasitic capacity C: 20pF or less (including Tx or Rx, overlay panel and TS pin capacitance)
Resistance value R: 560Ω to 1kΩ or less (including damping resistor)

Keep in mind that the electrostatic capacitance C of the entire electrode circuit also includes parasitic capacitance with objects around the board, such as the board’s GND pattern, the overlay panel, and the body chassis. By keeping C low in the design, the touch ON/OFF measurement value difference (signal value) will increase, and the SNR will improve when selecting a high frequency for the CTSU sensor drive pulse frequency. The total capacitance for each electrode can be confirmed using QE for Capacitive Touch.

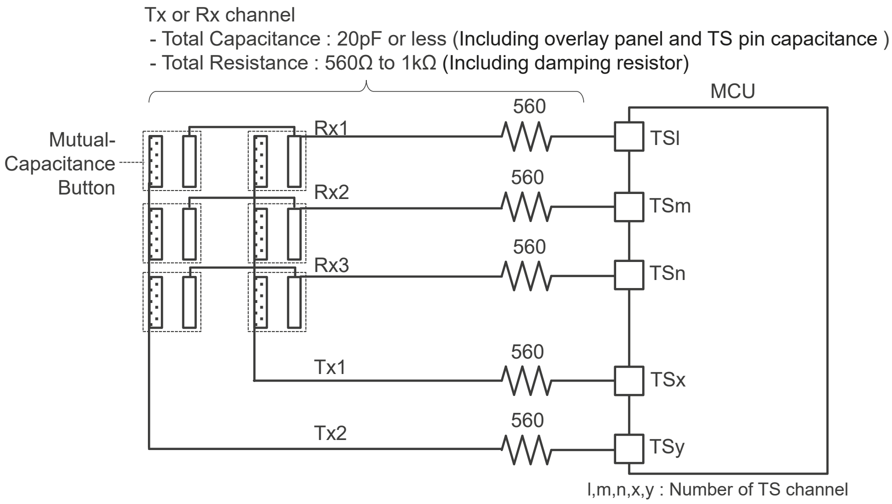


Figure3-4. Electrode Circuit for Mutual-capacitance Method

3.4.2 Electrode pads

Figure3-5 shows the recommended electrode pattern for the mutual-capacitance method. Renesas has verified operation using the pattern in this example. This pattern supports an overlay panel thickness of 2mm to 3mm. The Tx pattern surrounds the Rx pattern to protect the Rx electrode, which is vulnerable to noise. This configuration increases the distance between Tx and Rx opposing sides (called “facing distance” herein) as well as the surface area that comes in contact with the finger.

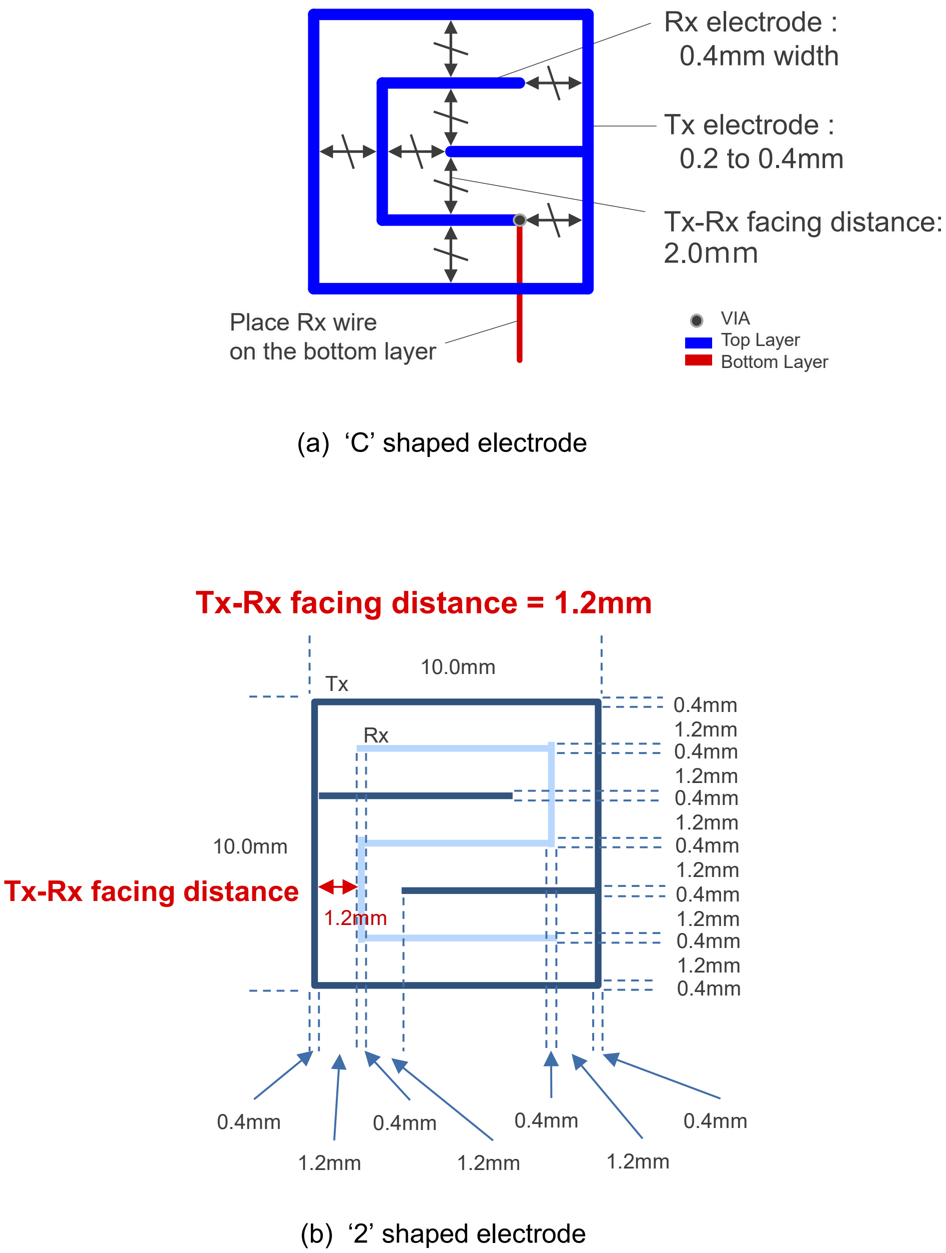


Figure3-5. Mutual Capacitance Method: Pattern Example

Mutual-capacitance method touch measurement measures the electromagnetic field (capacitive coupling) between Tx and Rx and captures the phenomenon of the capacitive coupling decreasing as a fingertip (i.e., part of the human body) in close proximity attracts part of the electromagnetic field. Therefore, the layout pattern must be designed to (1) maximize the capacitive coupling between Rx and Tx, and (2) make the rate of capacitance coupling reduction as large as possible when a finger is in proximity

Figure3-6 shows an image of the Tx/Rx coupling capacitance electromagnetic field for mutual-capacitance method electrodes. A greater Tx/Rx facing distance is required when using a thick overlay panel. However, as most products limit the electrode size, it is often difficult to extend the Tx/Rx distance. As shown in Figure3-5, you may need to use an electrode with a shorter Tx/Rx distance like the Type C electrode, but compared to the Type 2 electrode, the shorter Tx/Rx distance of the Type C electrode means the measured value may also be smaller.

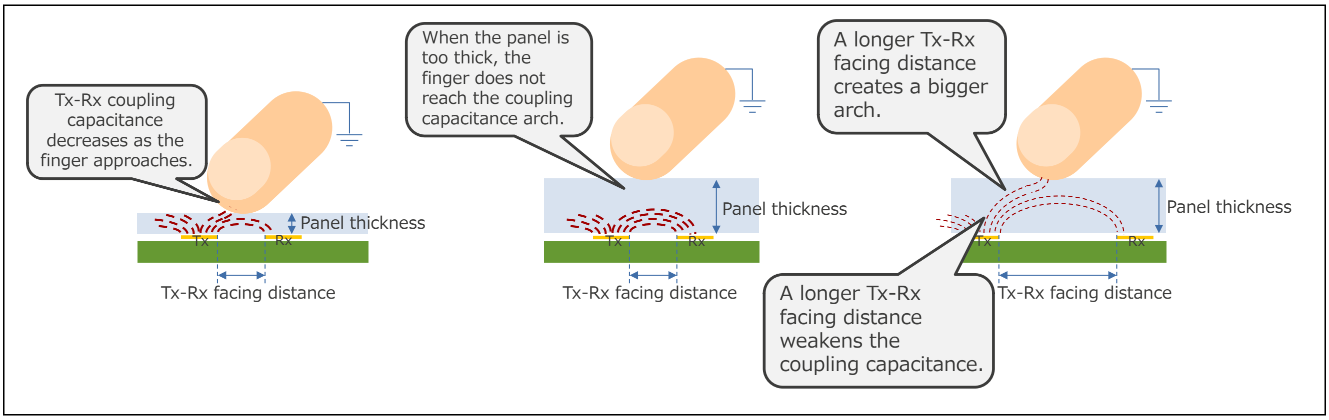


Figure3-6. Image of Electrode Tx-Rx Capacitance Coupling for Mutual Capacitance Method

Figure3-7 shows an image of capacitance coupling based on electrode pad Tx/Rx parallel run distance and Tx/Rx facing distance in the mutual-capacitance method. The longer the parallel run distance of transmitter electrode Tx and receiver electrode Rx, and the shorter the Tx/Rx facing distance, the stronger the capacitive coupling between the Tx and Rx electrodes and the larger the electrostatic capacitance. Also, the electric field induction in the human body increases at touch, causing the Tx/Rx electrostatic capacitance to decrease, resulting in a larger change in the CTSU measurement value. When electrode pads are the same size, the longer the Tx/Rx parallel run distance, the more complicated the layout. In addition, a longer Tx/Rx facing distance supports thicker overlay panels and air gaps, but creates a denser electromagnetic field, leading to lower capacitance.

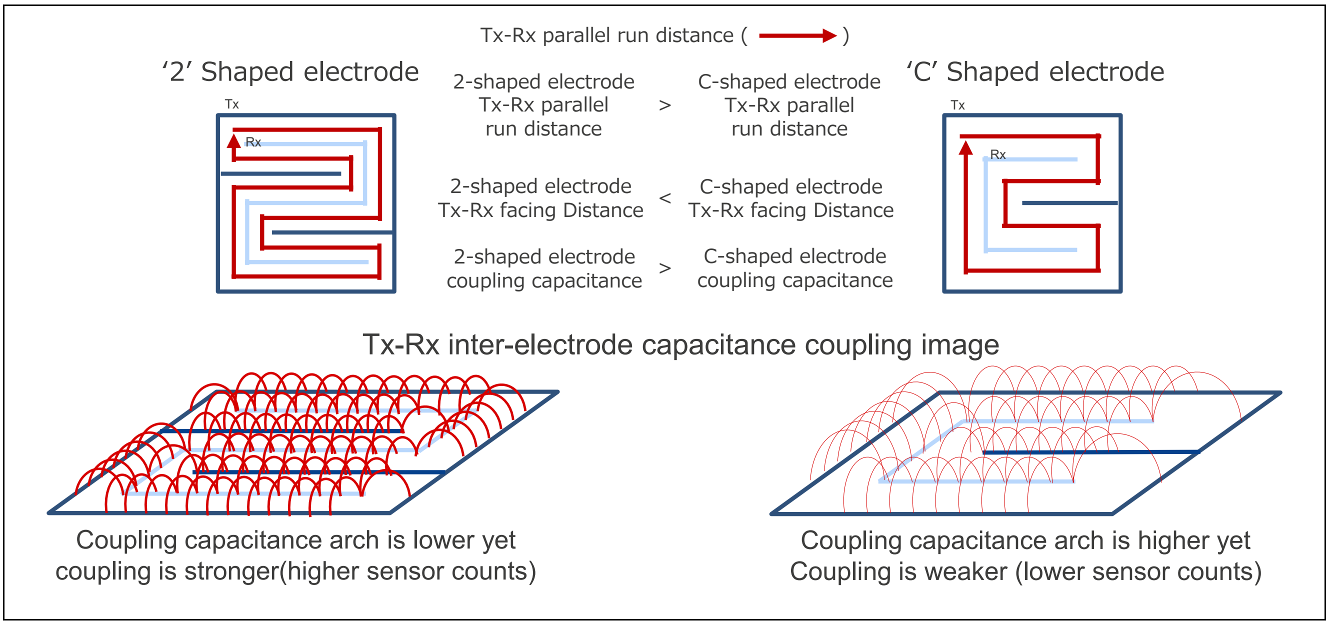


Figure3-7. Image of Capacitance Coupling Based on Electrode Tx/Rx Parallel Run Distance and Facing Distance for Mutual-capacitance Method

Figure3-8 shows the electrode Tx/Rx coupling capacitance electromagnetic field and air gap (incl. panel thickness) for the mutual-capacitance method. In this method, when the layout design includes an air gap between the electrode and overlay panel, the Tx/Rx facing distance must be as long as possible, in the same manner as when using a thick panel. The facing distance between the transmitter electrode Tx and receiver electrode Rx depends on the panel thickness. The recommended Tx/Rx facing distance is approx. 0.6 times the panel and air gap thickness.

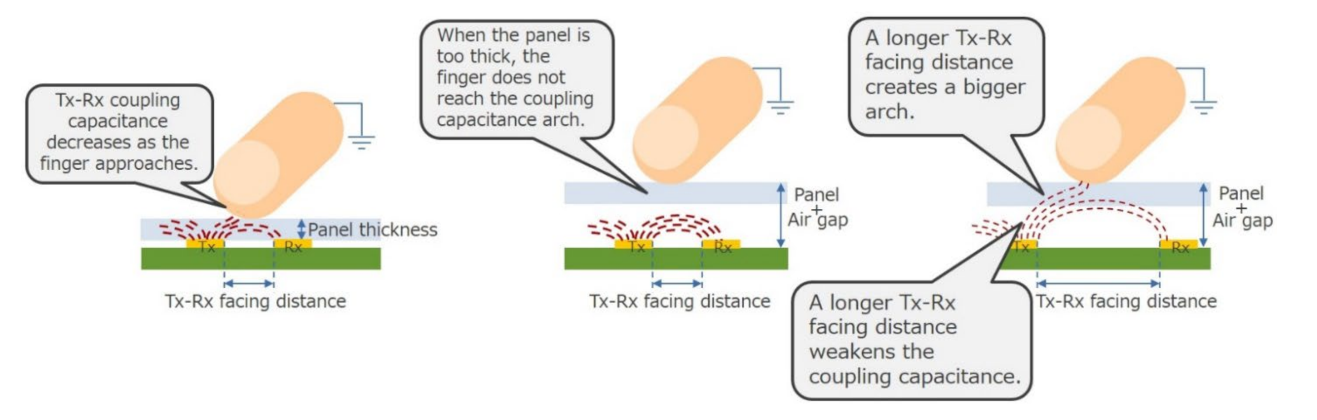


Figure3-8. Tx/Rx Coupling Capacitance Electromagnetic Field and Air Gap (incl. panel thickness) for Mutual Capacitance Method

The following are points to consider when designing mutual-capacitance method button patterns other than those shown in Figure3-5.

No	Design Parameter	Ideal Design	Description	Design Considerations
①	Tx/Rx facing distance	Approximately 0.6 times the total thickness of the panel and the air gap.	The reaction distance changes in the vertical direction of the electrode.	Wide spacing: Overlay panel can be thicker, but SNR will decrease. Narrow spacing: SNR is improved, but the overlay panel needs to be thinned.
②	Tx/Rx parallel run distance	Long distance	SNR will increase. Tx-Rx parasitic capacitance (mutual-capacitance) will increase. The reduction in Tx/Rx mutual-capacitance at touch will increase.	Short parallel distance, SNR will decrease.
③	Electrode size (Tx surrounds Rx)	10x10mm to 15x15mm	By maximizing the facing distance between electrode and finger, mutual capacitance is reduced significantly at touch, maximizing the SNR.	
④	Tx electrode pattern width (wiring width)	Thick and wide area	The electric field emitted by Tx becomes stronger and Tx/Rx mutual capacitance increases. The SNR improves.	If the line width is thin or the area is narrow, Tx/Rx mutual-capacitance decreases. Touch detection may fail.
⑤	Rx electrode pattern width (wiring width)	Thick and wide area	The electric field received by Rx becomes stronger and Tx/Rx mutual-capacitance increases. The SNR improves.	If the line width is thin or the area is narrow, Tx/Rx mutual-capacitance decreases, lowering the SNR. Touch detection may fail.

3.4.3 Wiring

The following are recommended wiring shapes and dimensions.

- Wiring width: 0.15mm (the thinnest wire achievable through mass production)
- Wiring spacing: Rx: 1.27mm pitch
  Tx : 1.27mm pitch
  Rx / Tx interval: 20mm
  However, leave at least 5mm around the electrode pad circumference (about twice the length of the electrode pad) to reduce crosstalk.
- To prevent false detections, increase the distance between Rx and Tx wiring to eliminate capacitive coupling.
- Wiring and cross-hatched GND pattern width: 2.0mm
- Wiring and GND pattern spacing: 1.27mm

Make sure the design satisfies the following wiring requirements as well.

- Keep the wiring as short as possible. Parasitic capacitance increases in proportion to the wiring length. In addition, The longer the wiring length, the more susceptible it is to external noise. Keep this in mind when planning to use the device in environments with RF frequency noise.
  Try to have as few corners in the wiring as possible; make corners 45 degrees or rounded.
  This reduces noise radiated from the wiring.
- Drill vias at the edge of the electrode pad and layout wiring on the back side. This helps reduce malfunctions when wires at touch. However, keep the number of vias at a minimum as they tend to increase parasitic capacitance.
- As an anti-noise countermeasure, place a cross-hatched GND pattern directly under (the back layer of wiring) the electrode and wiring.
- Do not place wiring other than that used for the touch function directly under the electrode wiring.
  If you must do so, make the wiring orthogonal and minimize the facing distance. This reduces the effects of noise caused by capacitive coupling between wires.
- Do not alternate TS pin allocations between Tx and Rx, instead, assign groups of Tx or Rx. If the Tx and Rx wiring are adjacent due to the limited number of MCU pins or layout restrictions, after pulling out the wiring from the TS pin, increase the distance between the Tx wiring and the Rx wiring as much as possible.
- If the electrode is touched near adjacent Rx and Tx wiring, capacitive coupling may occur and cause a false detection. Therefore, place the Rx and Tx wiring as far apart as possible.
- If it is necessary to cross Rx and Tx wiring, place them on the board’s top and bottom layers accordingly, so that the wiring is perpendicular to each other. Minimizing the facing distance of the wiring will minimize capacitive coupling and reduce false detection.

The electrode wiring has a small parasitic capacitance and is susceptible to external noise. Appropriate placement of the GND shield improves noise immunity. In addition, since the non-measurement TS pins of the CTSU are fixed to the GND level, the wiring connected to the TS pins also functions as a shield. The shorter the placement spacing of the GND shield and the TS pin wiring intervals are, the higher the parasitic capacitance of the TS pins will be, so adjust the placement and wiring spacing to satisfy the total parasitic capacitance conditions.

Figure3-9 shows an electrode routing example for the mutual capacitance method. Tx and Rx electrode wiring must be routed with ample distance from neighboring button electrodes and other areas where finger touch is anticipated. This clearance distance will reduce the risk of false detection due to a non-accurate touch, which may occur when a non-electrode pad area is touched. It is important to separate the Tx and Rx electrode wiring so that an unintentional touch does not occur across both traces at the same time. Similarly, if the touch measurement pins (TS) set to Rx and Tx are adjacent, coupling capacitance may occur between the two pins, reducing the relative rate of decreasing capacitance, thus causing a decrease in sensitivity. To prevent capacitive crosstalk, group the Rx and Tx lines separately and keep them as far away as possible

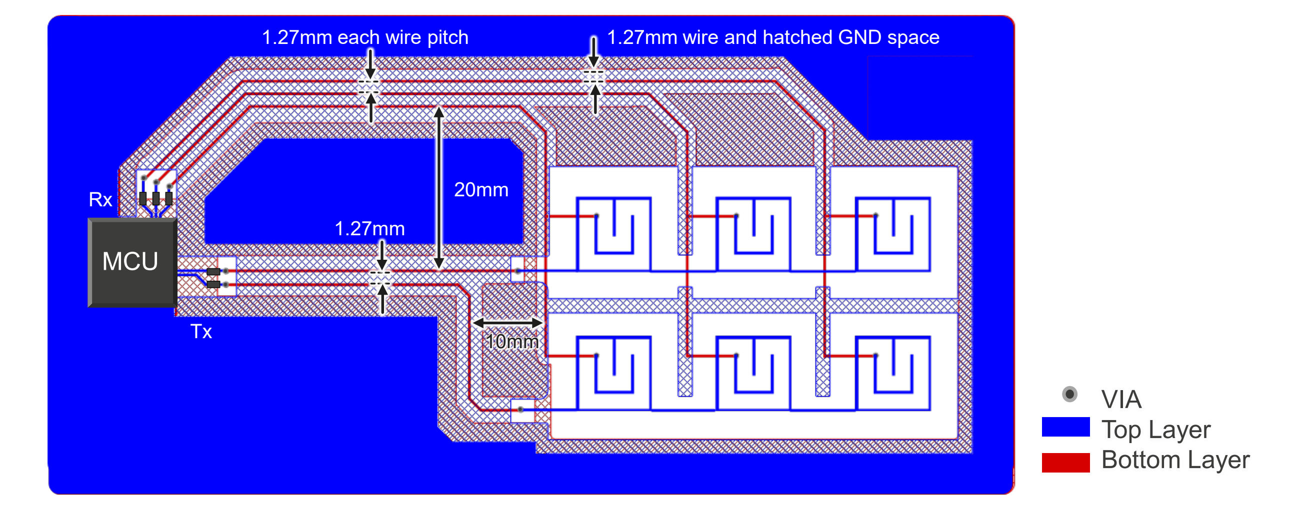


Figure3-9. Example of Electrode Routing for Mutual-capacitance Method

Figure3-10 shows the electrode wiring restrictions that apply in the mutual-capacitance method. Tx and Rx electrode wiring should not be routed in parallel in short range within the wiring area; they must be kept as far apart as possible. If the wiring must cross due to board constraints, do so at a 90º angle as far from the electrode as possible, and then separate the wiring immediately.

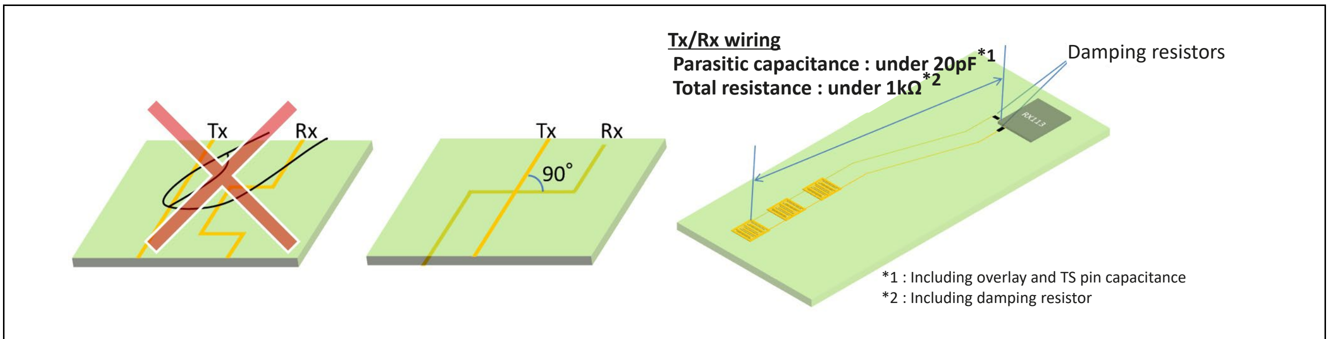


Figure3-10. Electrode Wiring Restrictions for Mutual Capacitance Method

3.5 Distance from Touch Surface to Electrode

Figure3-11 shows the relationship between the amount of capacitance change and the sensitive electrode. In the mutual capacitance method, no matter how close or far apart the finger (human body) and electrodes are, the decrease in Tx/Rx coupling capacitance will be reduced, so panel thickness and air gap thickness are factors to keep in mind at the design stage. As mentioned earlier, the ideal optimal panel thickness, including the air gap, is 1.7 times the distance between the Tx/Rx electrodes.

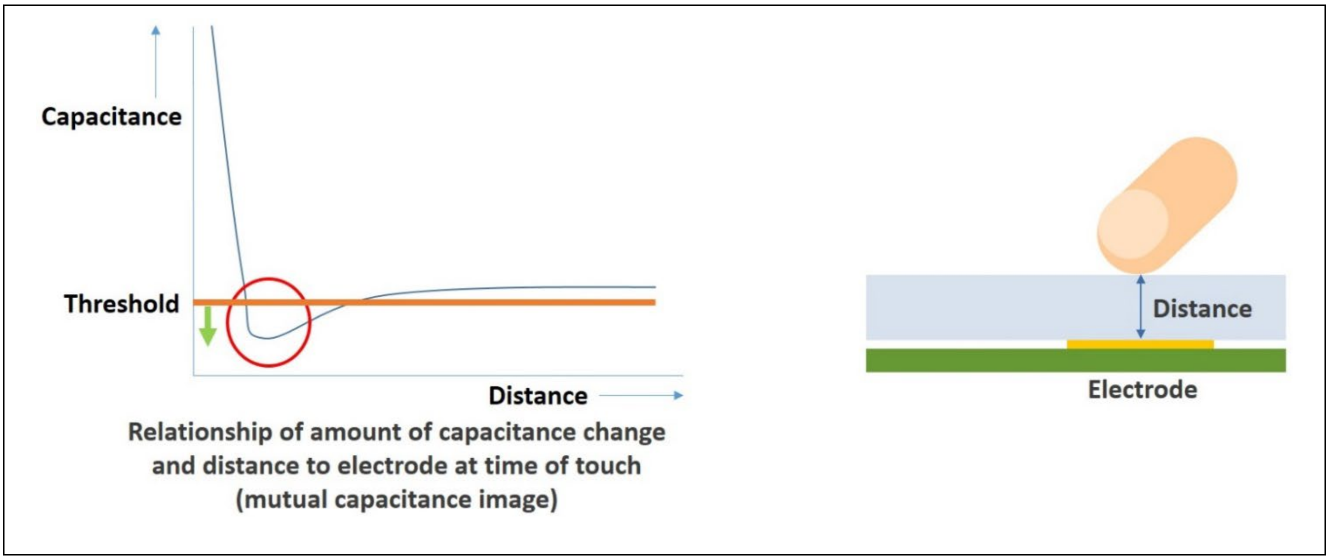


Figure3-11. Relationship of Capacitance Change and Sensitivity Distance for Mutual-capacitance Method

Figure3-12 shows the relationship between inter-electrode distance and panel thickness in the mutual capacitance method. To avoid false detections (crosstalk) between neighboring electrodes, the recommended inter-electrode distance is 2 times or more the panel thickness (including the air gap).

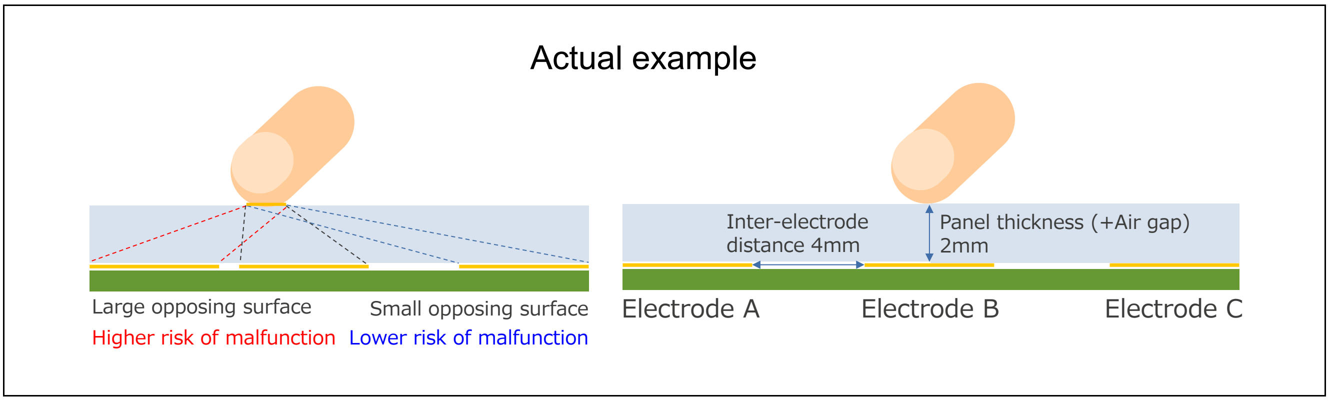


Figure3-12. Relationship of Inter-electrode Distance and Overlay Panel for Mutual-capacitance Method

3.6 Anti-noise Layout Pattern Designs

The electrode circuit configuration makes the electrode act as an antenna (the MCU pin is open only for coupling capacitance) and makes it vulnerable to electromagnetic field noise. Renesas Touch MCUs employ several anti-noise countermeasures to ensure high noise immunity. However, an MCU alone cannot prevent influence from all noise. Hardware countermeasures are indispensable when using the MCU in a severe noise environment. This section includes several design examples.

In general, the longer the wiring, the more chances for noise to synchronize and mix with the many noise frequencies. Make sure the wiring between button electrodes and the MCU is kept as short as possible.

The active shield cannot be used for the mutual capacitance method.

For details regarding anti-noise measurements for the IEC61000 series, see Capacitive Sensor MCU Capacitive Touch Noise Immunity Guide (R30AN0426).

3.6.1 Shield Patterns

3.6.1.1 Shield shapes

Figure3-13 shows the recommended dimensions for cross-hatched patterns. Shielding electrodes and electrode wiring is an effective measure against EMC. On multilayer boards, placing solid shields directly under electrodes and their wiring increases capacitive coupling, making it difficult to detect changes in capacitance at touch. Therefore, we recommended using a cross-hatched shield. Reducing the pitch or spacing from the recommended dimensions will improve noise immunity, but keep in mind that the parasitic capacitance of the electrode circuit will increase as the GND pattern ratio per unit area increases. In addition, the cross-hatched pattern is tilted 45 degrees depending on the wiring direction in order to reduce the capacitive coupling with the electrode wiring.

Item	Dimension
Pitch	1.5 mm
Line Width	0.15 mm
Line Space	1.35 mm

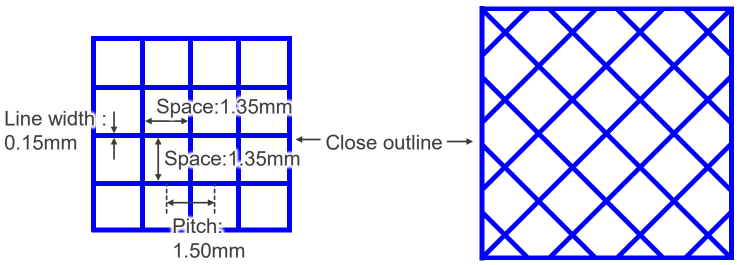


Figure3-13. Cross-hatched Pattern Dimensions

3.6.1.2 GND shield

A GND pattern is placed around the electrodes and wiring to generate capacitive coupling and suppress potential fluctuations caused by the effects of external noise. If a GND shield is placed too close to an electrode, the parasitic capacitance may increase so much that it causes touch detection to fail. If the noise environment is restrictive and the shield must be placed close to the electrode, we recommend a cross-hatching type that reduces capacitive coupling. Additionally, if the parallel run distance becomes longer due to the wiring length, the parasitic capacitance will increase, so it may be necessary to adjust the distance between the wiring and the shield.

① Board layer configuration: Use 2 or more layers as an anti-noise countermeasure
② Pattern shape: cross-hatched pattern
For detailed dimensions, see 3.6.1.1 Shield shapes.
③ Distance between touch electrode and cross-hatched GND shield: 4mm
④ Width of cross-hatched GND shield: 2mm or more
Connect the cross-hatched pattern and the solid GND.
Cover the area directly under the wiring with a cross-hatched GND pattern.
We do not recommend placing a cross-hatched GND shield directly under the electrode, as this will weaken the electric field in the direction of the button electrode overlay panel surface, reducing sensitivity.

Figure3-14 and Figure3-15 shows an anti-noise layout pattern example for the mutual capacitance method. We recommend using a cross-hatched ground pattern to cover the area around the electrode wiring. When the entire wiring area cannot be covered due to layout limitations, place priority on covering the area around the Rx electrode wiring with the cross-hatched GND pattern. Make sure the distance between the electrode wiring and the cross-hatched GND is 4mm or more.

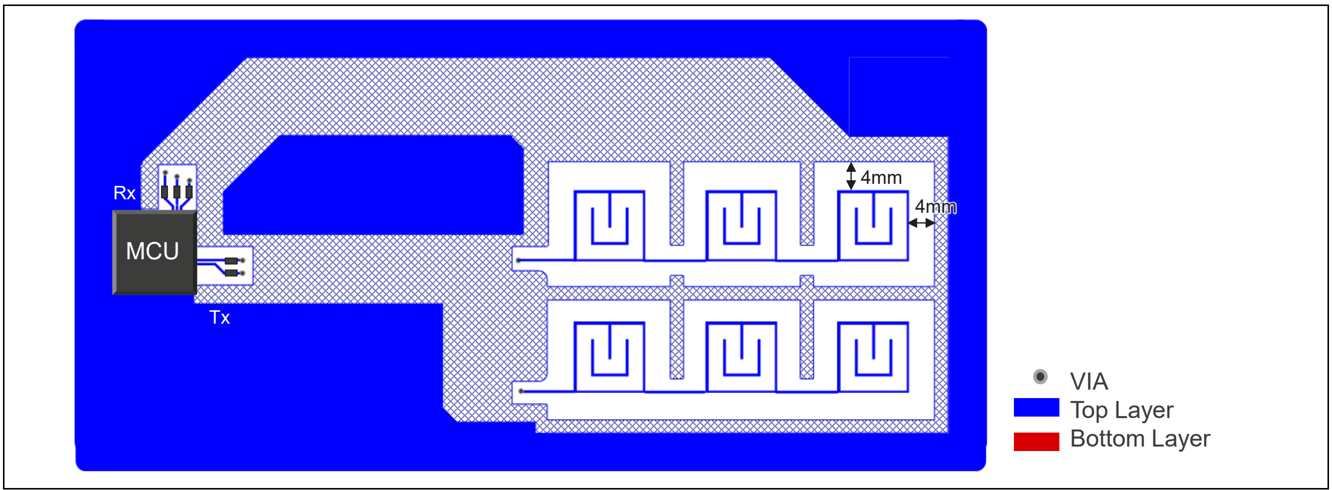


Figure3-14. Anti-noise Countermeasure Layout Pattern Example (top layer)

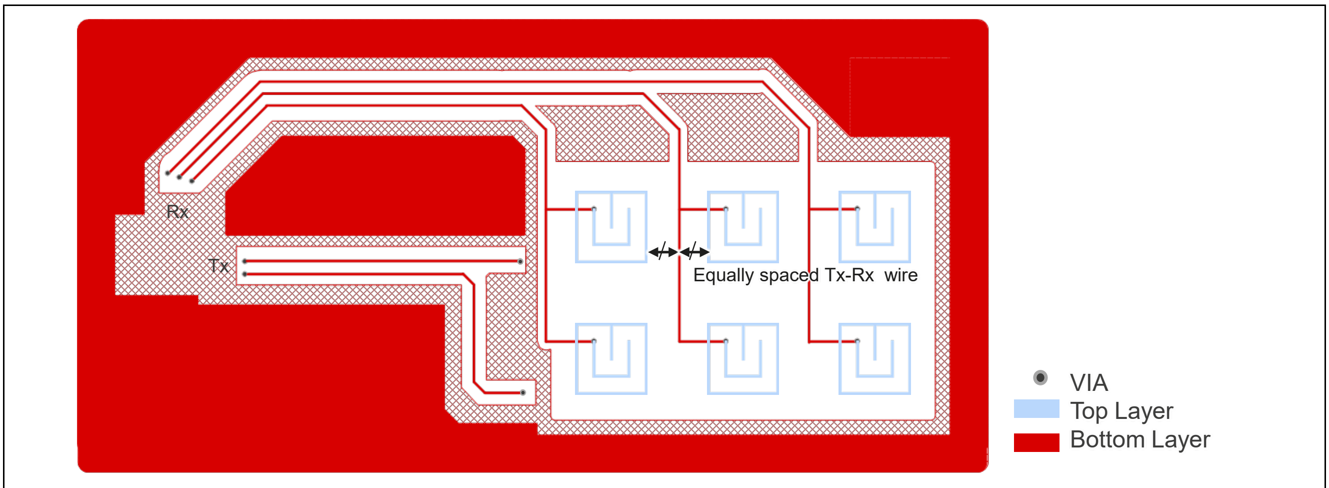


Figure3-15. Anti-noise Countermeasure Layout Pattern Example (bottom layer)

3.7 Design Application Examples

3.7.1 Water-resistant electrode layout pattern design

Figure3-16 depicts cautions regarding water-resistant electrode layout patterns for the mutual capacitance method. If the device is used under flowing water and a water film forms on the electrode surface, when the fingertip touches the water film, the effect is almost as if all electrodes under the water film are touched. This state greatly increases the risk of false detection (crosstalk) between adjacent electrodes in inverse proportion to the resistance value of the flowing water. Using sensing devices in the ocean or in other water containing electrolytes will deteriorate the operating conditions for electrostatic touch. The resistance value of the water film is reduced due to an increasingly thicker water film and a high dielectric constant of the water, which is increased even further by the electrolytes.

Products that require water resistance must be designed with wide spaces between electrode pads as a countermeasure against false detections between adjacent electrodes.

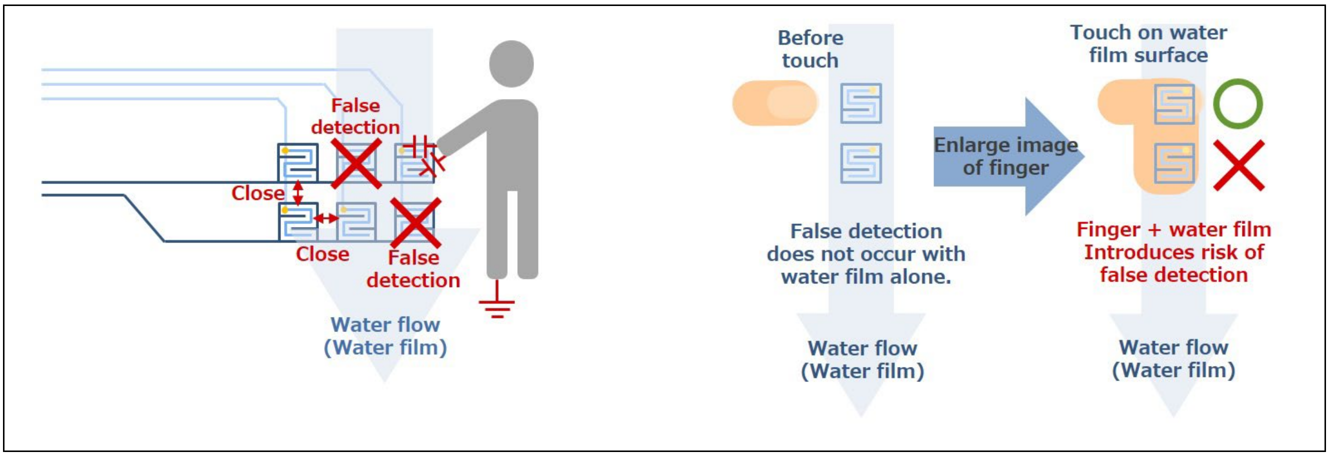


Figure3-16. Cautions for Water-resistant Electrode Layout Pattern in Mutual-capacitance Method

Figure3-17 shows the recommended water-resistant electrode layout for the mutual-capacitance method. Considering that water flows from top to bottom, the best water-resistant layout would be to position all electrodes in a single horizontal line.

Since the Tx wiring, which is not used by the electrode during measurement, outputs low, all Tx can be grouped into one line for water-resistant designs. This will enable the L level output by non-active Tx wiring to bridge with other electrodes via the water film, preventing false detections.

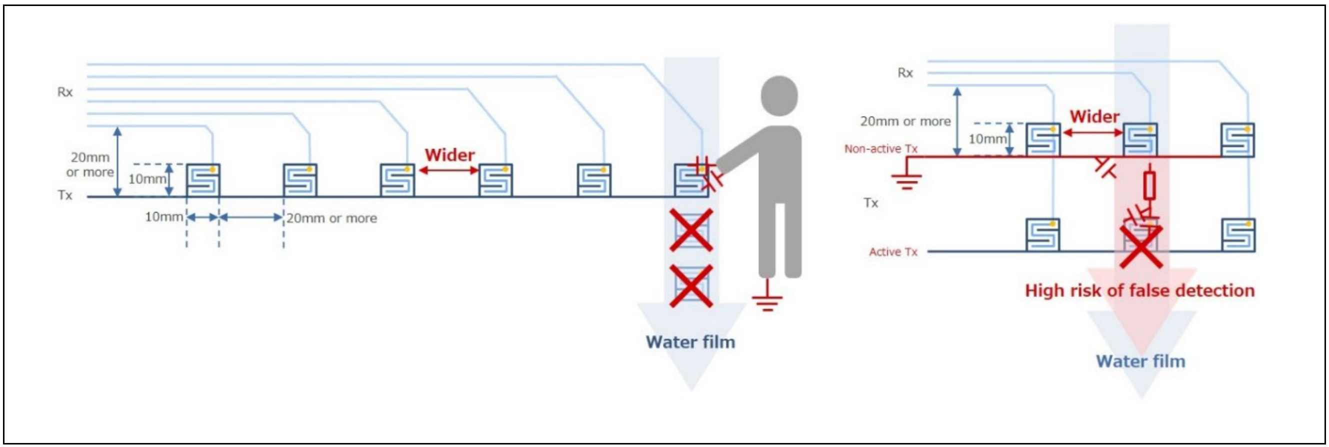


Figure3-17. Recommended Water-resistant Electrode Layout for Mutual-capacitance Method

Figure3-18 shows the relationship between electrode proximity and the overlay panel thickness for the mutual capacitance method. To prevent false detection between adjacent electrodes (crosstalk), the recommended inter-electrode distance is 2 or more times the thickness of the overlay panel (including air gap).

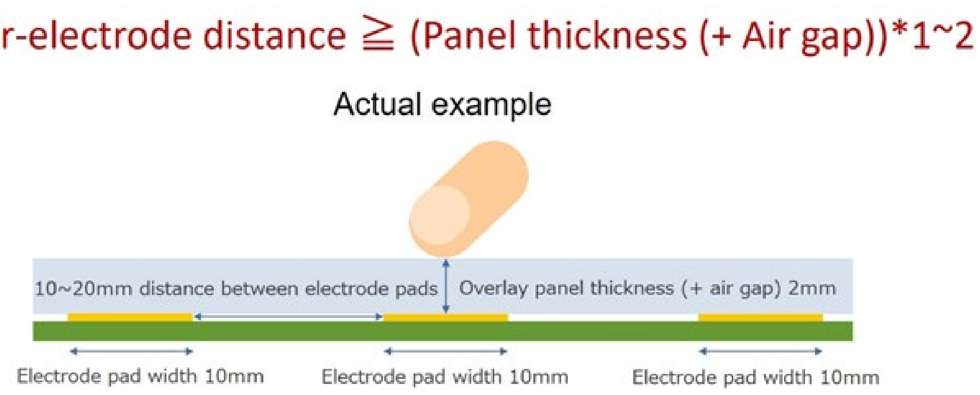


Figure3-18. Relationship of Water-resistant Inter-electrode Distance and Overlay Panel for Mutual-capacitance Method

3.7.2 LED wiring layout

3.7.2.1 Direct lighting example

Figure3-19 shows an example of the electrode pad and LED wiring for the mutual-capacitance method. The ideal routing is to position the LED around the outer edge of the electrode pad, as shown to the right of the figure. In the mutual capacitance method, the Tx/Rx facing area can be increased to improve detection sensitivity. However, this creates difficulty in positioning the LED wiring going into the electrode pad at the Tx and Rx electrodes. The Tx/Rx parallel runs are short and may cause sensitivity deterioration for electrode pads of the same size.

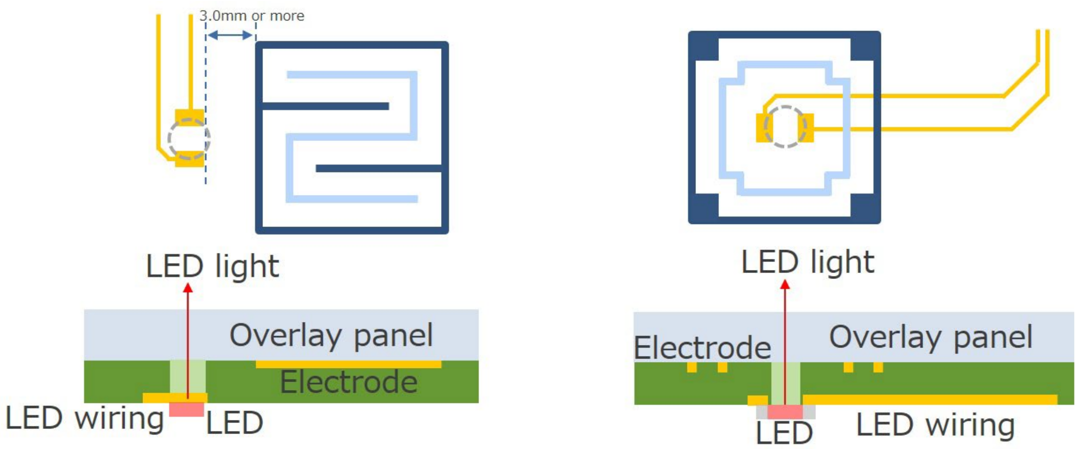


Figure3-19 Electrode Pad and LED Wire Routing for Mutual-capacitance Method

3.7.2.2 Indirect lighting example

Figure3-20 shows an LED routing example using an electrode pad and a light guide plate for the mutual capacitance method. The LED (the light source) must be a set distance from light-emitting surface to ensure even lighting.
Placing multiple LEDs (light sources) in opposing positions helps to eliminate uneven lighting.

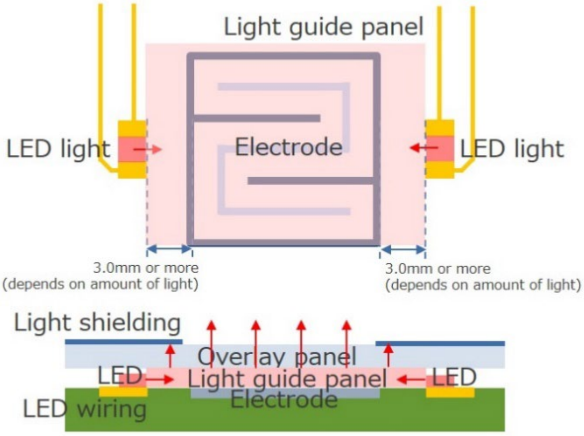


Figure3-20 LED Wire Routing with Electrode Pad and Light Guide Plate for Mutual-capacitance Method

3.8 Variation and Fluctuation of Parasitic Capacitance

Capacitive touch buttons will experience unintended variations in parasitic capacitance due to changes in the surrounding environment, aging, or assembly variations between the PCB and the overlay panel. Capacitive touch buttons made by Renesas address this through software-based drift correction and offset tuning processes. Software processing alone may not be sufficient in some cases. Therefore, from the step of hardware design, attention must be paid to variations in parasitic capacitance.

This section explains the reasons that cause fluctuations in parasitic capacity and individual changes due to changes of surrounding environment. As for drift correction processing and offset tuning processing, please refer to the application note “Capacitive Sensor Microcontrollers CTSU Capacitive Touch Introduction Guide (30AN0424)”.

3.8.1 Effect of changes in the surrounding environment

Parasitic capacitance fluctuates due to changes in the surrounding environment, particularly when the temperature varies. The basic theory is similar to self-capacitance method, referring to Section 2.8.

We explained the temperature-dependent effect on the parasitic capacitance Cp between the electrode and the shield in the way of self-capacitance. However, note that in the mutual-capacitance method, a similar phenomenon occurs in the coupling capacitance Cm between the transmit electrode (Tx) and the receive electrode (Rx).

3.8.2 Manufacturing Variations, Individual Differences, and Age-Related Deterioration

In the manufacturing of final products or evaluation prototypes, manufacturing variations may cause fluctuations in parasitic capacitance. Additionally, operational failures may occur due to aging.

Particularly when the PCB pattern is large or when the overlay panel is temporarily fixed during prototype evaluation, an air gap may form between the electrode and the overlay panel. Furthermore, if the overlay panel is secured with adhesive material after product manufacturing, deterioration of the adhesive properties may increase the distance between the electrode and the finger, potentially causing the button to become unresponsive.

To minimize individual variations and performance differences between buttons, it is crucial to ensure the overlay panel is securely fixed to the substrate. Additionally, selecting materials suitable for the application is necessary to minimize the impact of aging.

4. Reference Materials

4.1 Reference Documents

The latest version can be downloaded from the Renesas Electronics website.

- Capacitive Sensor Microcontrollers CTSU Capacitive Touch Introduction Guide (R30AN0424)
- Capacitive Sensor MCU Capacitive Touch Ripple Noise Prevention Guide (R30AN0426)
- Capacitive Sensor MCU Capacitive Touch Noise Immunity Guide (R30AN0246)
- Capacitive Sensor MCU QE for Capacitive Touch Advanced Mode Parameter Guide (R30AN0428)

4.2 Base Clock Frequency/Sensor Drive Pulse Frequency Settings

This shows the base clock frequency/sensor drive pulse frequency set by auto tuning using QE for Capacitive Touch with a combination of parasitic capacitance and total resistance for a representative MCU of each CTSU version. The “Prefer” is that the sensor drive pulse frequency is set to 1MHz or more by the automatic adjustment of QE for Capacitive Touch. The "Valid" range is the range that can be measured by CTSU, and it is a condition that may reduce the SNR or noise immunity of the measured value compared to the "Prefer" range. The "deprecated" range is a condition in which measurement errors, overflows, and underflows occur in the CTSU measurements, resulting in reduce the SNR and button detection become impossible. In this section, typical values for parasitic capacitance and total resistance are described. See Table 2-2 for detailed numbers in the recommended ranges.

The actual base clock frequency/sensor drive pulse frequency will vary depending on the MCU’s operating clock and the peripheral module clock input to the CTSU module. When designing a board, prototyping and sufficient evaluation should be carried out by the user to determine whether a specific MCU can be used or not. To check the CTSU version installed in each microcontroller, refer to the hardware user's manual for each microcontroller or refer to 4. Capacitive Sensor MCU in Capacitive Sensor Microcontrollers CTSU Capacitive Touch Introduction Guide (30AN0424).

Table 4-1 List of products with built-in capacitive sensors and corresponding figure numbers

Capacitance Sensor Type		**CTSU1**			**CTSU2**	
Product Category/Family	RL78	RL78/G16	-	-	RL78/G22, RL78/G23 RL78/L23	
					RL78/F22, RL78/F25	-
	RX	RX113, RX130 RX230, RX231, RX23W		RX671	RX140 RX260, RX261	
	RA	RA2A1, RA4M1, RA4W1		RA4M2, RA4M3 RA6M1, RA6M2, RA6M3, RA6M4, RA6M5	RA0L1 RA2E1, RA2L1 RA4L1	
CTSU Operating Mode		Normal Operation	Low voltage	Normal Operation	Normal Operation	Low voltage
Category (Note)		A	B	C	D	E
Figure Number (QE for Capacitive Touch V4.1.0 or earlier)		Figure4-1	Figure4-6	Figure4-2	Figure4-3	Figure4-7
Figure Number (QE for Capacitive Touch V4.2.0 or later)		-	-	-	Figure4-4, Figure4-5	Figure4-8, Figure4-9

Note: The Category is specific to this application note.

4.2.1 Normal Operating Mode

4.2.1.1 For QE for Capacitive Touch V4.1.0 or earlier

Figure4-1 shows the relation between the parasitic capacitance/damping resistor of RX130 set by auto tuning and base clock frequency as a typical example of category A in Table 4-1 of CTSU1. The following figures are based on 32MHz operating clocks.

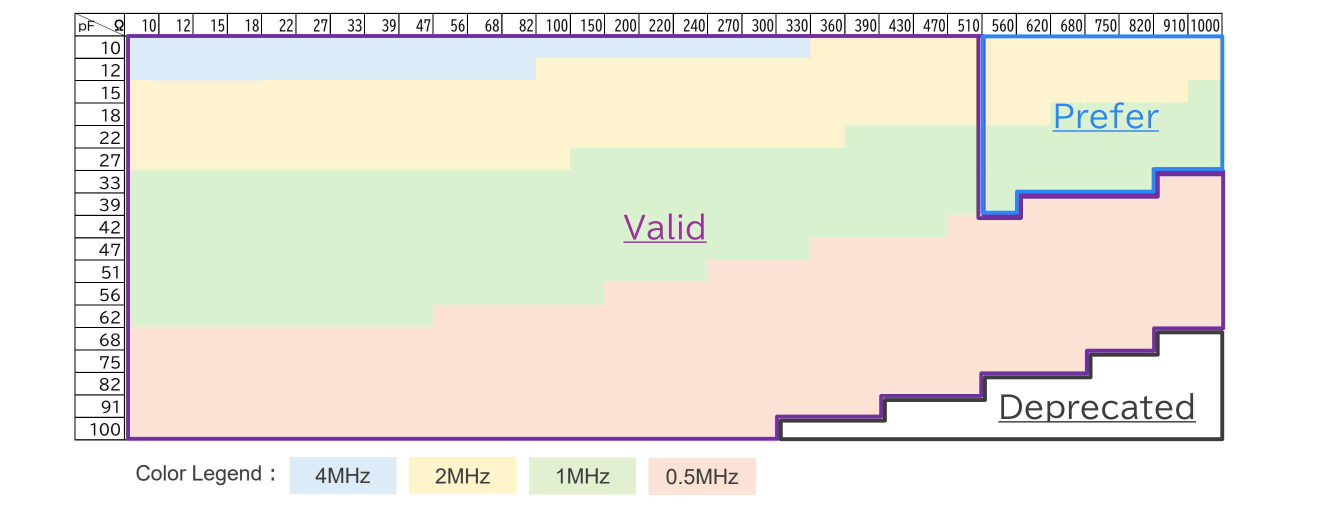


Figure4-1. Relationship between CTSU1 (RX130) Parasitic Capacitance/Damping Resistance and Base Clock Frequency

Figure4-2 shows the relation between the parasitic capacitance/damping resistor of RX671 set by auto tuning and base clock frequency as a typical example of category C in Table 4-1 of CTSU1. The following figures are based on 30MHz operating clocks.

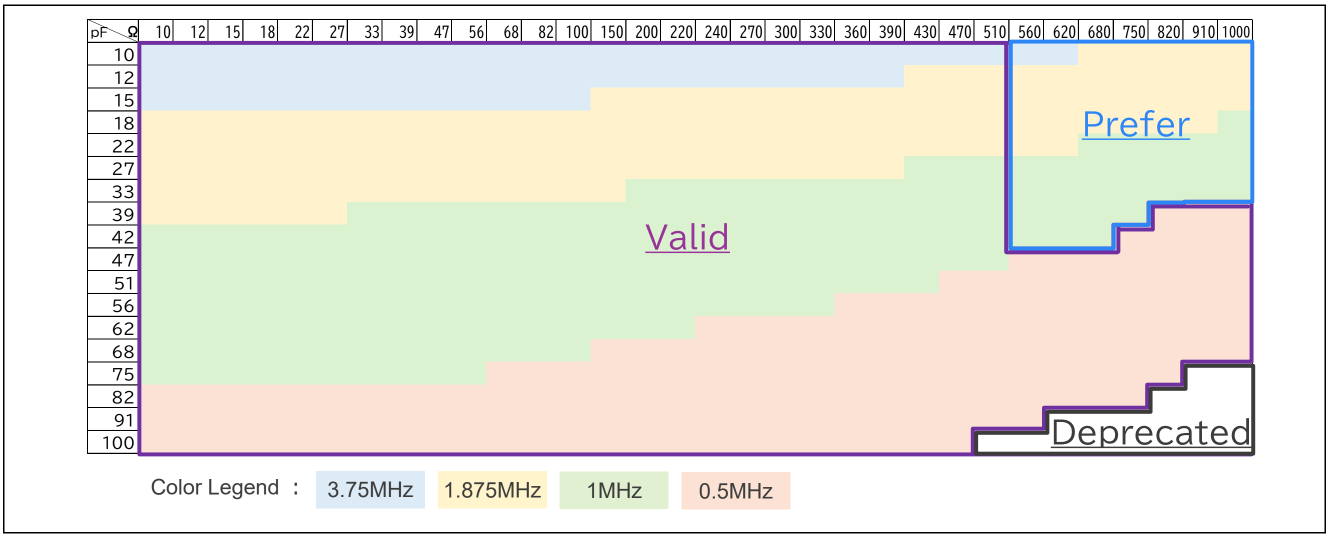


Figure4-2. Relationship between CTSU1 (RX671) Parasitic Capacitance/Damping Resistance and Base Clock Frequency

Figure4-3 shows the relation between the parasitic capacitance/damping resistor of CTSU2 set by auto tuning and base clock frequency.

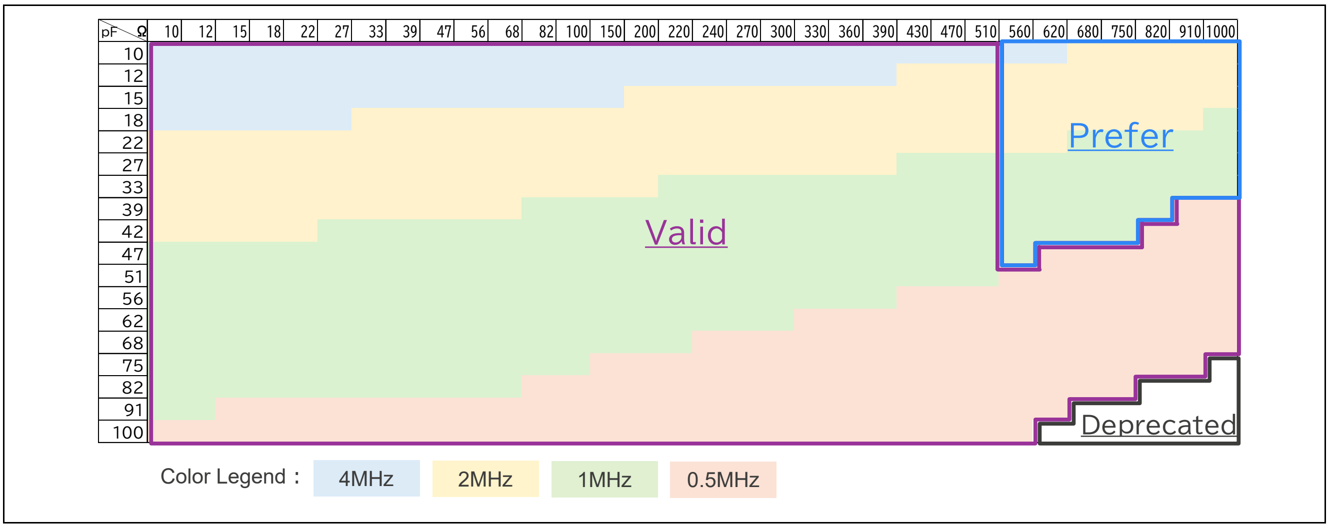


Figure4-3. Relationship between CTSU2 Parasitic Capacitance/Damping Resistance and Base Clock Frequency

4.2.1.2 For QE for Capacitive Touch V4.2.0 or later（Only for CTSU2-embedded MCU）

Figure4-4 shows the relationship between the parasitic capacitance/damping resistance in low-voltage mode and the sensor drive pulse frequency set by auto-tuning for the CTSU2 and RX140 (SUCLK 40 MHz upper limit) as a representative Category D device in Table 4-1.

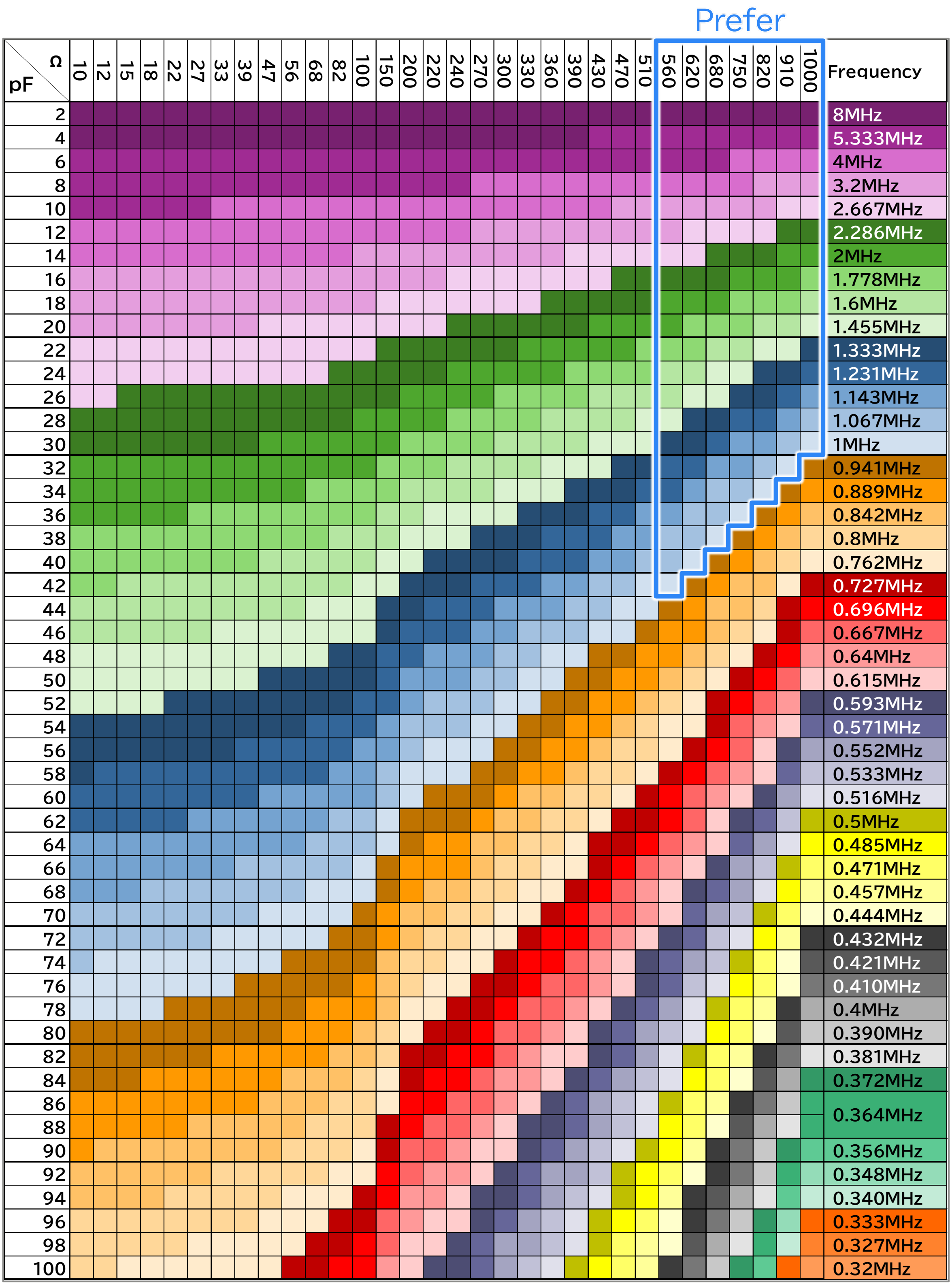


Figure4-4. Relationship Between Parasitic Capacitance/Damping Resistance of CTSU2 and Sensor Drive Pulse Frequency (QE for Capacitive Touch V4.2.0 or Later)

Figure4-5 shows the relationship between the parasitic capacitance/damping resistance in the low-voltage mode of the RL78/G23 (SUCLK 32 MHz upper limit) as a representative of Category D in Table 4-1 and the sensor drive pulse frequency set by automatic tuning.

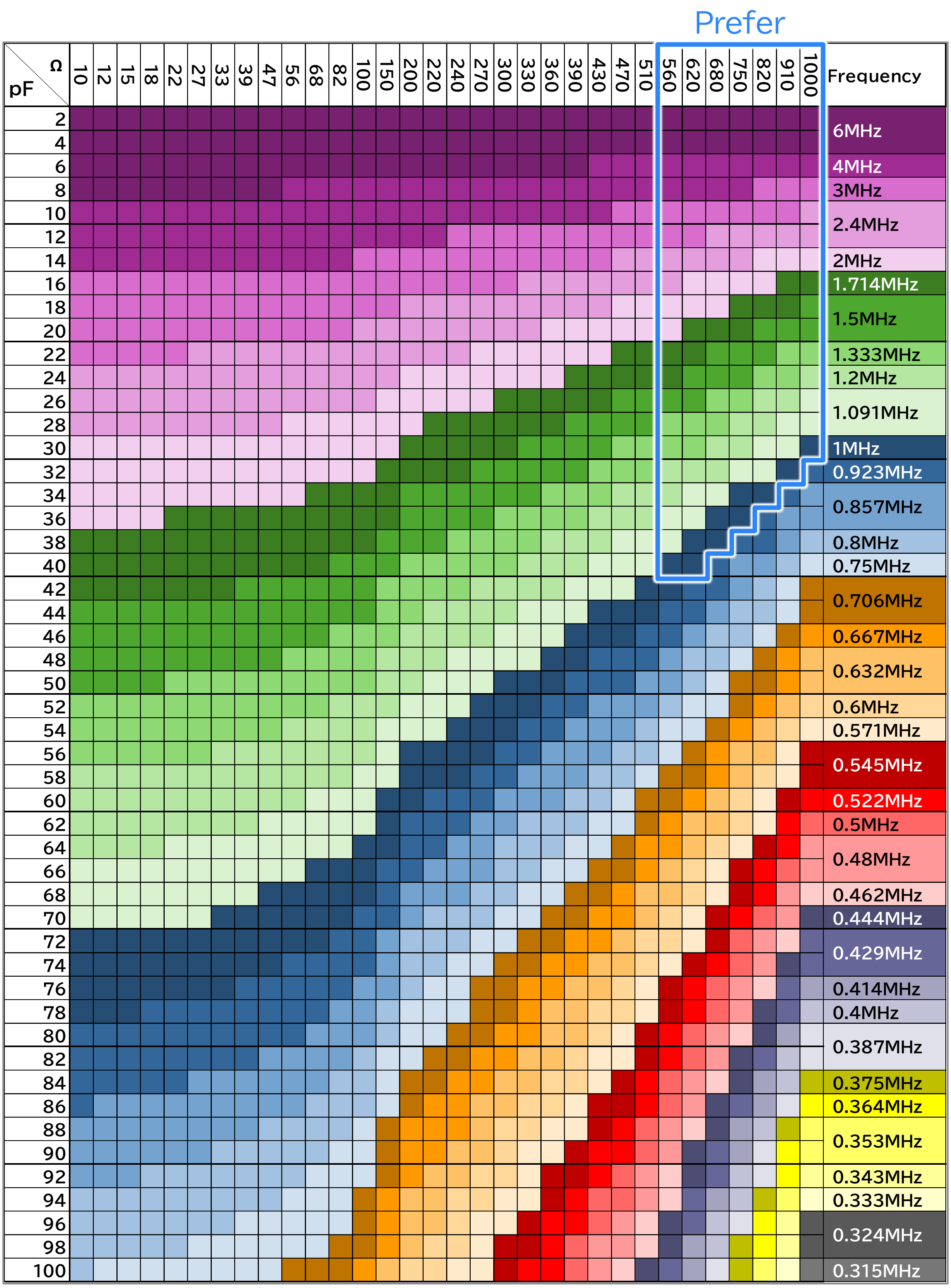


Figure4-5. Relationship Between Parasitic Capacitance/Damping Resistance of CTSU2 and Sensor Drive Pulse Frequency (QE for Capacitive Touch V4.2.0 or Later)

4.2.2 Low Voltage Operating Mode

4.2.2.1 For QE for Capacitive Touch V4.1.0 or earlier

Figure4-6 shows the relation between the parasitic capacitance/damping resistor of RX130 set by auto tuning and base clock frequency as a typical example of category B in Table 4 1 of CTSU1 in low voltage operating mode. The following figures are based on 32MHz operating clocks.

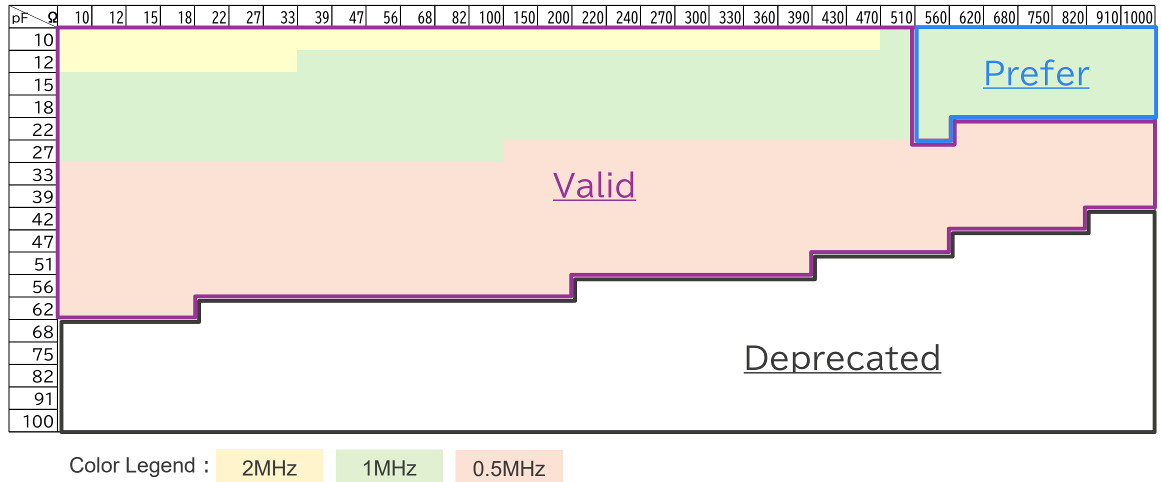


Figure4-6. Relationship between CTSU1 (RX130, Low Voltage Operating Mode) Parasitic Capacitance/Damping Resistance and Base Clock Frequency

Figure4-7 shows the relation between the parasitic capacitance/damping resistor of CTSU2 in low voltage operating mode set by auto tuning and base clock frequency.

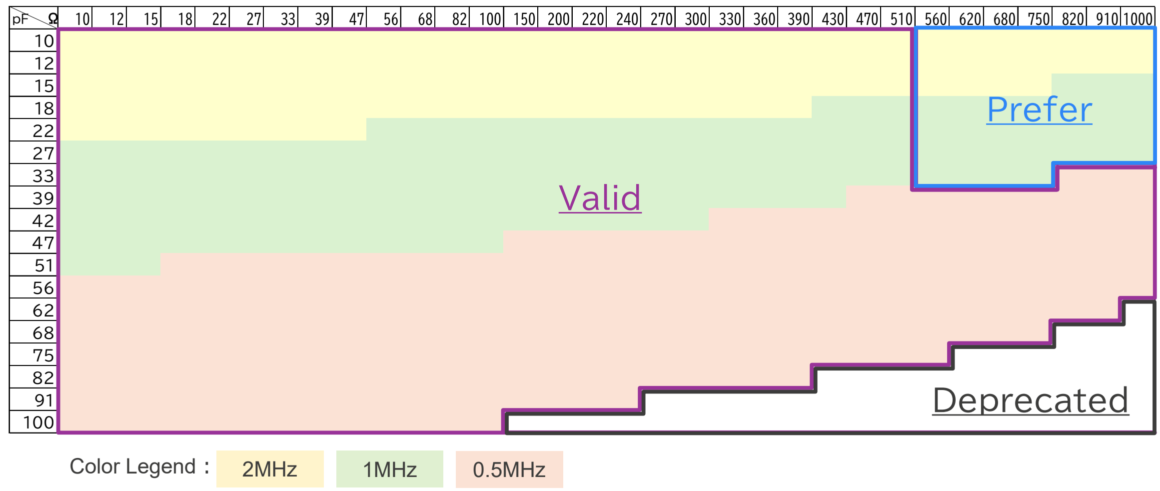


Figure4-7. Relationship between CTSU2 (Low Voltage Operating Mode) Parasitic Capacitance/Damping Resistance and Base Clock Frequency

4.2.2.2 For QE for Capacitive Touch V4.2.0 or later（Only for CTSU2-embedded MCU）

Figure4-8 shows the relationship between the parasitic capacitance/damping resistance in low-voltage mode and the sensor drive pulse frequency set by automatic tuning for the CTSU2 and RX140 (SUCLK 40 MHz upper limit) as a representative of Category E in Table 4-1.

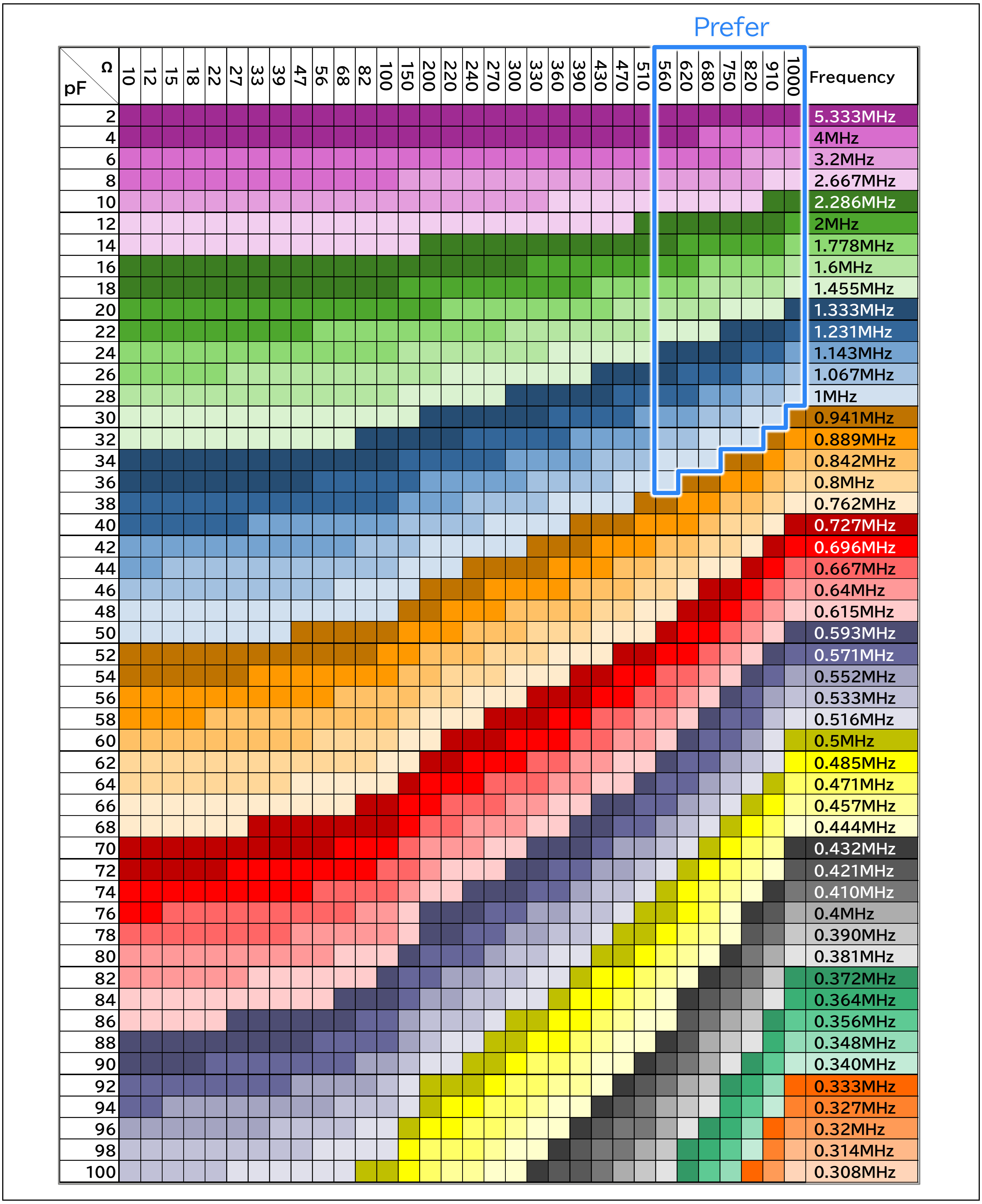


Figure4-8. Relationship Between Parasitic Capacitance/Damping Resistance of CTSU2 and Sensor Drive Pulse Frequency (QE for Capacitive Touch V4.2.0 or Later)

Figure4-9 shows the relationship between the parasitic capacitance/damping resistance in the low-voltage mode of the RL78/G23 (SUCLK 32MHz upper limit) as a representative of Category E in Table 4-1 and the sensor drive pulse frequency set by automatic tuning.

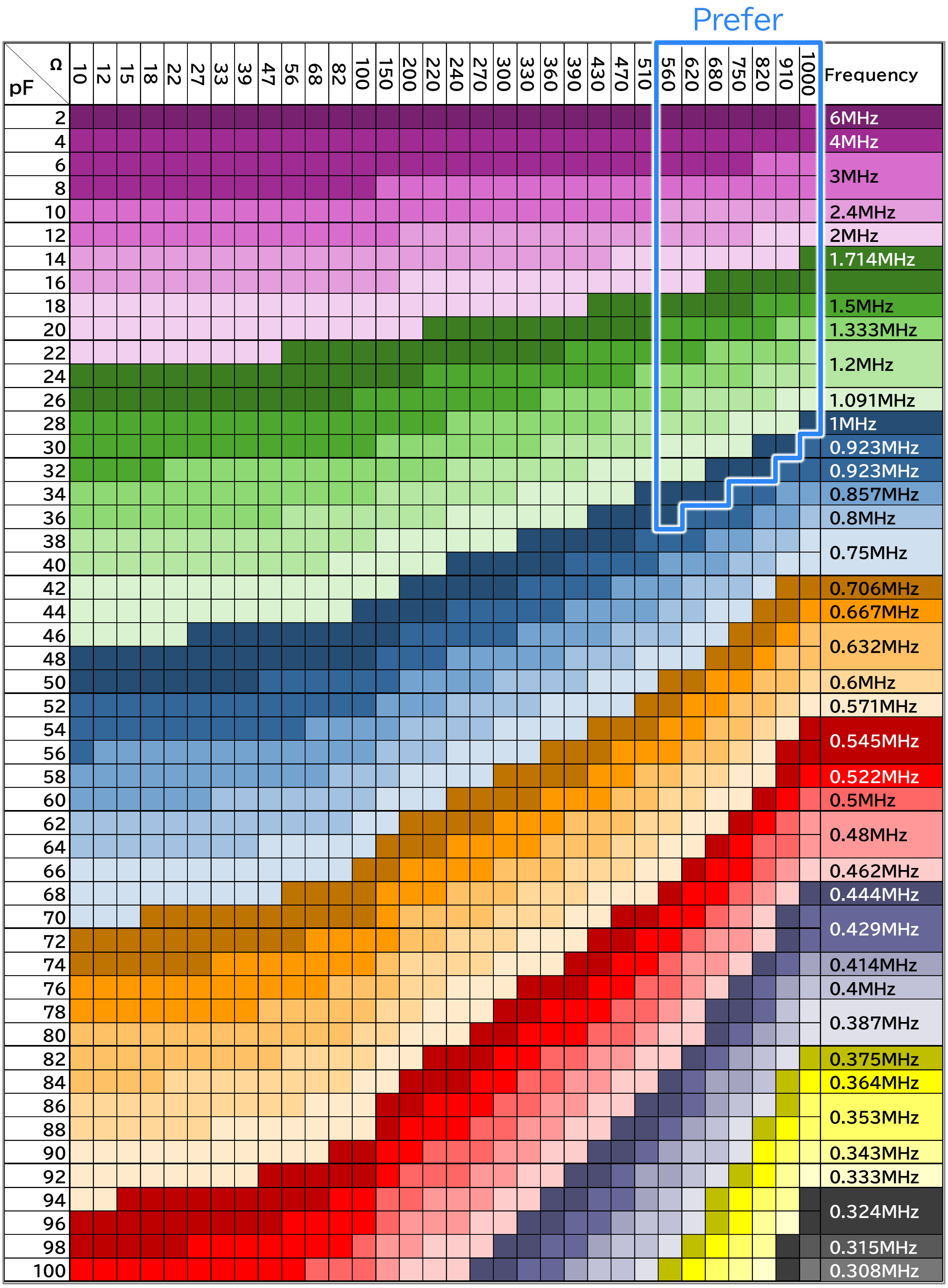


Figure4-9. Relationship Between Parasitic Capacitance/Damping Resistance of CTSU2 and Sensor Drive Pulse Frequency (QE for Capacitive Touch V4.2.0 or Later)

5. Self-capacitance Method Button Patterns and Characteristics Data

The characteristics of capacitive touch buttons vary depending on the combination of various design parameters such as electrode size and wiring pitch. This chapter provides data on how sensitivity is affected when individual design parameters of self-capacitance method buttons are varied. By combining the data for each parameter, you can estimate what risks may occur during board design.

The data provided in this application note does not guarantee the electrical characteristics of each MCU. When designing a board, prototyping and sufficient evaluation should be carried out by the user to determine whether a specific MCU can be used or not.

5.1 Self-capacitance Method Button Sensitivity (SNR)

This section defines button sensitivity based on Signal to Noise Ratio (SNR). Figure 5-1 shows Button Sensitivity (SNR) Derivation Method. The SNR is calculated from the count difference value and noise value when the button is touched and not touched. The measured value is the average of an arbitrary number of samples. In this document, the noise value is ±3σ of the standard deviation of an arbitrary number of samples; the worse of the touch or non-touch measurements is adopted. The noise value may increase or decrease depending on the data acquisition time, so evaluate with sufficient sample acquisition time for better accuracy.

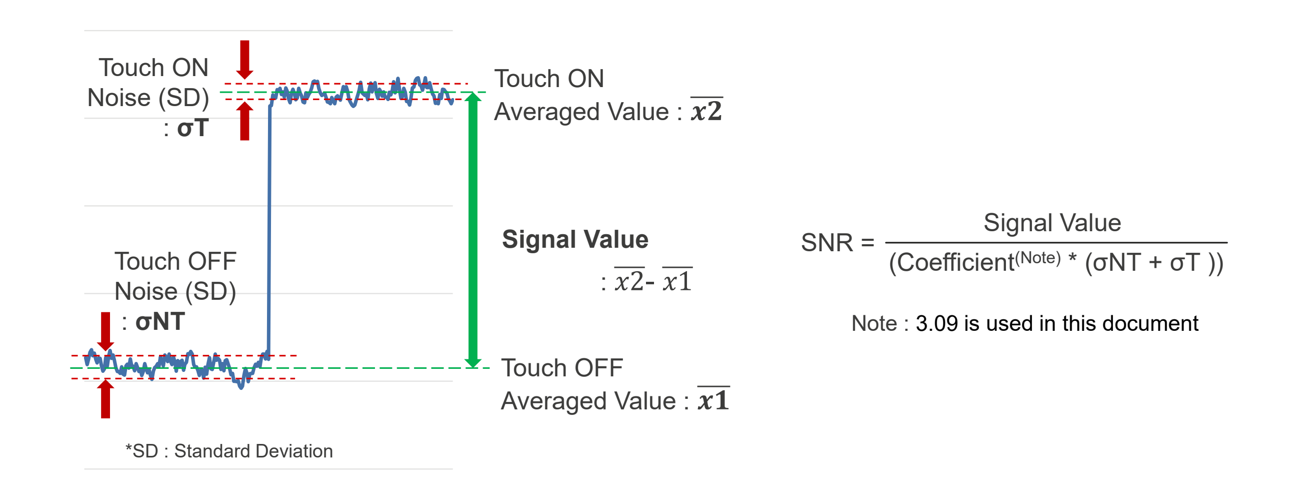


Figure 5-1 Button Sensitivity (SNR) Derivation Method

Table 5-1 lists the measurement results shown in Figure 5-1. When the difference value is 1491 and the noise value (3.09× (σNT+σT)) is 143.96 at the time of button touch, the SNR is 10.35. In this evaluation, the noise value for non-touch is applied because the noise was larger at non-touch.

Table 5-1 Measurement Results of Evaluation Board Pattern Example (Recommended design values, 1 button)

Item	Non-Touch	Touch	Difference
Parasitic capacitance (incl. CPU board)	17.29 pF	17.94 pF	0.65 pF
Parasitic capacitance (evaluation board only)	6.81pF	7.46pF	
Measured value	15379	16870	1491
Noise value	20.50	26.09	—
SNR	**10.35**		

Note: Sensor drive pulse frequency = 2MHz

5.2 Evaluation Conditions

Table 5-2 Hardware Conditions

Item	Specification
CPU board	RA2L1 Cap Touch CPU Board (RTK0EG0018C01001BJ) (RA2L1 Capacitive Touch Evaluation System (RTK0EG0022S01001BJ) accessory)
MCU	RA2L1 (R7FA2L1AB2DFP)
Operating frequency	48MHz
Power supply	5.0V (powered via stabilized power)
Pseudo finger	Φ10.0 x 50mm stainless steel rod

Table 5-3 Software Development Environment

Item	Specification
Integrated development environment	Renesas e² studio Version: 2025-04
Compiler	GCC ARM Embedded 13.2
RA FSP	Version 5.9.0
Development support tool for capacitive method touch sensor	QE for Capacitive Touch V4.1.0
Emulator	Renesas E2 emulator Lite

Table 5-4 Measurement Conditions

Item	Settings
CTSU resistor setting	Use results from automatic adjustment processing of QE for Capacitive Touch (Sensor Drive pulse frequency is determined by automatic adjustment; multi-frequency measurement = 3 times, measurement time = 0.128ms x number of multi-frequency measurements)
Measurement interval	20ms (generated by hardware timer (AGT))
Data acquisition points	1000 points
Data determination method	1000 points averaged
TS pin parasitic capacitance measurement method	Use automatic adjustment process log of QE for Capacitive Touch
Touch determination method (How to Determine Measured Values for Multi-Clock Measurements)	Value Majority Mode(VMM).

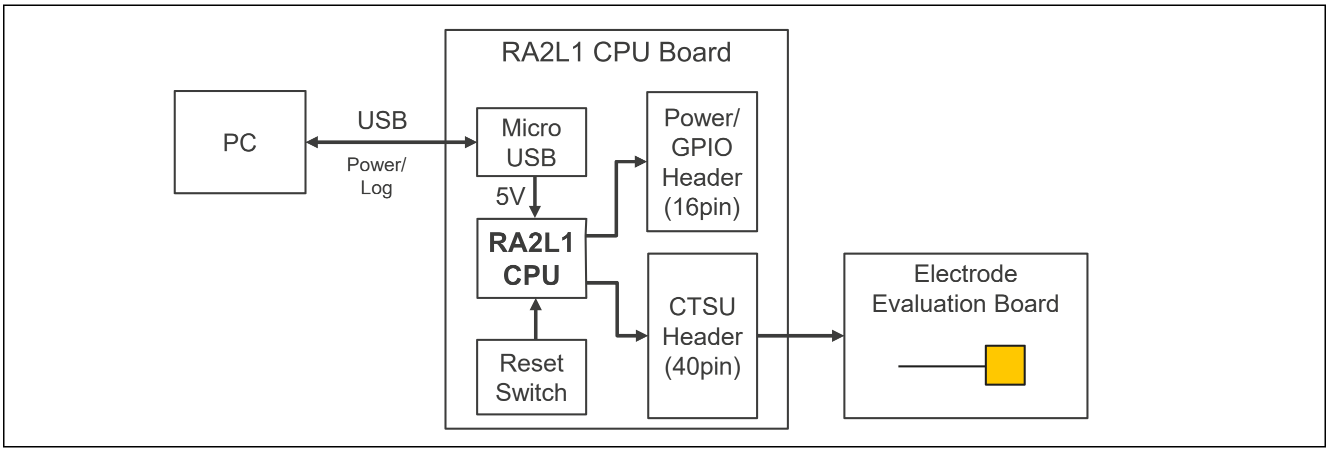
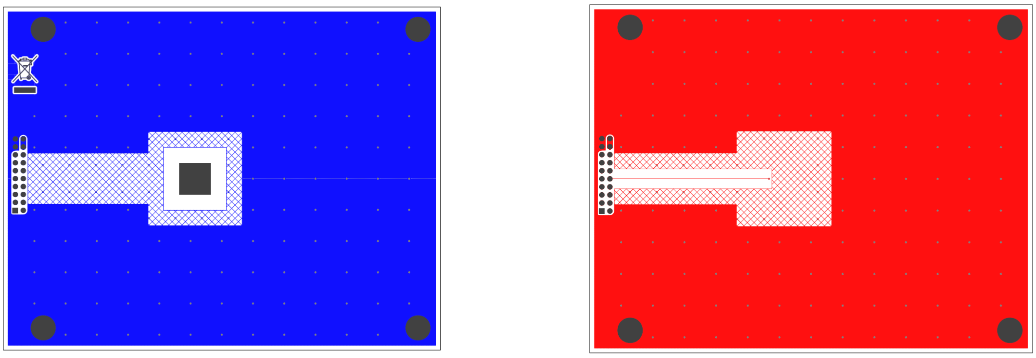


Figure 5-2 Evaluation Board Block Diagram

Table 5-5 shows the recommended electrode design values. Figure 5-3 shows an evaluation board pattern example (recommended design values, 1 button), Figure 5-4 shows an evaluation board pattern example (recommended design values, 3 buttons). The number of buttons is limited for each item to ensure that changes to one parameter do not affect other design parameters.

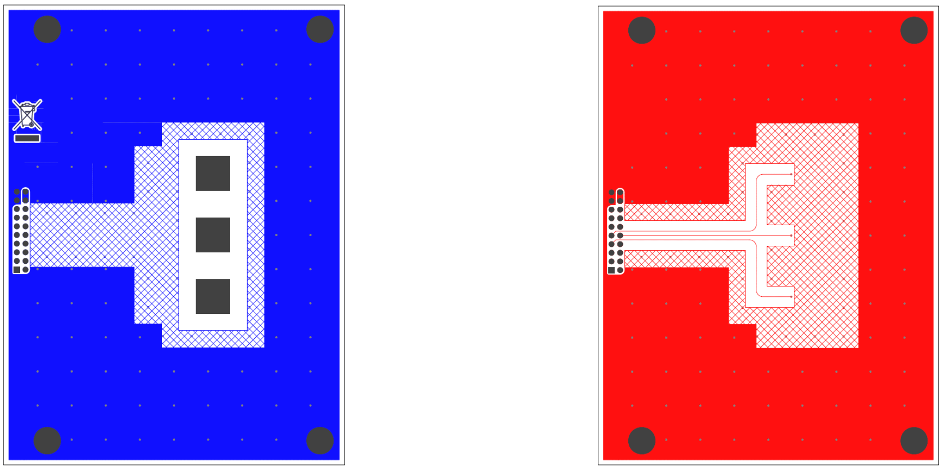
Table 5-5 Recommended Electrode Design Values

Parameter		Specification	Unit	Item in Figure 2-1
Electrode (PAD)				
	Shape	Square or rectangle	-	①
	Size	10x10 to 15x15	mm	②
	Electrode proximity	Electrode size x 0.8	mm	③
	Cross-hatched GND pattern width	5.0	mm	⑦
	Distance between cross-hatched GND shield and electrode	5.0	mm	⑧A
Wiring				
	Wire width	0.15 to 0.20	mm	④
	Wire length	Shortest distance	mm	⑤
	Wiring pitch	1.27	mm	⑥
	Cross-hatched GND pattern width	3.0	mm	⑦
	Distance between cross-hatched GND shield and wiring	5.0	mm	⑧B
Damping resistor		560	Ω	—



(a) Top layer (b) Bottom layer

Figure 5-3 Evaluation Board Pattern Example (recommended design values, 1 button)



(a) Top layer (b) Bottom layer

Figure 5-4 Evaluation Board Pattern Example (recommended design values, 3 buttons)

5.3 Design Parameters and Sensitivity Characteristics

This section provides examples of design parameters and sensitivity characteristics as well as the symbols used as abbreviations in the graphs showing various evaluation results. Table 5-6 lists Symbols Used in Graphs. Table 5-7 lists the Board Specifications used for evaluation.

Table 5-6 Symbols Used in Graphs

Symbol	Description
★	Electrode board with recommended design values
Difference	Difference between button touch and non-touch
L	Wiring length
$f_{0.5}$	Sensor drive pulse frequency = 0.5MHz
$f_{1.0}$	Sensor drive pulse frequency = 1.0MHz
$f_{2.0}$	Sensor drive pulse frequency = 2.0MHz
$f_{4.0}$	Sensor drive pulse frequency = 4.0MHz

Table 5-7 Board Specifications

Item	Specification
Board thickness	1.6mm
Material	FR-4
Number of layers	2 or 4 layers

5.3.1 Electrode Size

Table 5-8 shows the Board Specifications for Electrode Size Variation. For evaluation purposes, only the electrode size was varied; all other design parameters remained fixed.

Table 5-8 Board Specifications for Electrode Size Variation

Design Parameter	Specification	Unit	Notes
Electrode size	**5.0x5.0, 10x10 30x30, 50x50**	**mm**	**Square**
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

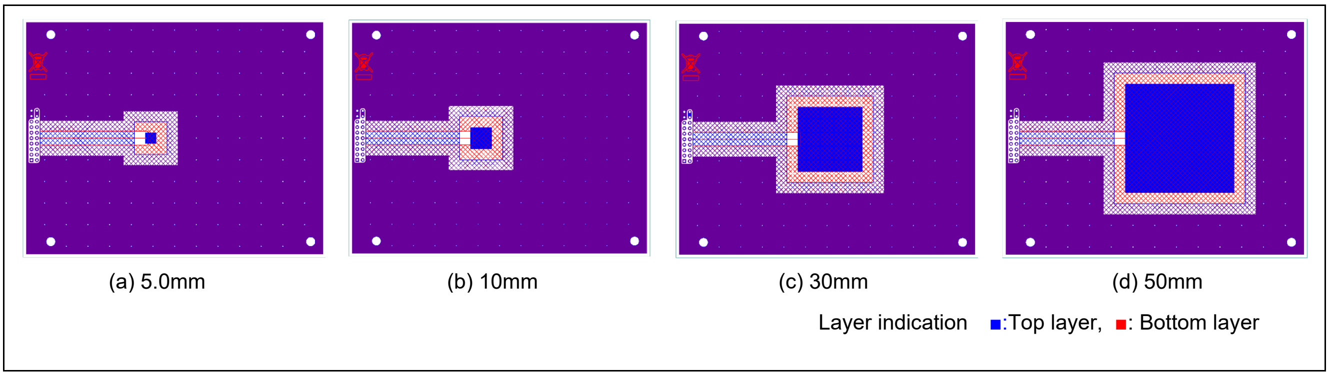


Figure 5-5 Evaluation Board Patterns (electrode sizes)

Figure 5-6 shows Electrode Size and Sensitivity. Parasitic capacitance includes the approximate 10.48 pF parasitic capacitance of the CPU board.

- The parasitic capacitance of the electrode increases in accordance with the area ratio. Because a fixed amount of parasitic capacitance from elements like GND shields and connectors is always present, the total parasitic capacitance does not scale directly with electrode-area ratio and increases by a smaller amount.
- CTSU measured capacitance at touch increases in proportion to the electrode size. Parasitic capacitance is generated between the side of the finger and the electrode in addition to the area of the finger that is in direct contact with the electrode.
- SNR at touch decreases as electrode size increases. The sensor drive pulse frequency decreases depending on the total parasitic capacitance of the electrode circuit, which also causes the SNR to decrease.

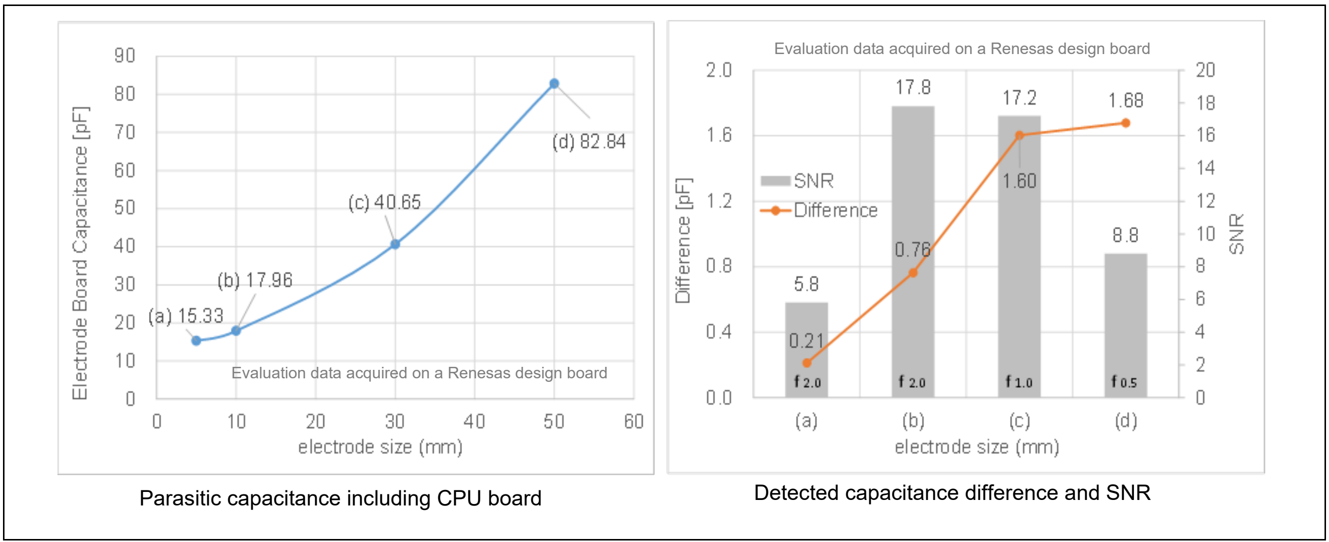


Figure 5-6 Electrode Size and Sensitivity Characteristics

5.3.2 Wiring Length

Table 5-9 lists Board Specifications for Wiring Length Variations, and Table 5-10 lists Combined Shield Conditions. For evaluation purposes, only the wiring length was varied; all other design parameters remained fixed. The effects on sensitivity with different GND patterns are also noted.

Table 5-9 Board Specifications for Wiring Length Variations

Design Parameter	Specification	Unit	Note
Wiring length	**50, 300, 600**	**mm**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	
GND shield pattern design	Cross-hatched or solid	-	

Note: Recommended design values shown in Table 5-5, except as noted.

Table 5-10 Combined Shield Conditions

Label Name	Cross-hatched pattern	Wiring-Shield Distance	Electrode-Shield Distance
COND1	Cross-hatched/3.0/5.0	3.0mm	5.0mm
COND2	Cross-hatched /0.5/0.5	0.5mm	0.5mm
COND3 Note: GND pattern directly under the electrode is not included.	Solid/0.5/0.5	0.5mm	0.5mm

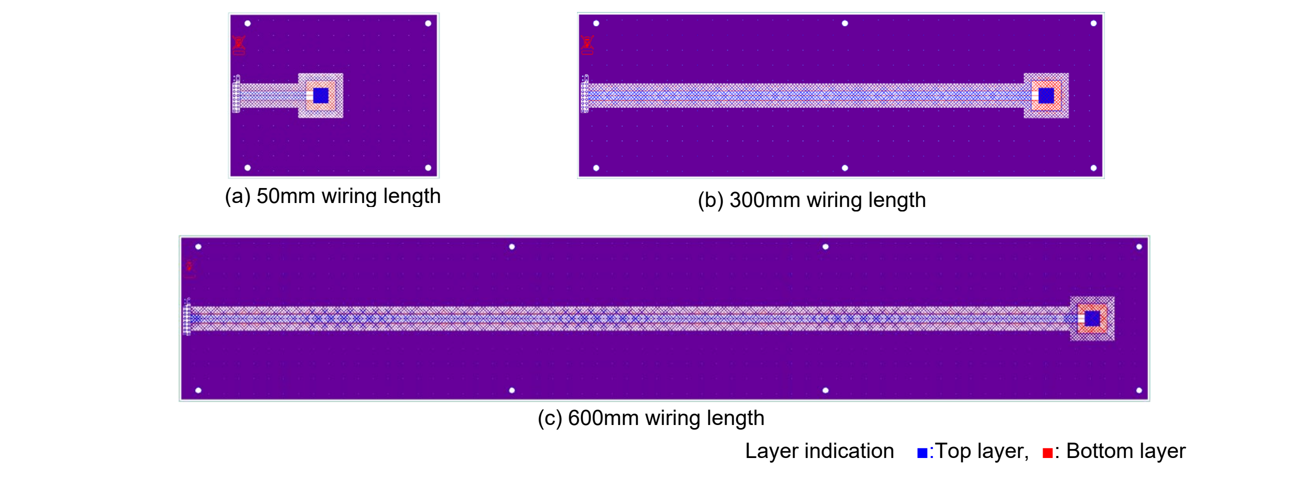


Figure 5-7 Evaluation Board Pattern (COND1)

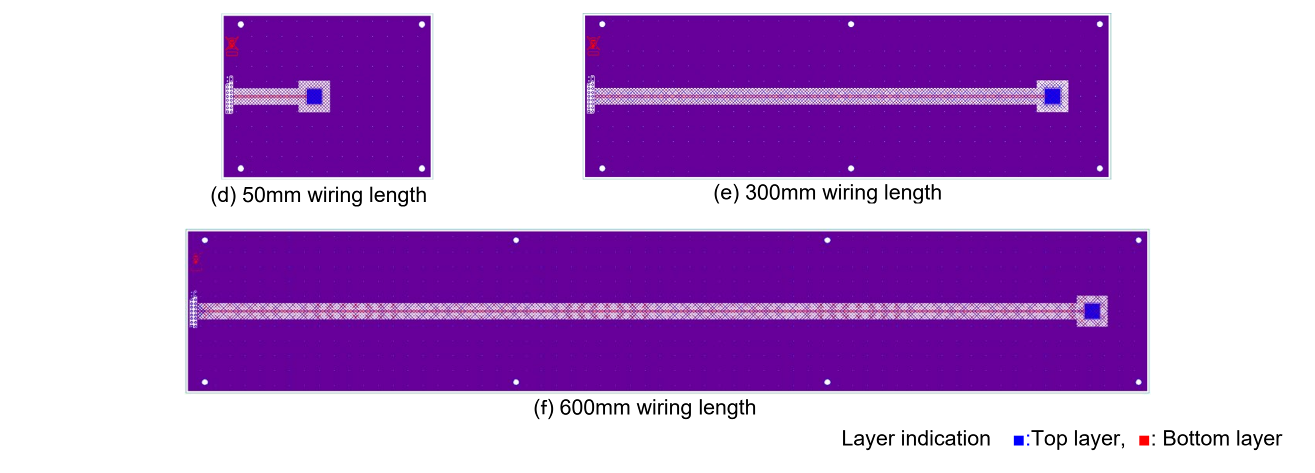


Figure 5-8 Evaluation Board Pattern (COND2)

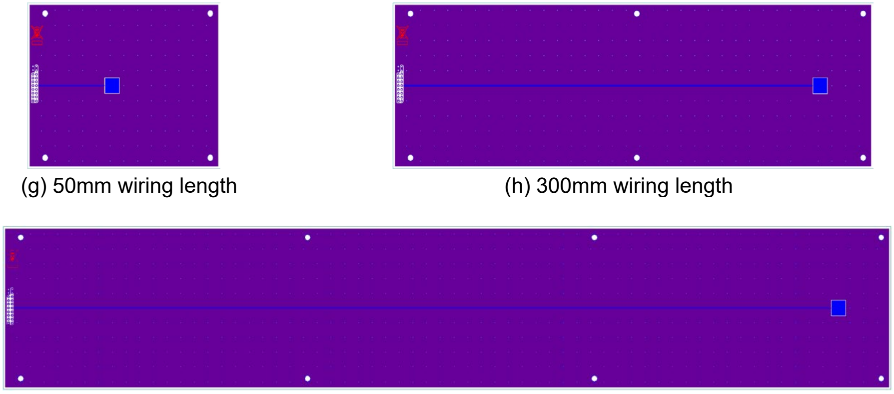
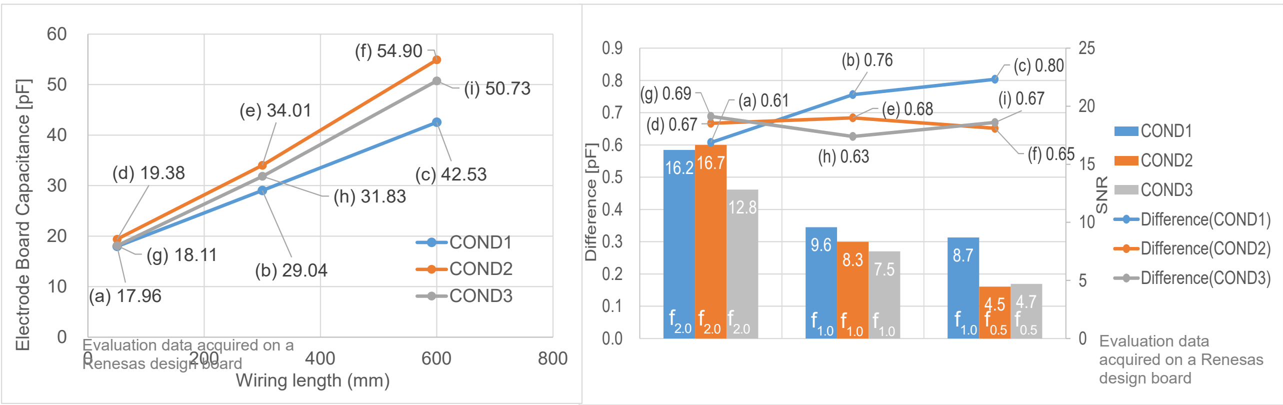


Figure 5-9 Evaluation Board Pattern (COND3)

Figure 5-10 shows Wiring Length and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF. Parasitic capacitance increases in proportion to the wiring length.

- The closer the GND shield is to the electrode and the wiring, the more the parasitic capacitance increases.
- The amount of parasitic capacitance increase at button touch is detected as a constant value regardless of the wiring length.
- The SNR at button touch is lower with longer wiring lengths. As the sensor drive pulse frequency decreases based on the total parasitic capacitance of the electrode circuit, the SNR also decreases.



Parasitic capacitance including CPU board

Detected capacitance difference and SNR

Figure 5-10 Wiring Length and Sensitivity Characteristics

5.3.3 Multiple Button Design

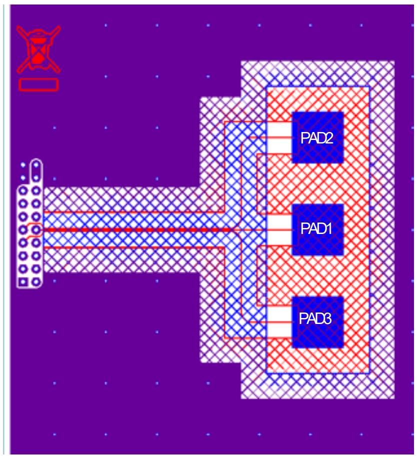
5.3.3.1 Wiring Pitch

Table 5-11 lists the Board Specifications for Wiring Pitch Variations. For evaluation purposes, only the wiring pitch and length was varied; all other design parameters remained fixed.

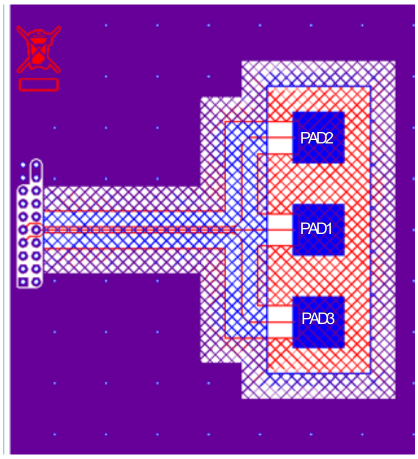
Table 5-11 Board Specifications for Wiring Pitch Variations

Design Parameter	Specification	Unit	Notes
Wiring pitch	**0.3, 0.5, 1.27, 2.54**	**mm**	
Wiring length	50, 300	mm	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

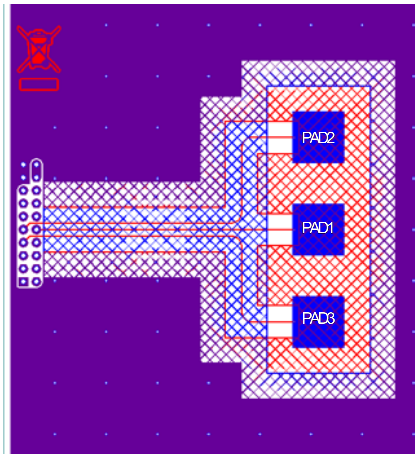
Note: Recommended design values shown in Table 5-5, except as noted.



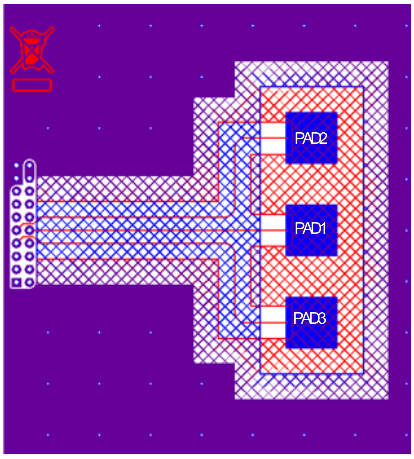
(a) 0.3mm wiring pitch



(b) 0.5mm wiring pitch



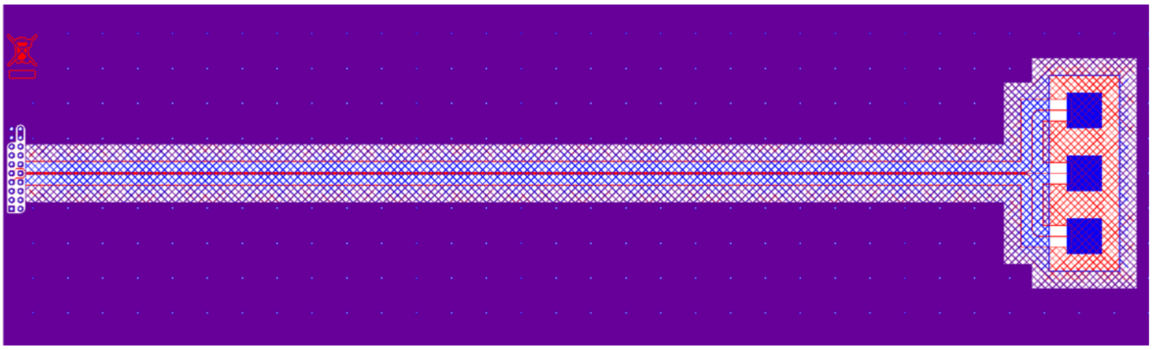
(c) 1.27mm wiring pitch



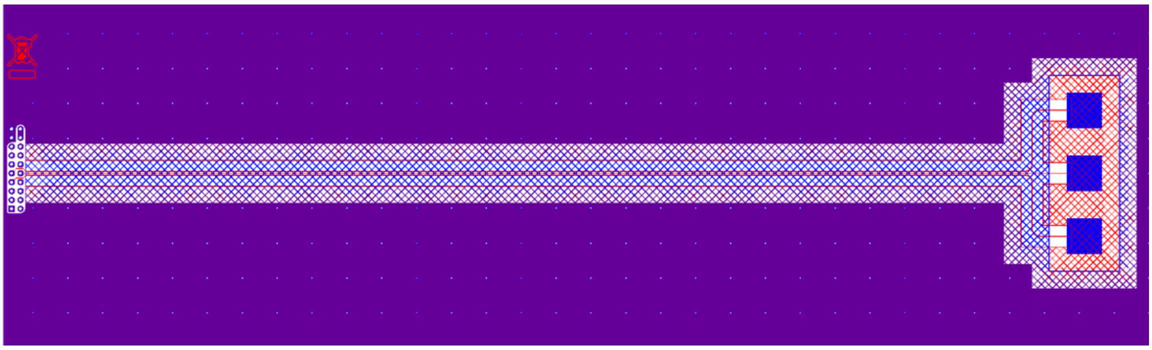
(d) 2.54mm wiring pitch

Layer indication ■:Top layer, ■: Bottom layer

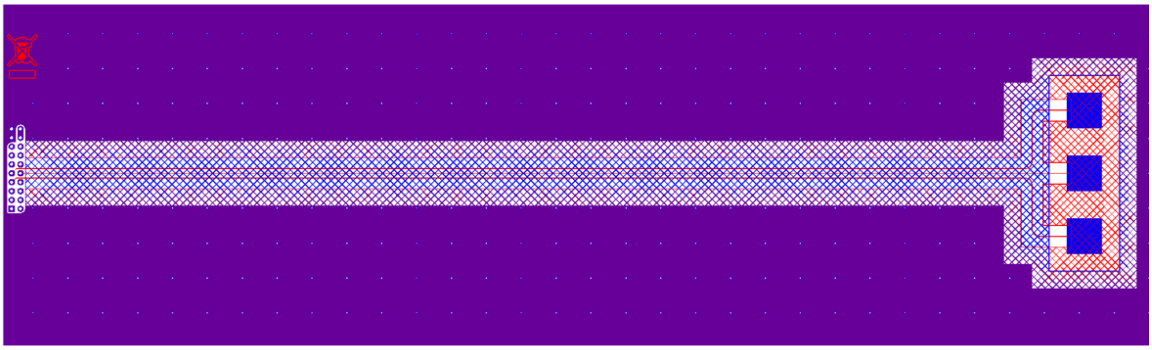
Figure 5-11 Evaluation Board Pattern (wiring length = 50mm)



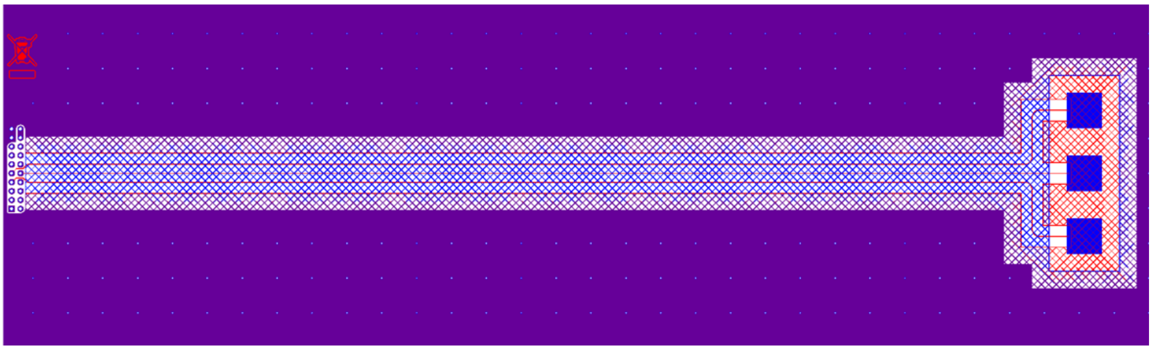
(e) 0.3mm wiring pitch



(f) 0.5mm wiring pitch



(g) 1.27mm wiring pitch



(h) 2.54mm wiring pitch

Layer indication ■:Top layer, ■: Bottom layer

Figure 5-12 Evaluation Board Pattern (wiring length = 300mm)

Figure 5-13 shows Wiring Pitch and Parasitic Capacitance (incl. CPU board) and Figure 5-14 shows Wiring Pitch and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The narrower the wiring pitch, the more the parasitic capacitance increases.
- The amount of parasitic capacitance at button touch is detected as a constant value regardless of the wiring pitch.
- When wiring is on both sides of the electrode, as in PAD1, the SNR at touch is lower because the wiring pitch is narrower. As the sensor drive pulse frequency decreases based on the total parasitic capacitance of the electrode circuit, the SNR also decreases. When wiring is only on one side and it is on the outer side of the wiring group, the SNR is constant regardless of the wiring pitch. The SNR of the wiring on the outer side of the wiring group changes depending on the distance to the GND shield.

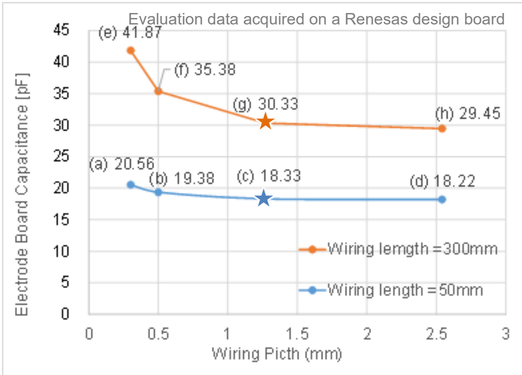


Figure 5-13 Wiring Pitch and Parasitic Capacitance (incl. CPU board)

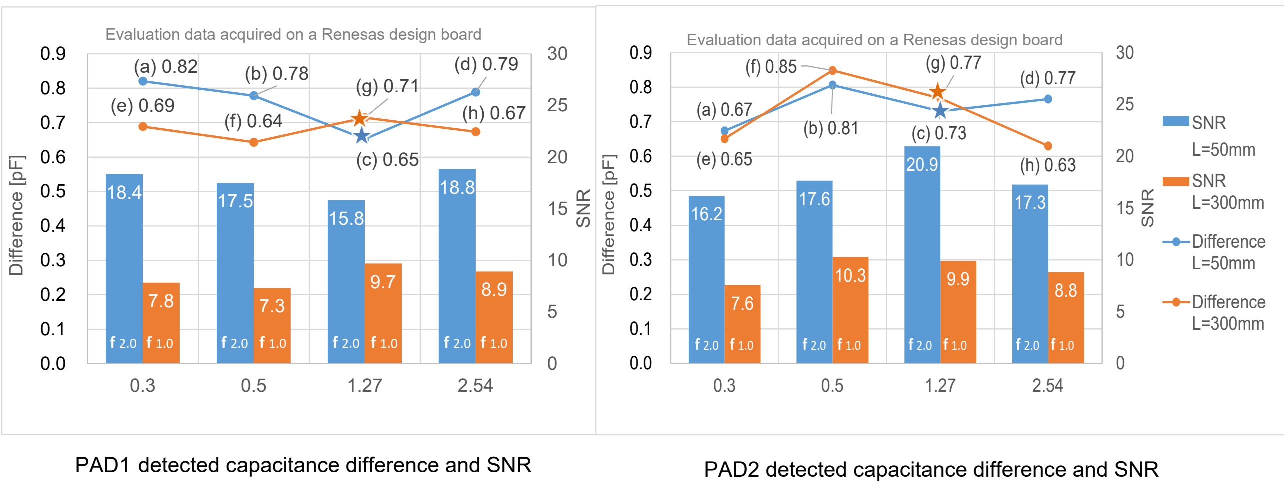


Figure 5-14 Wiring Pitch and Sensitivity Characteristics

5.3.3.2 Distance between Button Electrodes

The following indicates the sensitivity characteristics based on the distance between button electrodes. For evaluation purposes, only the distance between button electrodes was varied; all other design parameters remained fixed.

Table 5-12 Board Specifications for Variations of Distance Between Button Electrodes

Design Parameter	Specification	Unit	Notes
Distance between button electrodes	**3.0, 8.0, 10.0, 15.0**	**mm**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

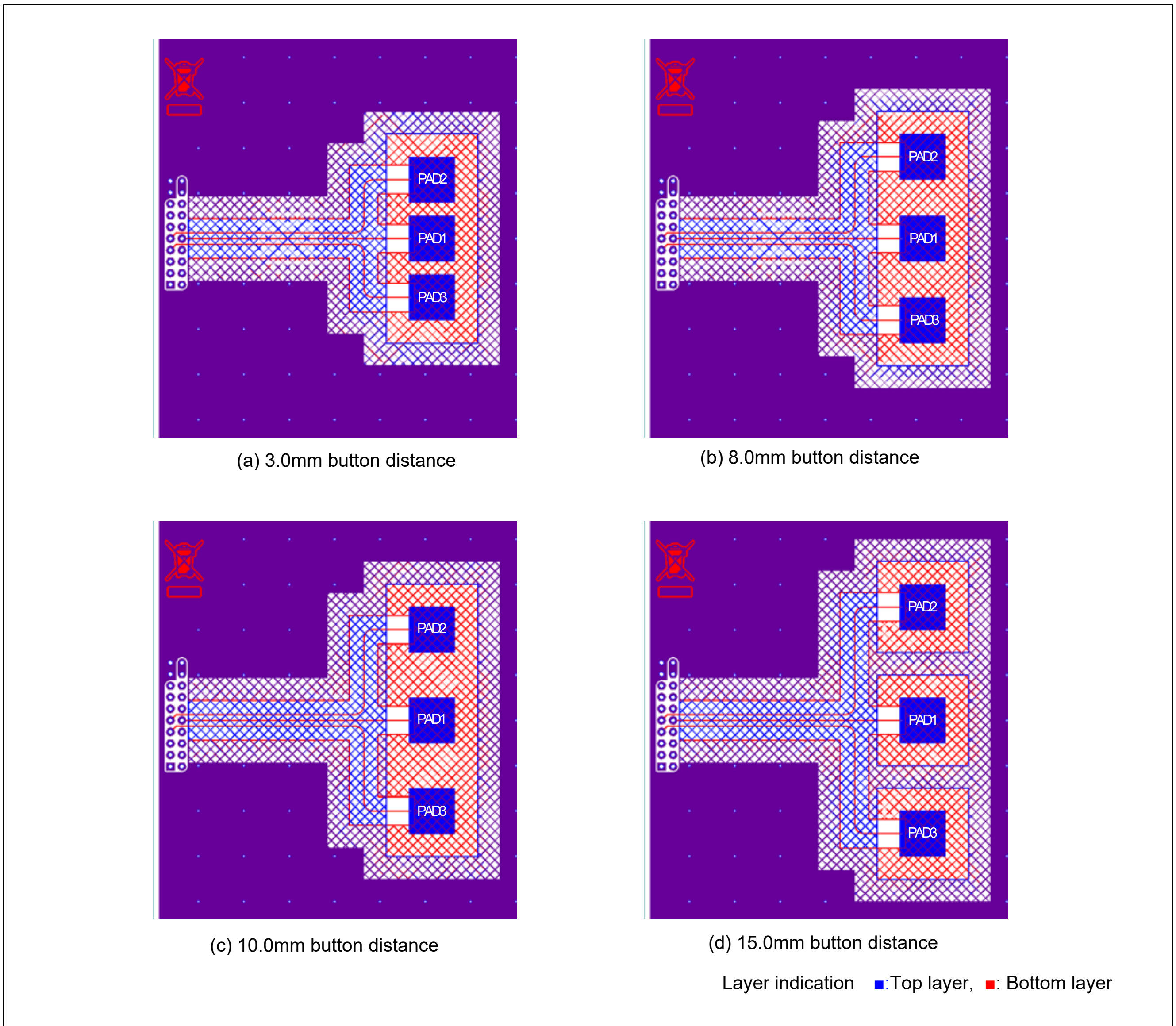
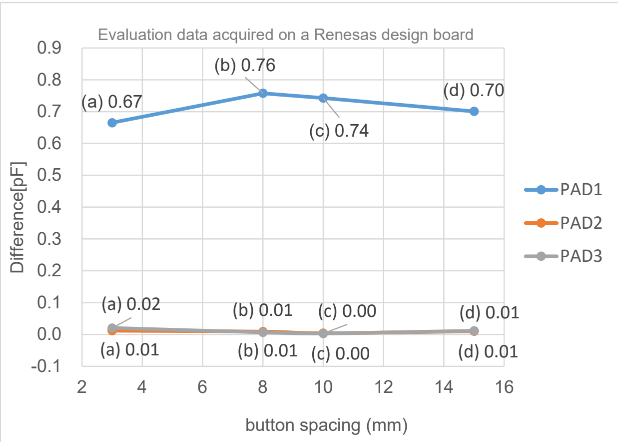


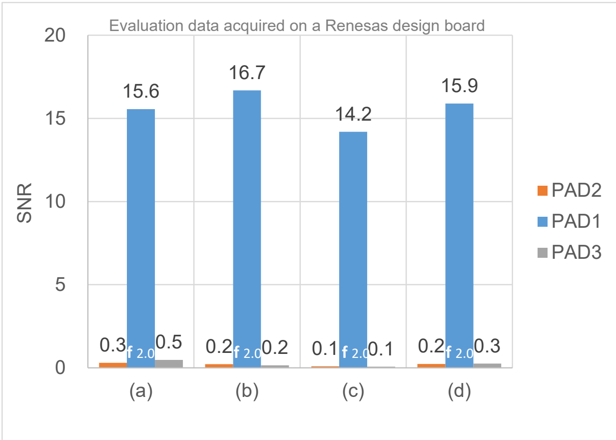
Figure 5-15 Evaluation Board Pattern (distance between button electrodes)

Figure 5-16 shows the Distance Between Button Electrodes and Sensitivity.

- With an Overlay panel thickness of 2.0mm, even a narrow distance between button electrodes of 3.0mm will not cause the SNR of the target button to decrease nor will it cause false detection by neighboring buttons.



Parasitic capacitance including CPU



Detected capacitance difference and SNR

Figure 5-16 Distance Between Button Electrodes and Sensitivity Characteristics

5.3.4 GND Pattern Design

This section focuses on the effect of GND patterns on electrode characteristics. In this document, “shield” refers to a GND pattern that is located on the same layer of the board as the touch electrode and wiring and adjacent to both.

5.3.4.1 Electrode and Shield Distance

Table 5-13 lists Board Specifications for Electrode and Shield Distance Variations. Electrode shield proximity indicates the distance between the electrode and the GND shield. Either a cross-hatched GND pattern or solid GND pattern was used for the shield. For evaluation purposes, only the distance between the electrode and shield, as well as the distance between wiring and shield, were varied; all other design parameters remained fixed.

Table 5-13 Board Specifications for Electrode and Shield Distance Variations

Design Parameter	Specification	Unit	Notes
Shield type	**Hatched GND or solid GND**	**-**	
Distance between electrode and shield	**0.5, 1.0, 3.0, 5.0**	**mm**	
Distance between wiring and shield	3.0	mm	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

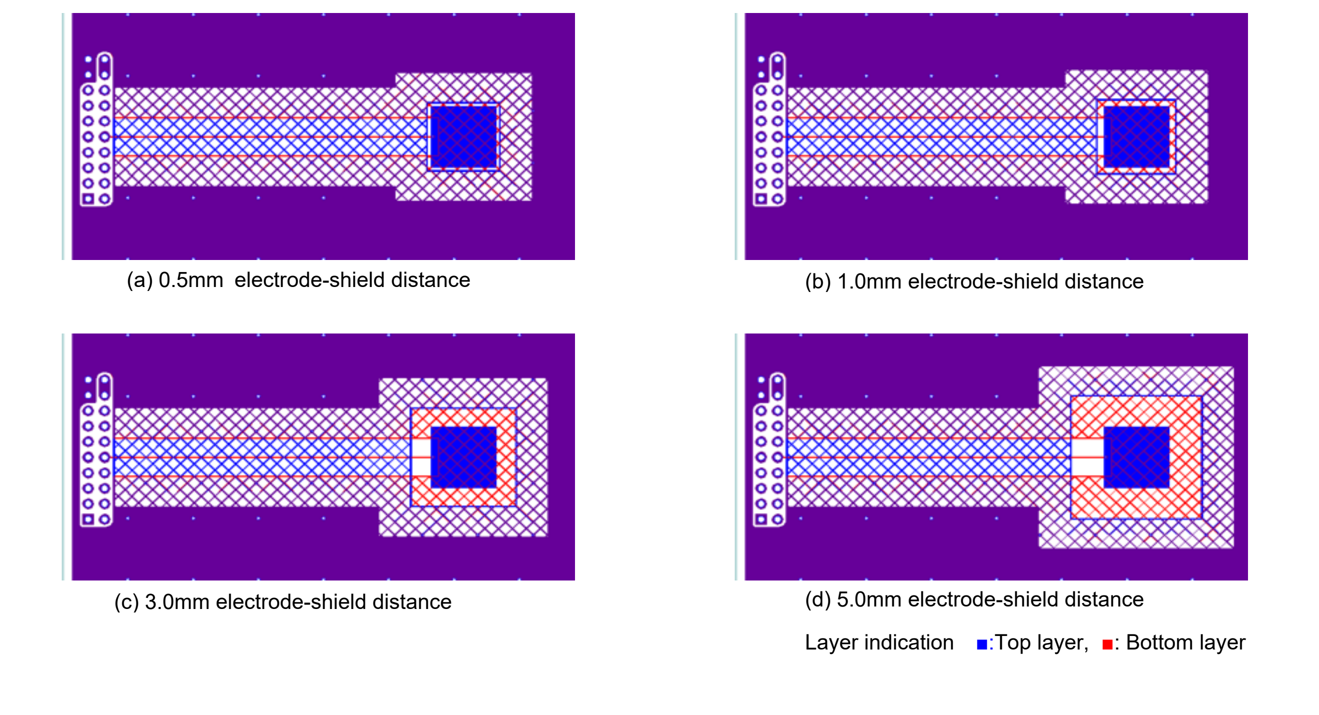
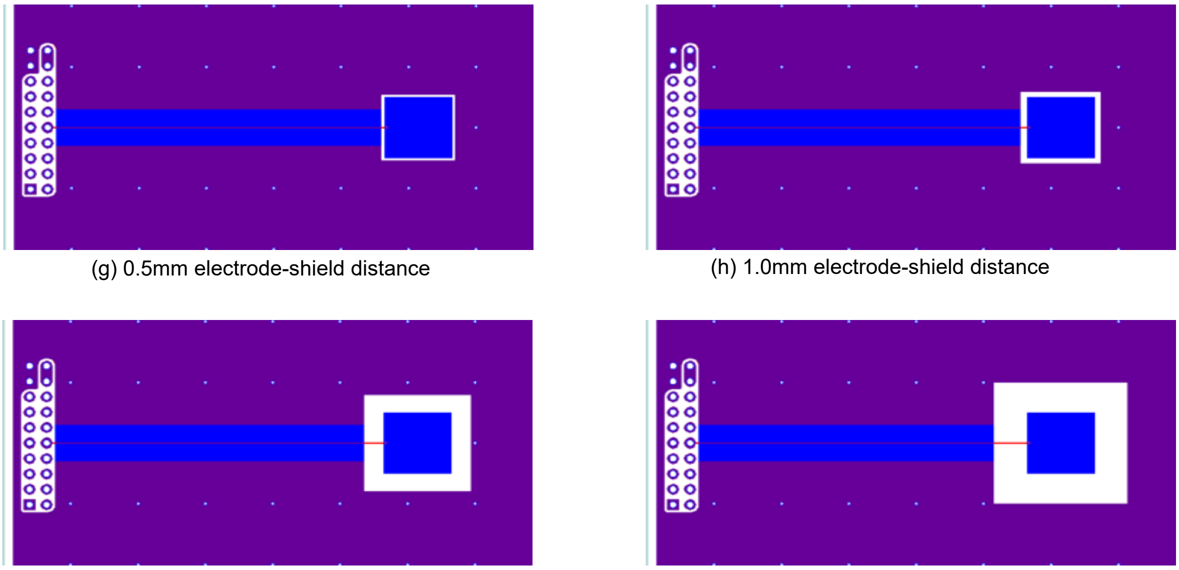


Figure 5-17 Evaluation Board Pattern (cross-hatched GND, only electrode-shield distance varied)



(g) 0.5mm electrode-shield distance

(h) 1.0mm electrode-shield distance

(i) 3.0mm electrode-shield distance

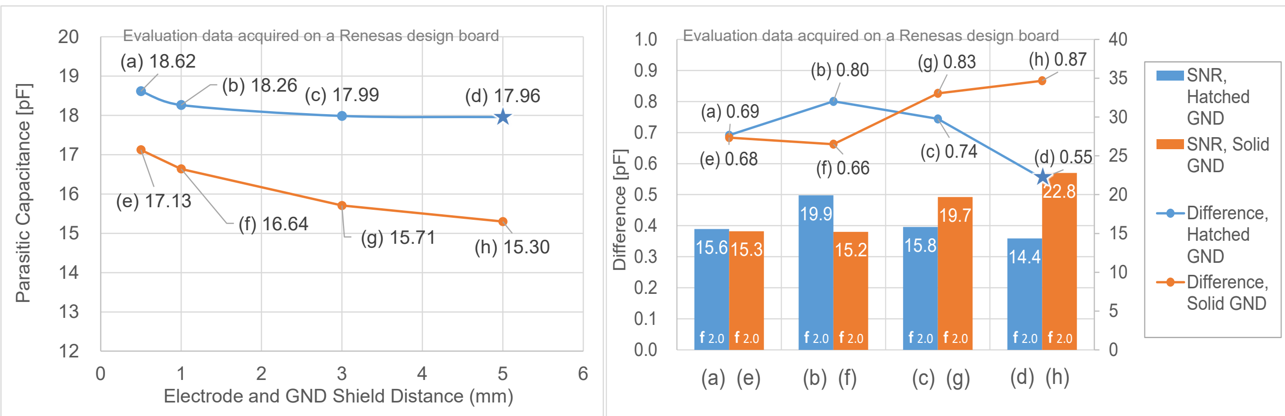
(j) 5.0mm electrode-shield distance

Layer indication ■:Top layer, ■: Bottom layer

Figure 5-18 Evaluation Board Pattern (only solid GND and electrode-shield distance varied)

Figure 5-19 lists Electrode-Shield Distance and Sensitivity . Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF. Note that the parasitic capacitance of boards using a solid GND shield pattern is smaller than those using a cross-hatched GND pattern due to the lack of solid GND pattern directly under the electrode.

- The shorter the distance between the electrode and the GND shield, the more the parasitic capacitance increases. Cross-hatched GND shields generate a smaller increase in parasitic capacitance than do solid GND shields, even with a shorter distance.
- The shorter the distance between the electrode and the GND shield, the smaller the detected capacitance difference.
- The shorter the distance between the electrode and the GND shield, the more the SNR tends to decrease.



Parasitic capacitance including CPU board

Detected capacitance difference and SNR

Figure 5-19 Electrode-Shield Distance and Sensitivity Characteristics

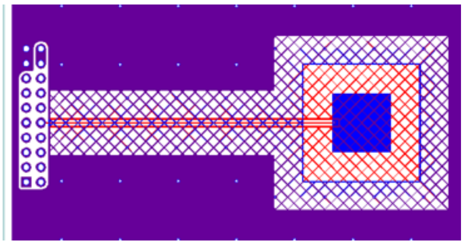
5.3.4.2 Distance between Wiring and Shield

Table 5-14 lists Board Specifications for Wiring-Shield Distance Variations. The wiring-shield distance indicates the distance between the wiring and the GND shield. Either a cross-hatched GND pattern or solid GND pattern was used for the shield. For evaluation purposes, only the distance between wiring and shield was varied; all other design parameters remained fixed.

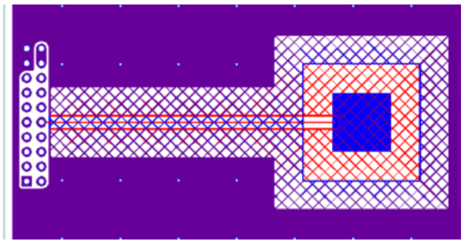
Table 5-14 Board Specifications for Wiring-Shield Distance Variations

Design Parameter	Specification	Unit	Notes
Shield type	**Cross-hatched GND, solid GND**	**-**	
Distance between wiring and shield	**0.5, 1.0, 3.0, 5.0**	**mm**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

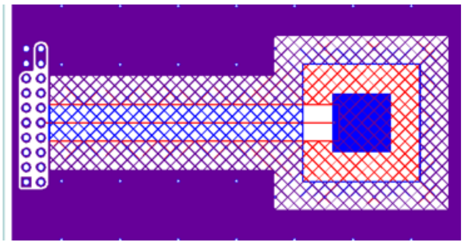
Note: Recommended design values shown in Table 5-5, except as noted.



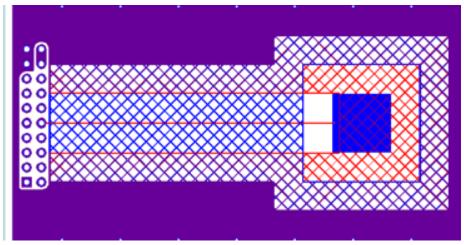
(a) 0.5mm wiring- shield distance



(b) 1.0mm wiring-shield distance



(c) 3.0mm wiring-shield distance



(d) 5.0mm wiring-shield distance

Layer indication ■:Top layer, ■: Bottom layer

Figure 5-20 Evaluation Board Pattern (cross-hatched GND)

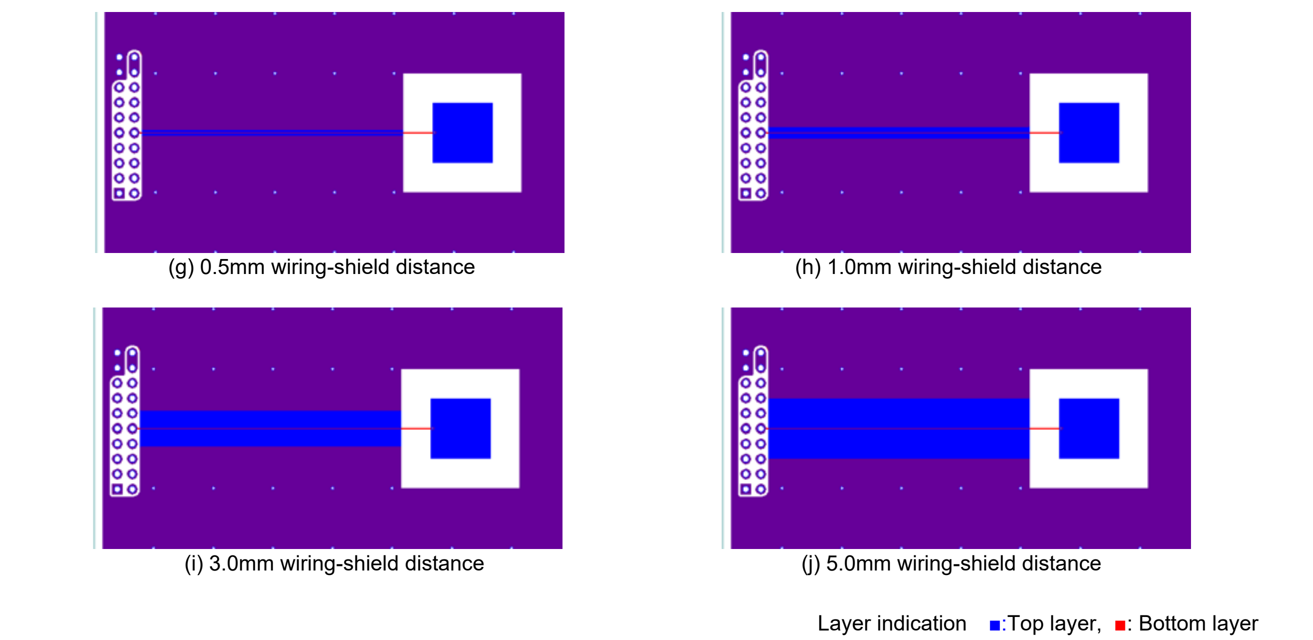


Figure 5-21 Evaluation Board Pattern (solid GND)

Figure 5-22 shows Wiring-Shield Distance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF. Note that the parasitic capacitance of boards using a solid GND shield pattern is smaller than those using a cross-hatched GND pattern due to the lack of solid GND pattern directly under the electrode.

- The shorter the distance between the wiring and the GND shield, the more the parasitic capacitance increases.
- The shorter the distance between the wiring and the GND shield, the smaller the detected capacitance difference.
- The shorter the distance between the wiring and the GND shield, the more the SNR tends to decrease.

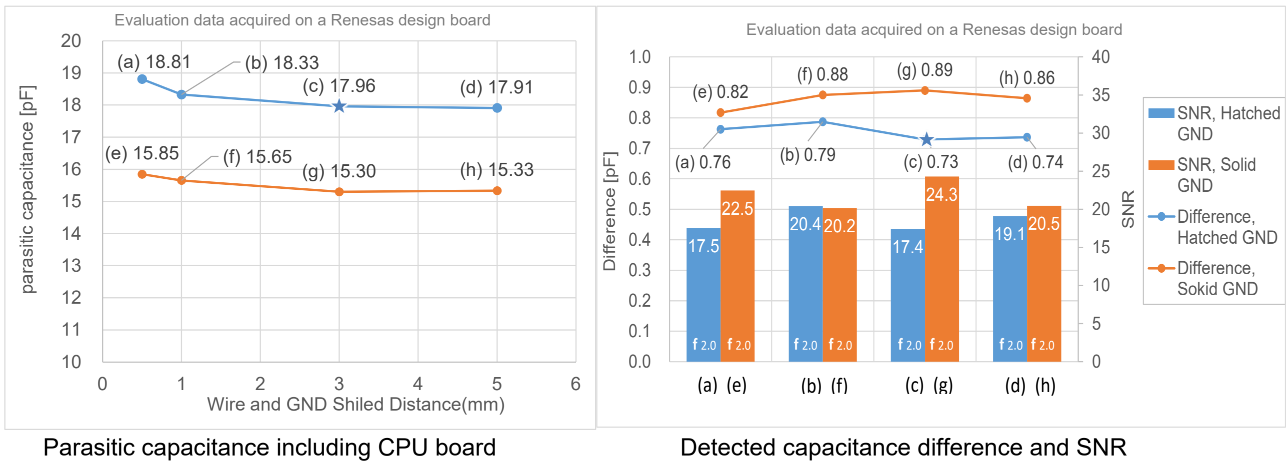


Figure 5-22 Wiring-Shield Distance and Sensitivity Characteristics

5.3.4.3 Effect of Inner Layer GND

Table 5-15 lists Board Specifications With/Without Inner Layer GND. For evaluation purposes, only the inner shield hierarchy on the multi-layered board was varied; all other design parameters remained fixed. The effect on sensitivity due to different shield types is also included. Note that use of a solid patten requires removing the pattern directly under the electrode.

Table 5-15 Board Specifications With/Without Inner Layer GND

Design Parameter	Specification	Unit	Notes
Inner shield layers	**L2, L3, none**	**-**	**L4 can be applied under all conditions**
Shield type	**Cross-hatched GND, solid GND**	**-**	**Solid GND does not include a pattern directly under the electrode**
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

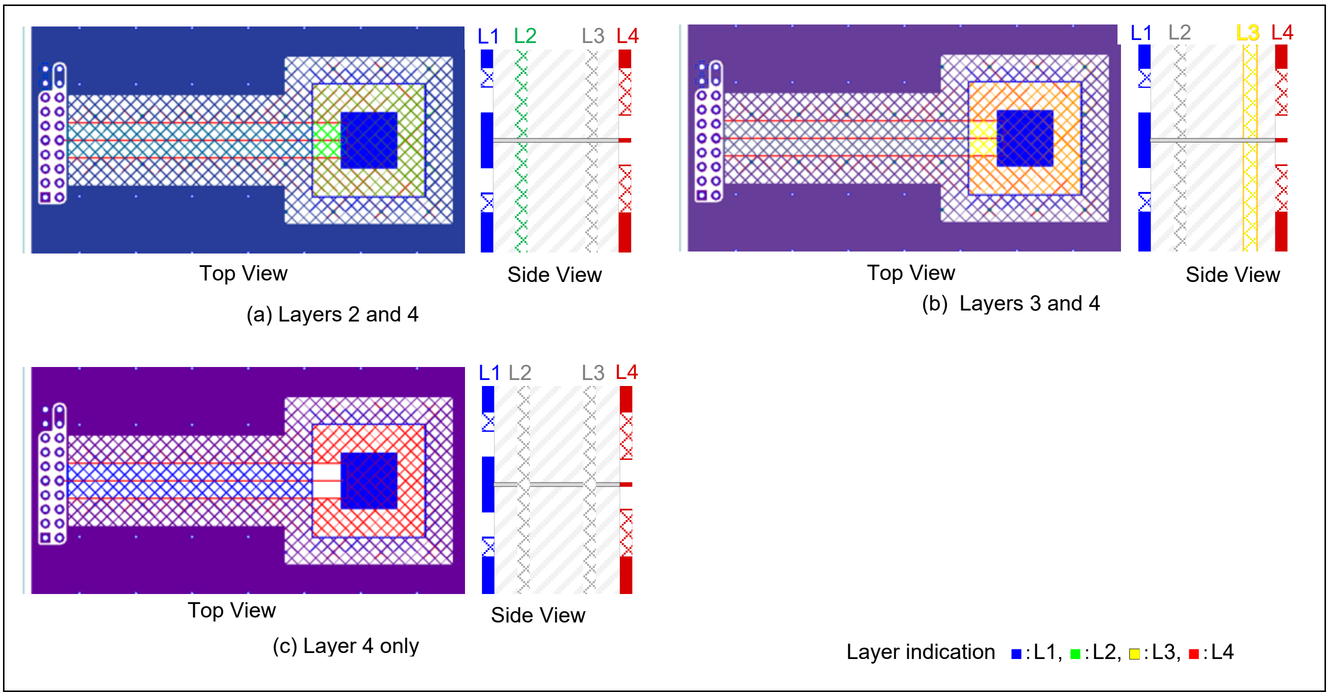


Figure 5-23 Evaluation Board Pattern (cross-hatched GND)

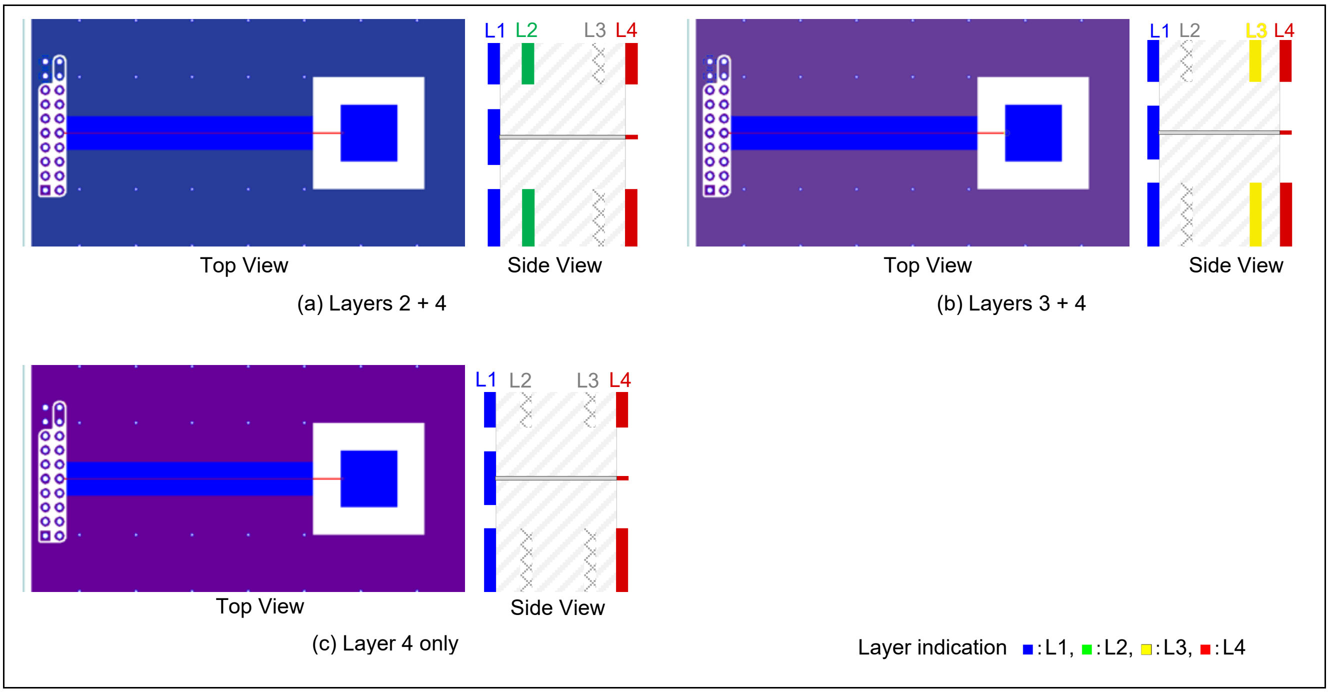
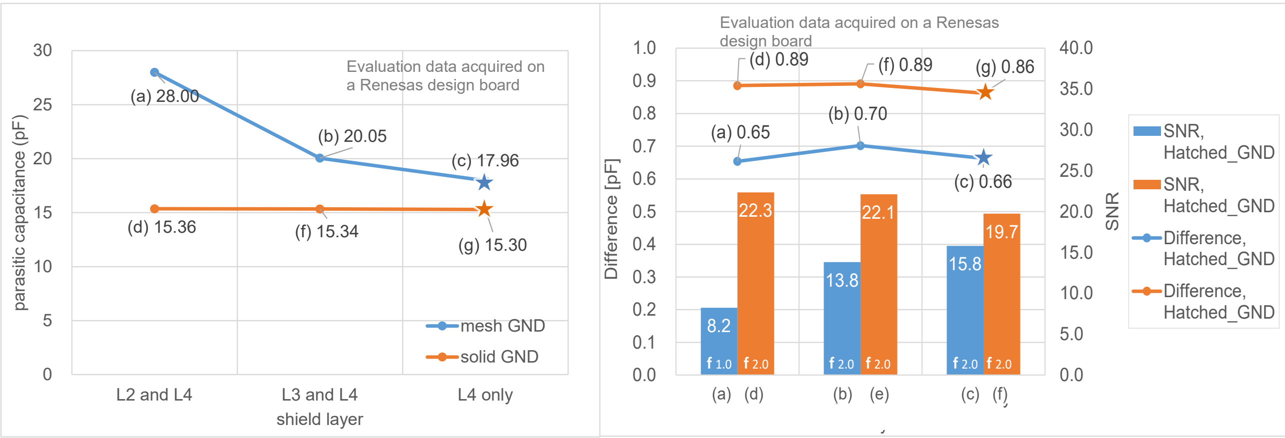


Figure 5-24 Evaluation Board Pattern (solid GND)

Figure 5-25 shows Inner Layer GND and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- When a shield is placed directly under the electrode, the closer the inner layer GND and the electrode are, the more the parasitic capacitance increases. Take caution as parasitic capacitance will increase even when a cross-hatched pattern is placed directly beneath the electrode. There is no increase in parasitic capacitance with a solid pattern because the pattern directly below the electrode is removed.
- The detected capacitance difference is constant, regardless of the shield level.
- The closer the inner layer GND is to the electrode, the lower the SNR. Placing the GND shield on an inner layer increases the total parasitic capacitance and lowers the sensor drive pulse frequency, which tends to lower the SNR.



Parasitic capacitance including CPU board
Detected capacitance difference and SNR

Figure 5-25 Inner Layer GND and Sensitivity Characteristics

5.3.4.4 Cross-hatched Shield Pattern Width

Table 5-16 lists Board Specifications for Cross-hatched Shield Pattern Width Variations. For evaluation purposes, only the cross-hatched shield pattern width and the distance between the cross-hatched shield and electrodes/wiring were varied; all other design parameters remained fixed.

Table 5-16 Board Specifications for Cross-hatched Shield Pattern Width Variations

Design Parameter	Specification	Unit	Notes
Cross-hatched shield pattern width (electrode periphery and wiring periphery)	**1.0, 3.0, 5.0, 10.0**	**mm**	
Distance between electrode and shield	**0.5, 1.0, 5.0**	**mm**	
Distance between wiring and shield	**0.5, 1.0, 3.0**	**mm**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	
Combined shield conditions (wiring-shield distance/ electrode-shield distance)			
COND1	3.0/5.0	mm	Recommended design values
COND2	1.0/1.0	mm	
COND3	0.5/0.5	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

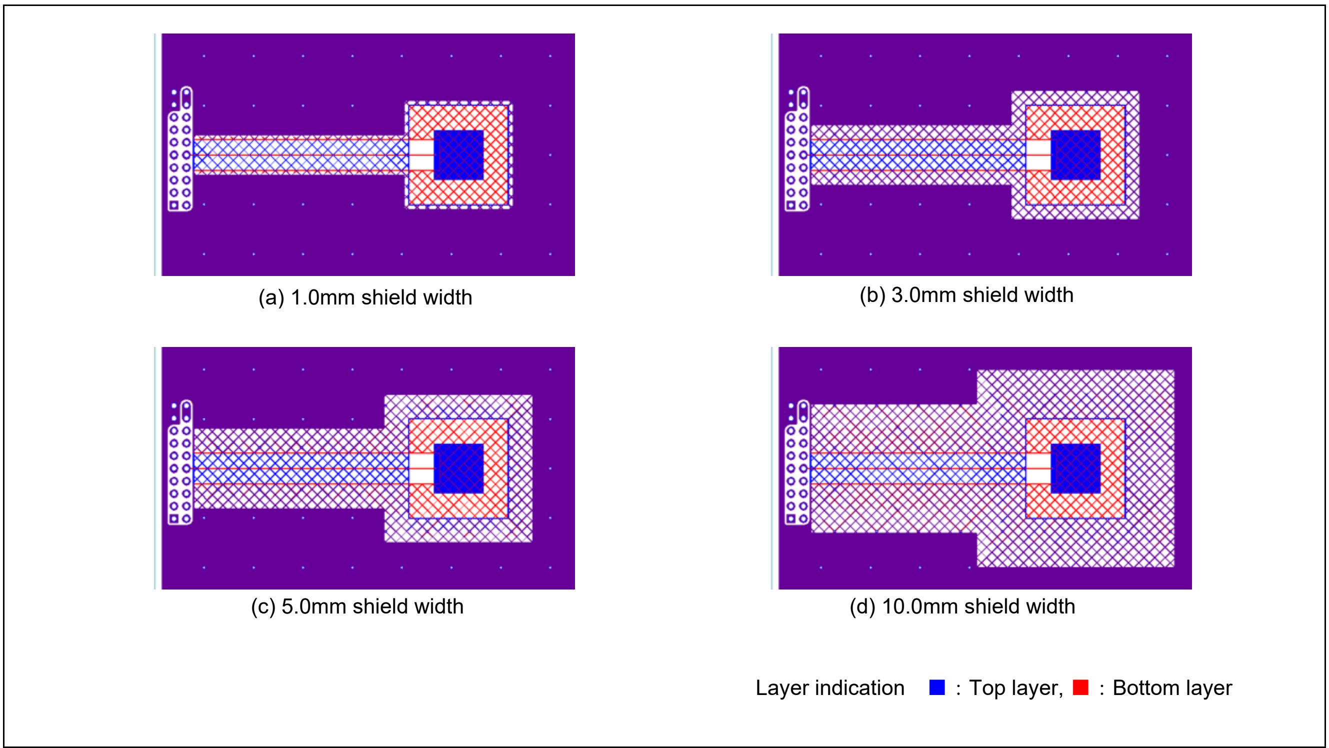


Figure 5-26 Evaluation Board Pattern (Distance between electrode/wiring and cross-hatched shield = recommended value)

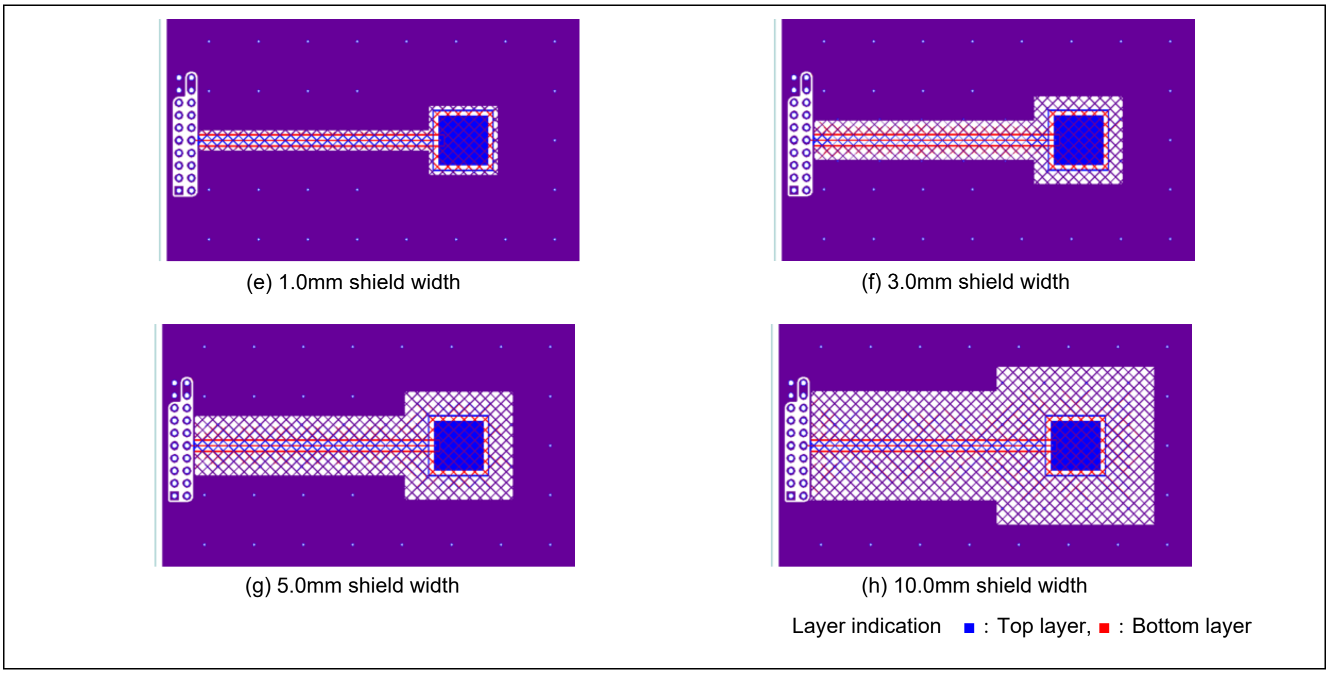


Figure 5-27 Evaluation Board Pattern (Distance between electrode/wiring and cross-hatched shield = 1.0mm)

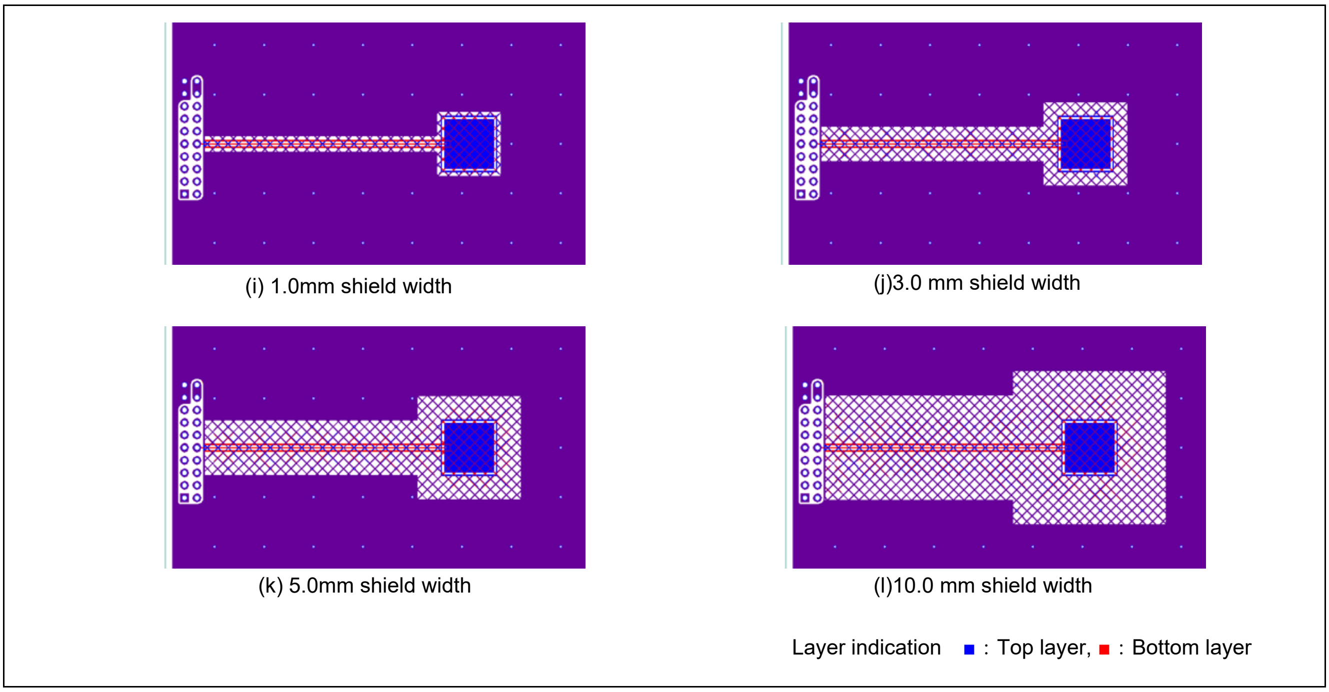


Figure 5-28 Evaluation Board Pattern (Distance between electrode/wiring and cross-hatched shield = 0.5mm)

Figure 5-29 shows Cross-hatched Shield Width and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- COND1 (recommended design): Parasitic capacitance is constant regardless of the cross-hatched GND pattern width. Although a solid GND is placed on around the cross-hatched shield, it should have no effect if there is sufficient distance between the shield and the electrode and wiring. In COND2 and COND3, as the cross-hatched shield width is narrowed, the distance between the solid GND and the electrode and wiring decreases, causing the parasitic capacitance to increase.

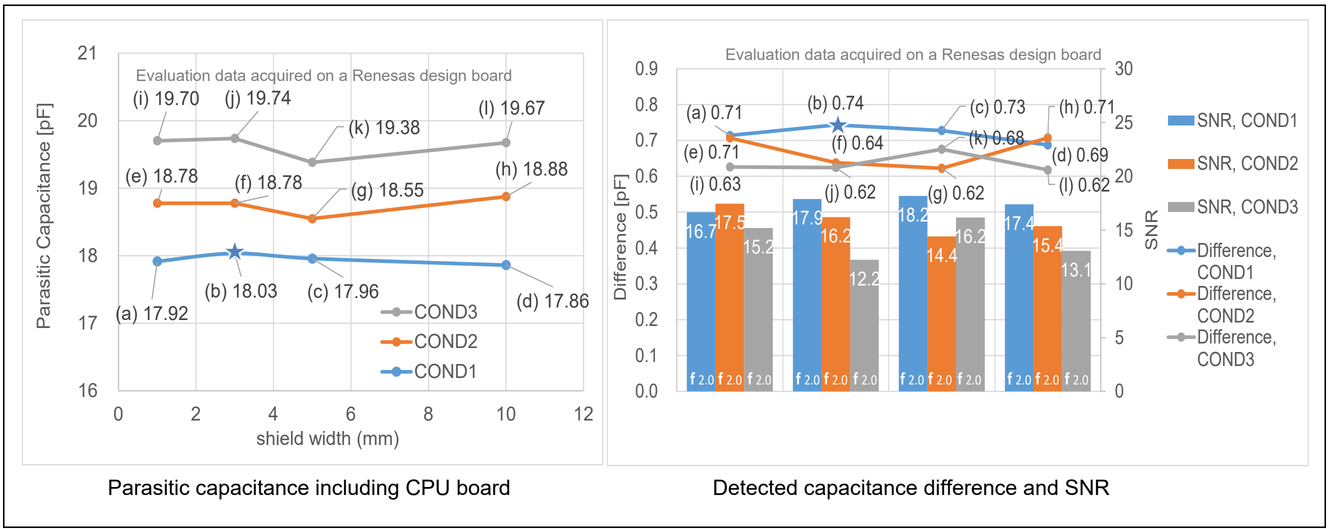


Figure 5-29 Cross-hatched Shield Width and Sensitivity Characteristics

5.3.4.5 Cross-hatched Shield Pattern Aperture Ratio

Table 5-17 lists Board Specifications for Cross-hatched Pattern Aperture Ratio. For evaluation purposes, only the inner shield hierarchy and the shield type on the multi-layered board was varied; all other design parameters remained fixed.

Table 5-17 Board Specifications for Cross-hatched Pattern Aperture Ratio Variations

Design Parameter	Specification	Unit	Notes
Shield aperture ratio	**30、81、90**	**%**	
Inner Shield layers	**Only the bottom layer (layer 4), layer 3 and 4**	**-**	
Shield type	Cross-hatched **GND**	**-**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

Figure 5-30 shows the Cross-hatched Pattern Dimensions.

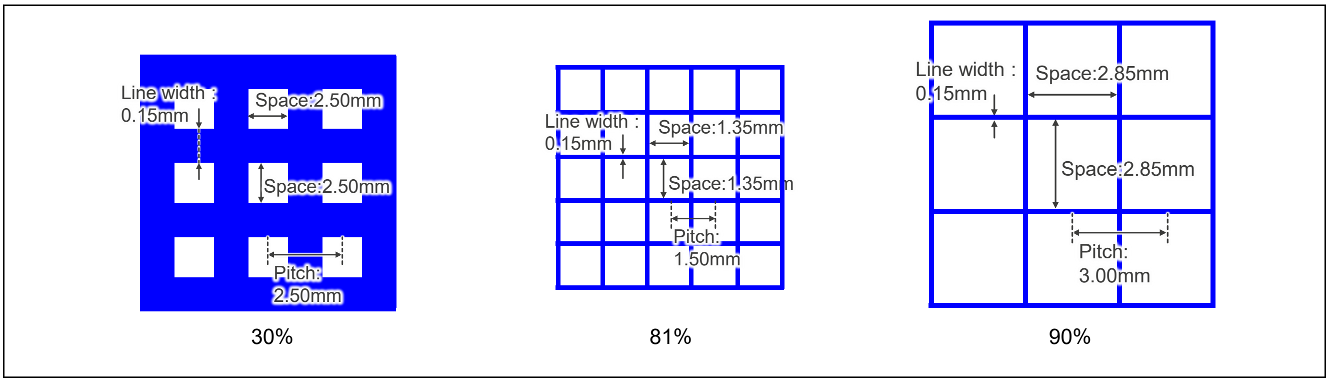


Figure 5-30 Cross-hatched Pattern Dimensions

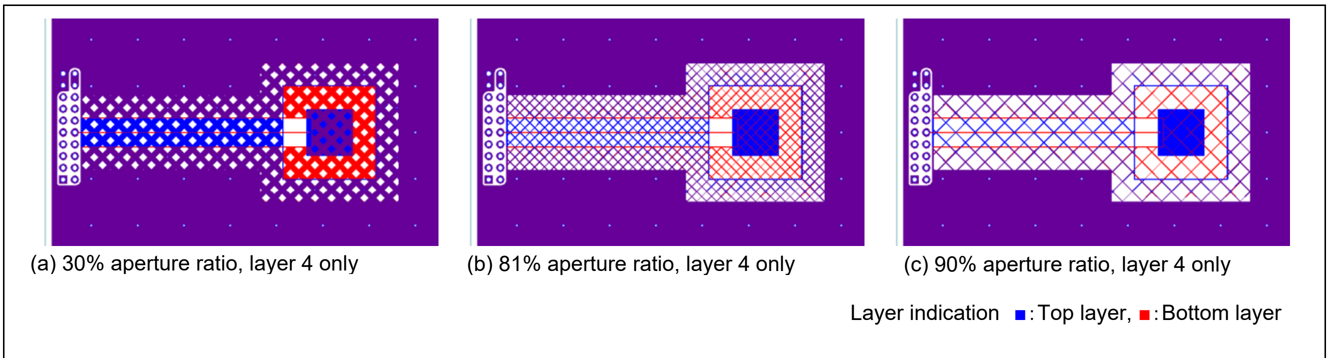


Figure 5-31 Evaluation Board Patterns (double-sided board, GND shield)

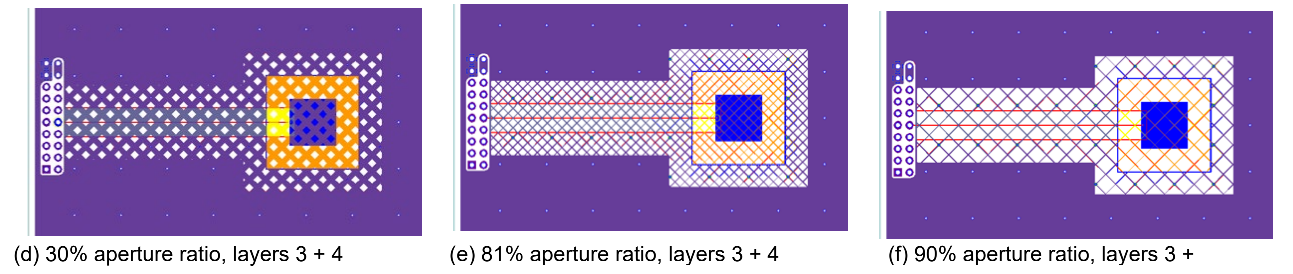


Figure 5-32 Evaluation Board Patterns (4-layered board, GND shield)

Figure 5-33 shows Cross-hatched Shield Aperture Ratio and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The smaller the cross-hatched GND aperture ratio, the larger the facing area opposite the electrode, which cause the parasitic capacitance to increase. In addition, when a GND shield layer is added to an inner layer, the facing distance decreases, causing the parasitic capacitance to increase proportionately.
- The detected capacitance difference at touch is constant, regardless of the aperture ratio.

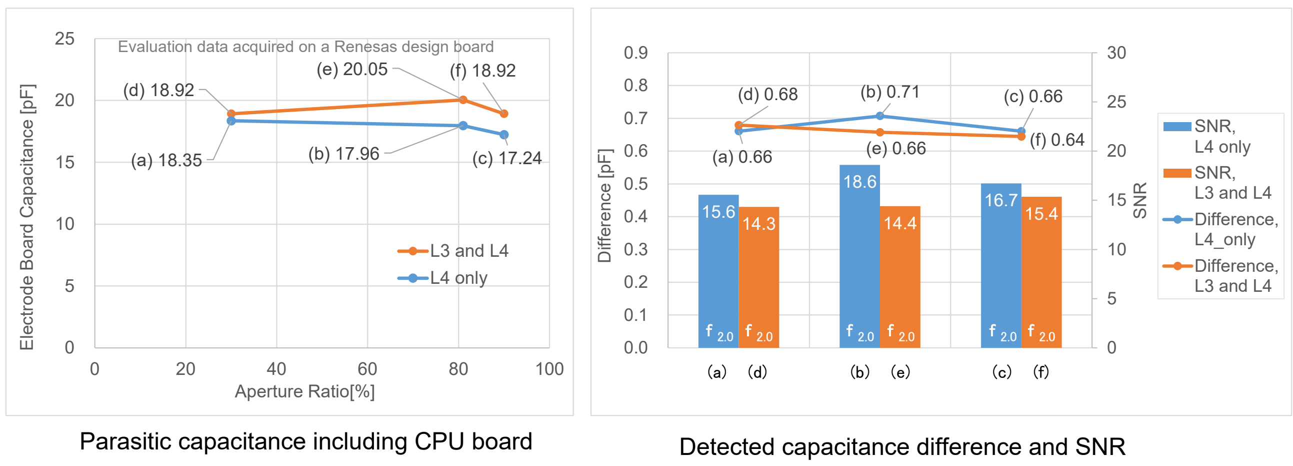


Figure 5-33 Cross-hatched Shield Aperture Ratio and Sensitivity Characteristics

5.3.5 Active Shield Design

5.3.5.1 Active Shield Area

Table 5-18 lists Board Specifications for Active Shield Electrode Capacitance Confirmation According to Number of Buttons. For evaluation purposes, only the number of button electrodes was varied; all other design parameters remained fixed.

Table 5-18 Board Specifications for Active Shield Electrode Capacitance Confirmation According to Number of Buttons

Design Parameter	Specification	Unit	Notes
Number of button electrodes	**1, 3, 5**	**electrode**	
Shield type	Active shield	-	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

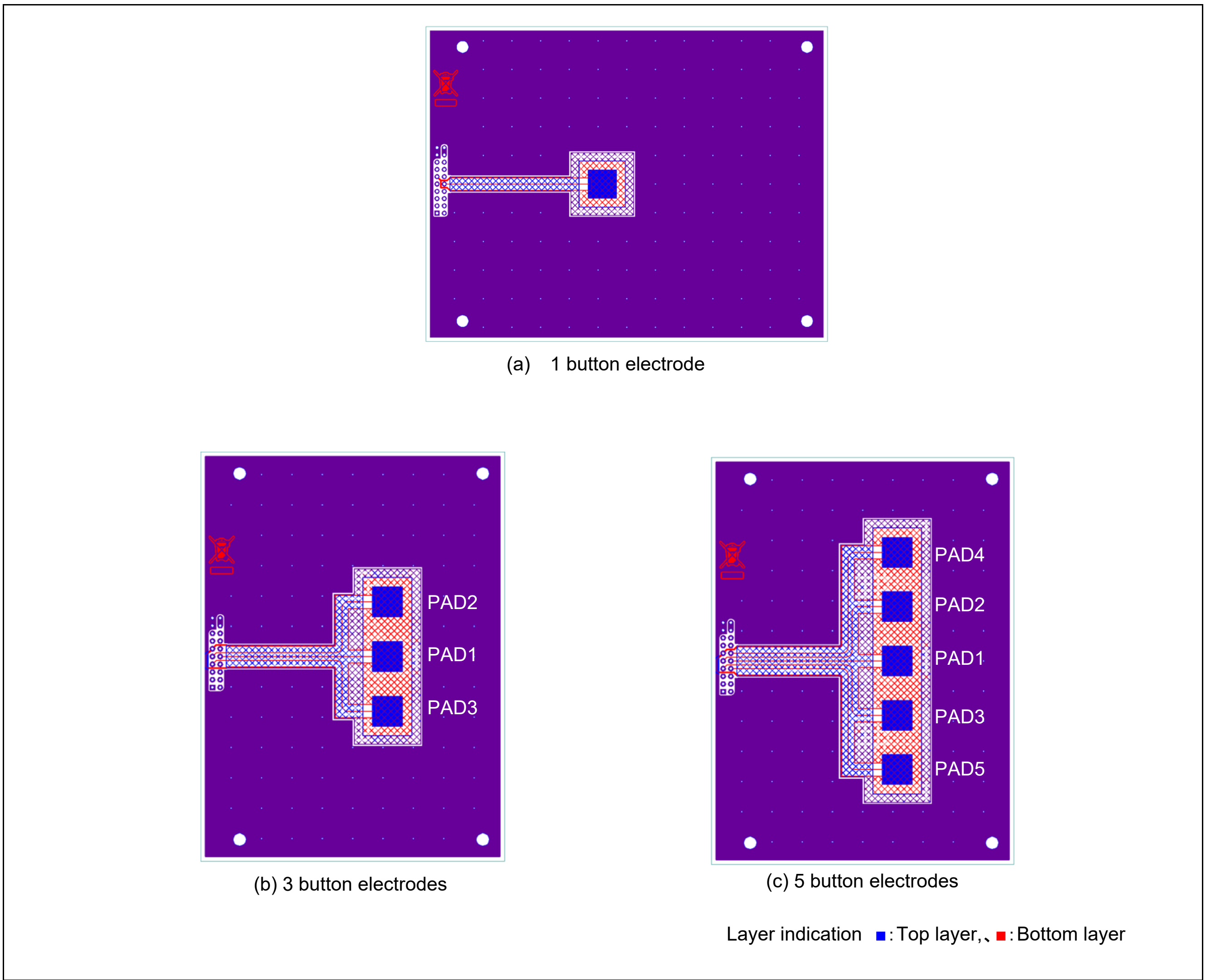
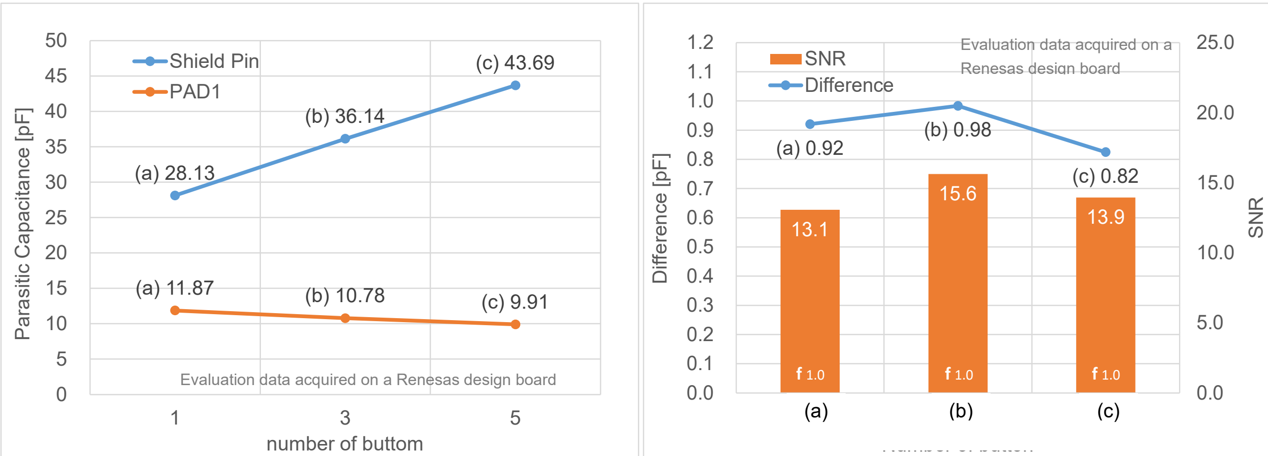


Figure 5-34 Evaluation Board Pattern (active shield electrode capacitance confirmation board)

Figure 5-35 shows Active Shield Capacitance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The evaluation board equipped with an active shield has less parasitic capacitance than the evaluation board with a cross-hatched GND shield, and the parasitic capacitance is mainly detected in the area of the CPU board. The CPU board remains as parasitic capacitance because it does not have an active shield.
- The parasitic capacitance of button PAD1 decreases in proportion to the total number of buttons. This improvement is due to the parasitic capacitance reduction effect of the active shield as well as the increased shield area, which increases the distance between the button and the peripheral solid GND.
- Since the active shield area increases as the number of button is increased, the parasitic capacitance from the active shield pin also increases.
- On the board used in this evaluation, the parasitic capacitance of the active shield tends to be larger than that of the button itself. The automatic adjustment function of QE for Capacitive Touch selects the drive pulse frequency to match the pin with the largest parasitic capacitance from the button or active shield configuration (method). When designing your application, keep in mind that the parasitic capacitance of the active shield pin may go over 50pF, depending on the number and size of buttons.
-



Parasitic capacitance including CPU board

Detected capacitance difference and SNR

Figure 5-35 Active Shield Capacitance and Sensitivity Characteristics

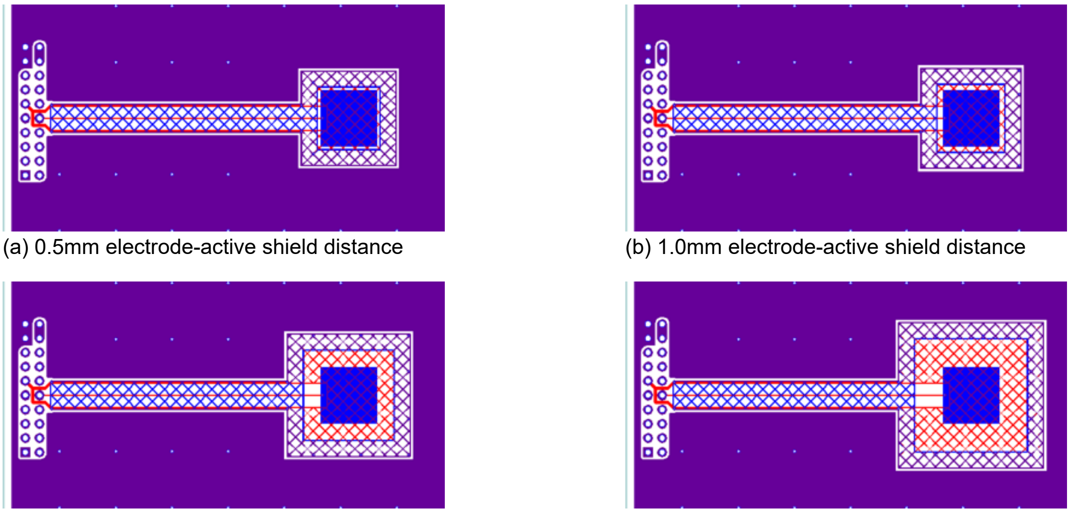
5.3.5.2 Distance Between Electrode and Active Shield

Table 5-19 lists Board Specifications for Electrode-Active Shield Distance Variations. For evaluation purposes, only the distance between the electrode and the active shield was varied; all other design parameters remained fixed.

Table 5-19 Board Specifications for Electrode-Active Shield Distance Variations

Design Parameter	Specification	Unit	Notes
Distance between electrode and active shield	**0.5, 1.0, 3.0, 5.0**	**mm**	
Distance between wiring and active shield	**0.5, 3.0, 5.0**	**mm**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.



(a) 0.5mm electrode-active shield distance

(b) 1.0mm electrode-active shield distance

(c) 3.0mm electrode-active shield distance

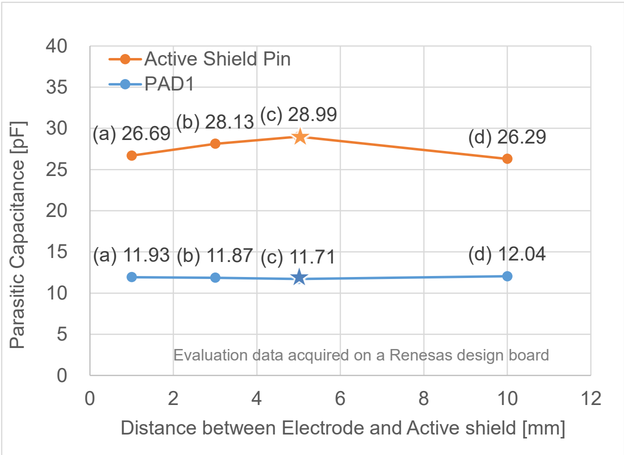
(d) 5.0mm electrode-active shield distance

Layer indication ■: Top layer, ■: Bottom layer

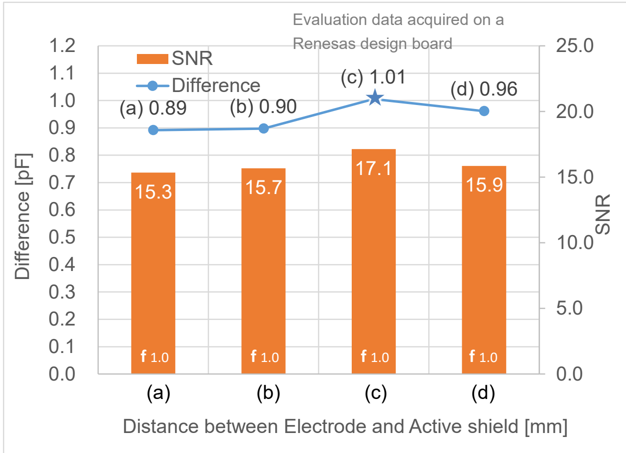
Figure 5-36 Evaluation Board Pattern

Figure 5-37 shows Electrode-Active Shield Distance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The parasitic capacitance of the button electrode is constant regardless of the distance between the electrode and the active shield. The parasitic capacitance of the active shield pin is dependent on the area of the shield.
- The SNR does not fluctuate due to the distance between the electrode and the active shield. Because the active shield reduces the effect of the distance between solid GND pattern on the outer periphery and the electrodes, the capacitance detection difference improves in proportion to the distance between the electrode and active shield.



Parasitic capacitance including CPU board



Detected capacitance difference and SNR

Figure 5-37 Electrode-Active Shield Distance and Sensitivity Characteristics

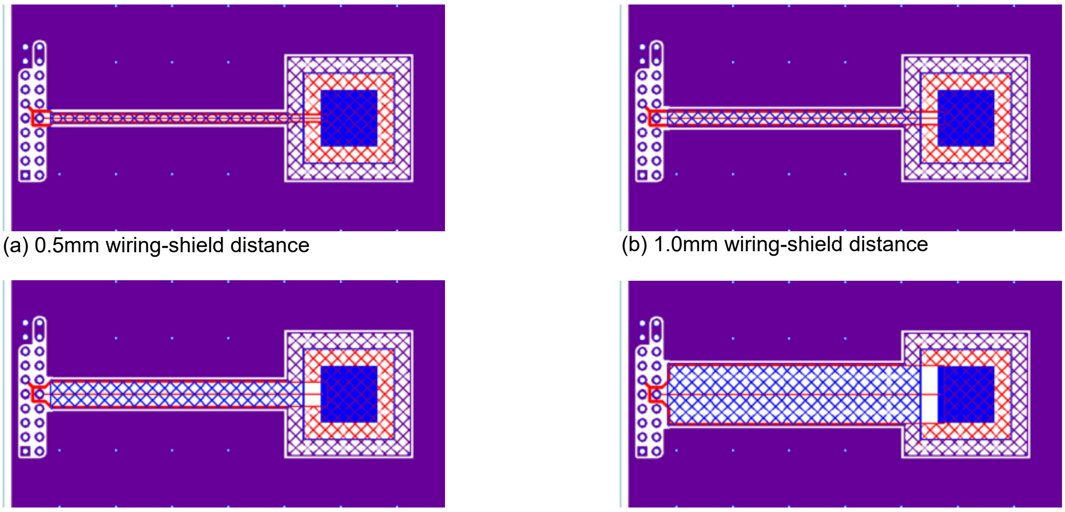
5.3.5.3 Distance between Wiring and Active Shield

Table 5-20 lists Board Specifications for Wiring-Active Shield Distance Variations. For evaluation purposes, only the distance between the wiring and active shield was varied; all other design parameters remained fixed.

Table 5-20 Board Specifications for Wiring-Active Shield Distance Variations

Design Parameter	Specification	Unit	Notes
Difference between wiring and active shield	**0.5, 1.0, 3.0, 5.0**	**mm**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.



(a) 0.5mm wiring-shield distance

(b) 1.0mm wiring-shield distance

(c) 3.0mm wiring-shield distance

(d) 5.0mm wiring-shield distance

Layer indication ■ : Top layer, ■ : Bottom layer

Figure 5-38 Evaluation Board Pattern (wiring-active shield distance)

Figure 5-39 shows Wiring-Active Shield Distance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The parasitic capacitance of the button electrode is constant regardless of the distance between the wiring and the active shield. The parasitic capacitance of the active shield pin is dependent on the area of the shield.
- The SNR does not fluctuate due to the distance between the wiring and the active shield. The capacitance detection value is constant, and the capacitance detection difference is not affected by the distance between the wiring and the active shield.

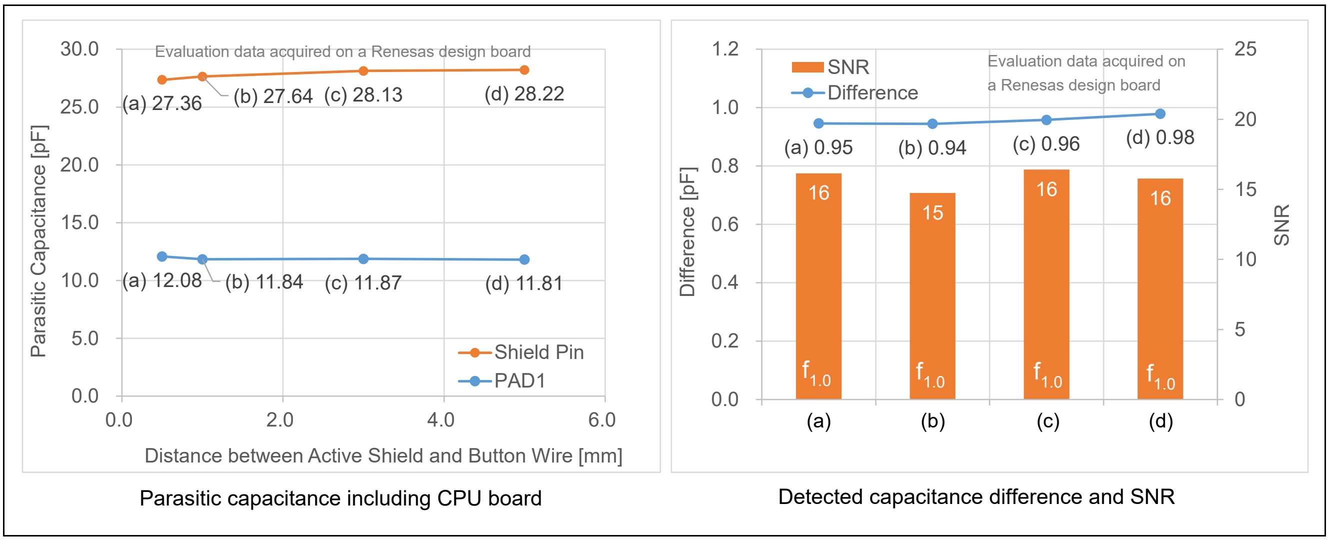


Figure 5-39 Wiring-Active Shield Distance and Sensitivity Characteristics

5.3.5.4 Distance Between Active Shield and Solid GND

Table 5-21 lists Board Specifications for Active Shield-Solid GND Distance Variations. For evaluation purposes, only the distance between the active shield and the solid GND was varied; all other design parameters remained fixed.

Table 5-21 Board Specifications for Active Shield-Solid GND Distance Variations

Design Parameter	Specification	Unit	Notes
Distance between active shield and solid GND	**0.5、1.0、5.0、10.0**	**mm**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

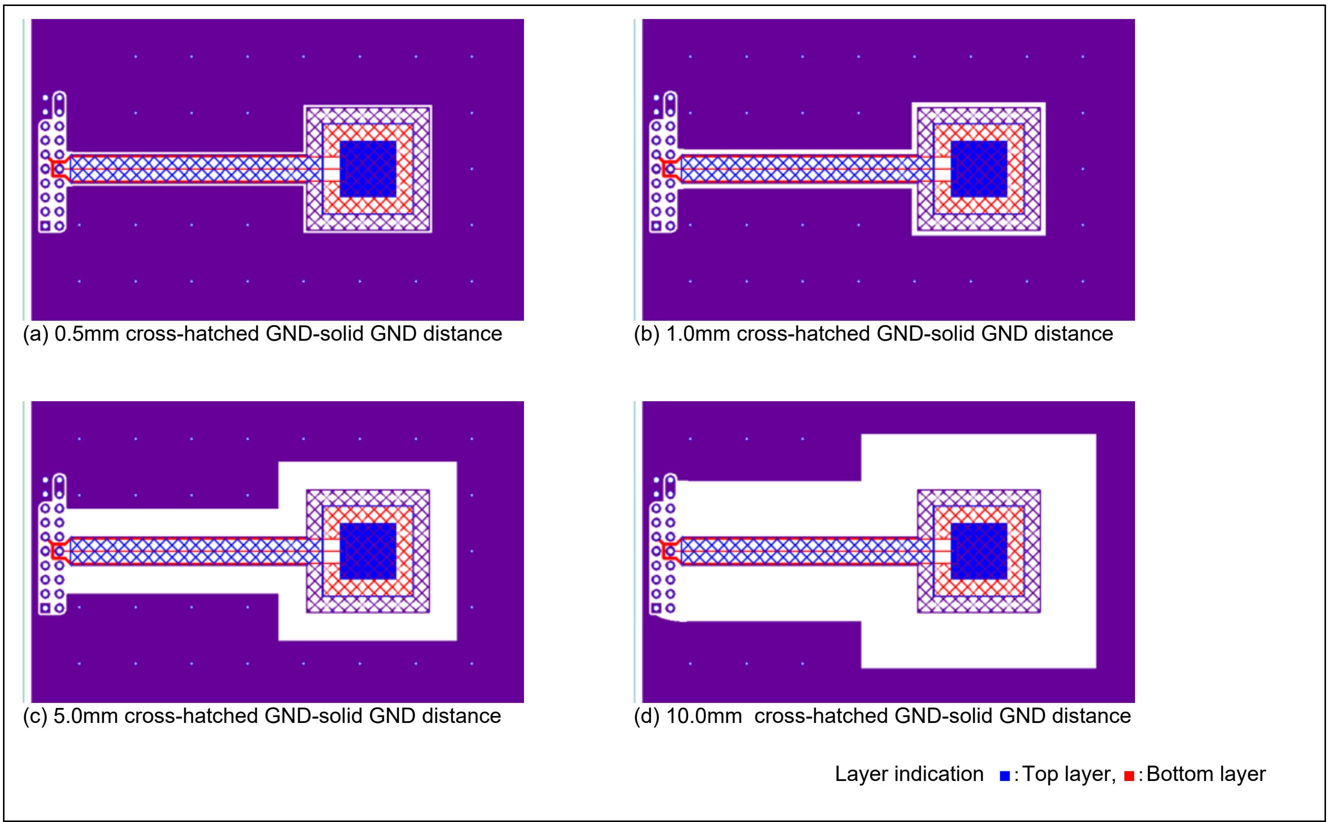
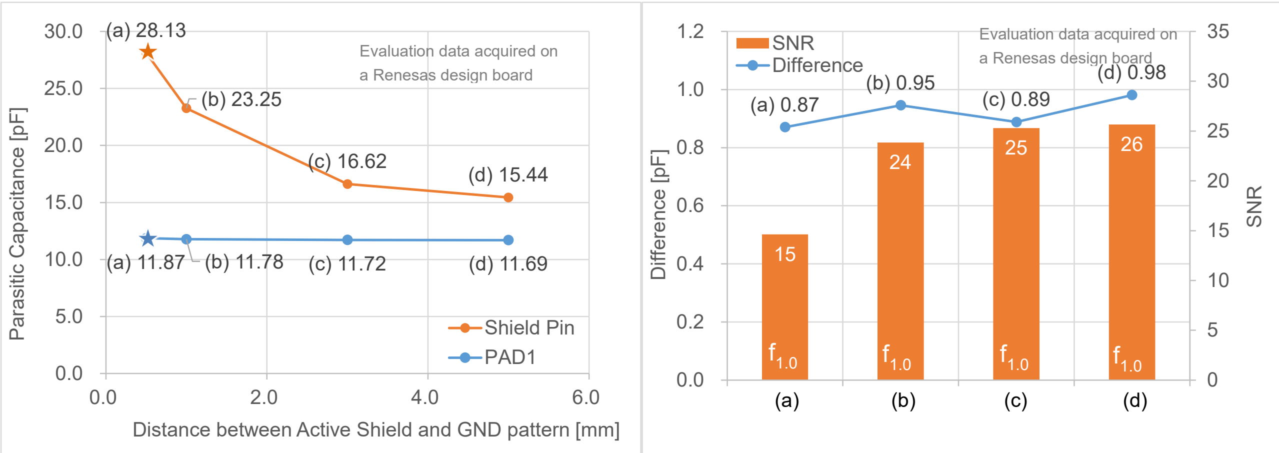


Figure 5-40 Evaluation Board Pattern (active shield-solid GND distance and sensitivity characteristics)

Figure 5-41 shows Active Shield-Solid GND Distance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The parasitic capacitance of the button is constant regardless of the distance between the active shield and the solid GND. The recommended design values ensure plenty of distance between the active shield and solid GND so that the button's parasitic capacitance is not affected. The shorter the distance between the active shield and the solid GND, the more the parasitic capacitance of the active shield pin increases.
- Because the drive pulse frequency is selected according to the pin with the largest parasitic capacitance, the SNR may decrease based on the board design.



Parasitic capacitance including CPU board

Detected capacitance difference and SNR

Figure 5-41 Active Shield-Solid GND Distance and Sensitivity Characteristics

5.3.5.5 Active Shield Pattern Width

Table 5-22 lists Board Specifications for Active Shield Pattern Width Variations. For evaluation purposes, only the distance between electrode and active shield and the distance between the related wiring and the active shield were varied; all other design parameters remained fixed.

Table 5-22 Board Specifications for Active Shield Pattern Width Variations

Design Parameter	Specification	Unit	Notes
Active shield width	**1.0, 3.0, 5.0, 10.0**	**mm**	
Distance between electrode and active shield	**0.5, 3.0, 5.0**	**mm**	
Distance between wiring and active shield	**0.5, 3.0, 5.0**	**mm**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	
Combined shield conditions (wiring-shield distance/ electrode-shield distance)			
Combination 1 (COND1)	3.0/3.0	mm	Recommended design values
Combination 2 (COND2)	0.5/0.5	mm	
Combination 3 (COND3)	5.0/5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

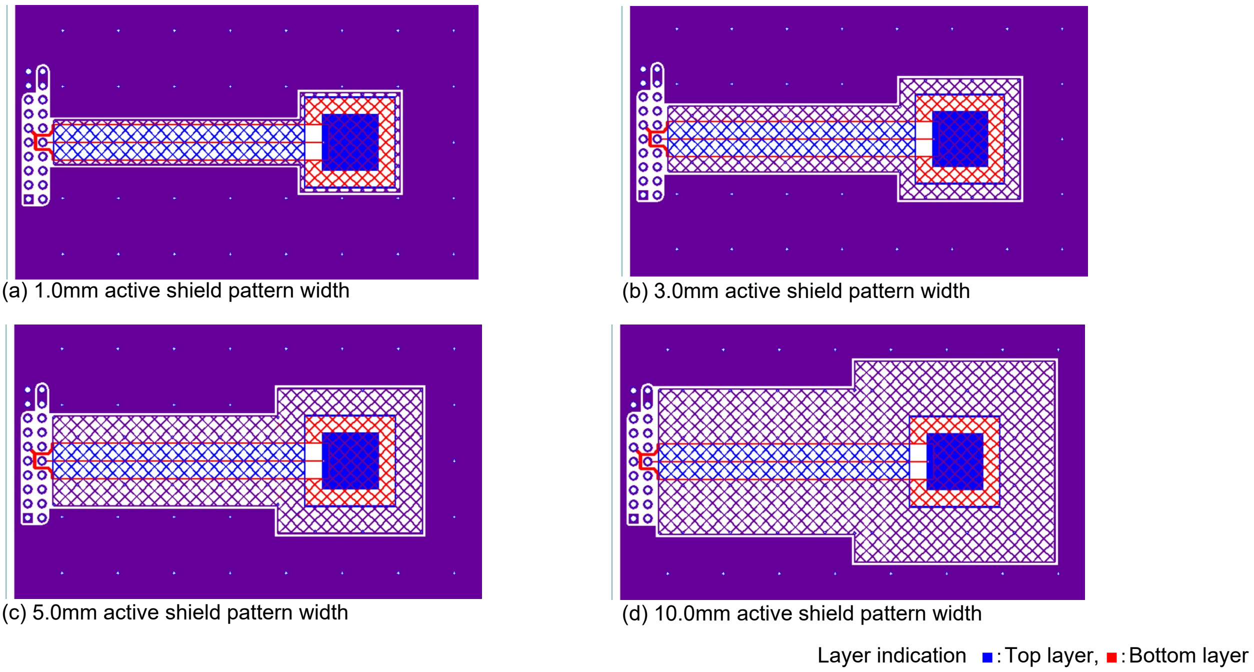
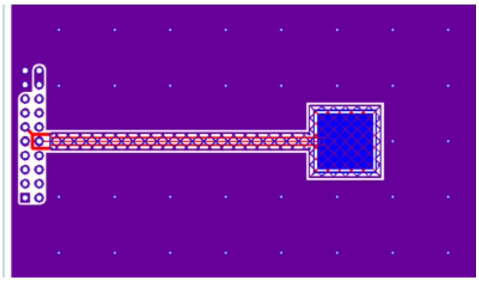
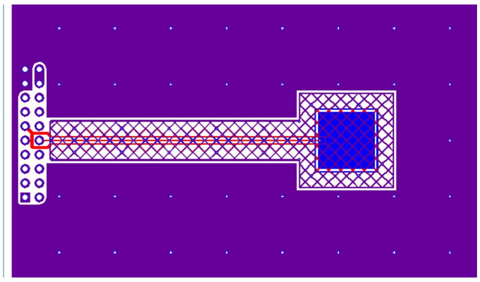


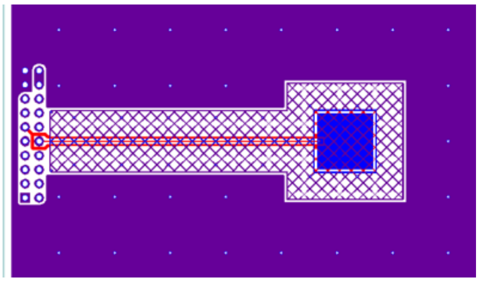
Figure 5-42 Evaluation Board Pattern (electrode/wiring and active shield distance: 3.0mm)



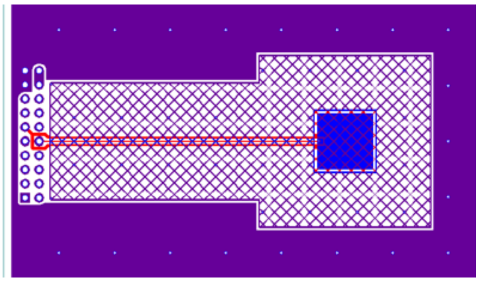
(a) 1.0mm active shield pattern width



(b) 3.0mm active shield pattern width



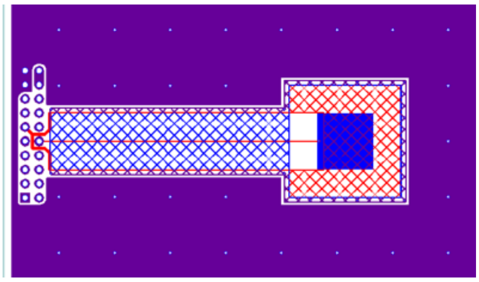
(c) 5.0mm active shield pattern width



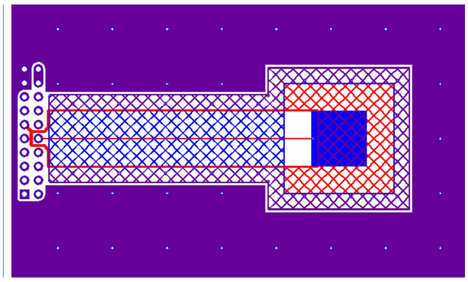
(d) 10.0mm active shield pattern width

Layout indication ■: Top layer, ■: Bottom layer

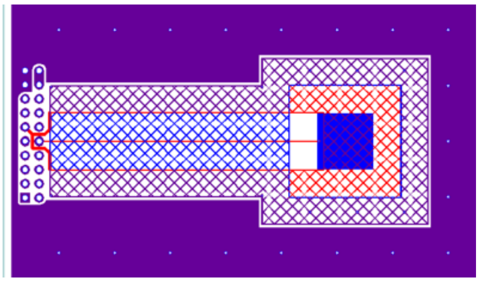
Figure 5-43 Evaluation Board Pattern (electrode/wiring and active shield distance: 0.5mm)



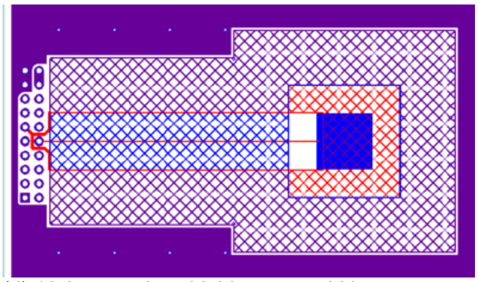
(a) 1.0mm active shield pattern width



(b) 3.0mm active shield pattern width



(c) 5.0mm active shield pattern width



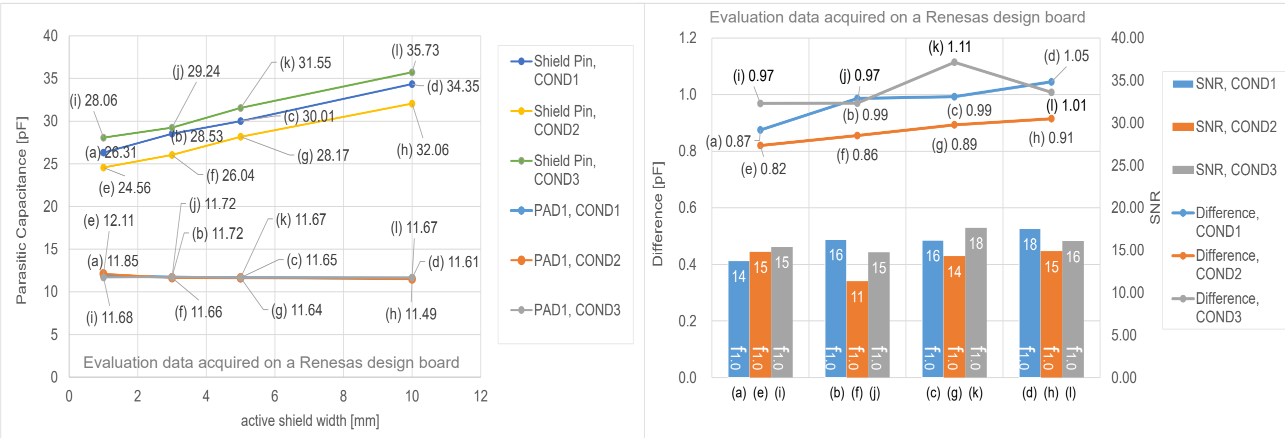
(d) 10.0mm active shield pattern width

Layout indication ■: Top layer, ■: Bottom layer

Figure 5-44 Evaluation Board Pattern (electrode/wiring and active shield distance: 5.0mm)

Figure 5-45 shows Active Shield Pattern Width and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The parasitic capacitance of the button has a slight tendency to increase when the active shield width is narrow. The shorter distance between the electrode and the solid GND pattern, the more the parasitic capacitance is affected. The active shield pin parasitic capacitance also increases due to the increase in area caused by the shield width.
- The SNR does not change due to the active shield width, but if parasitic capacitance increases due to the board design, SNR may decrease due to lower drive pulse frequency.
- The shorter the distance between the active shield and the electrode and wiring, the more the capacitance detection tends to decrease.
  The shorter the distance between the electrode and the solid GND pattern on the periphery of the active shield, the stronger the capacitive coupling of the electrode, making it difficult for capacitance changes to occur when the electrode is touched.



Parasitic capacitance including CPU board　　　　Detected capacitance difference and SNR

Figure 5-45 Active Shield Pattern Width and Sensitivity Characteristics

5.3.5.6 Damping Resistance Value of Active Shield Pin

Table 5-23 lists the Conditions for Evaluating Damping Resistance Value and Sensitivity Characteristics of Active Shield Pin. For evaluation purposes, only the number of button electrodes was varied; all other design parameters remained fixed.

Table 5-23 Conditions for Evaluating Damping Resistance Value and Sensitivity Characteristics of Active Shield Pin

Design Parameter	Specification	Unit	Notes
Damping resistance value	**10, 560, 1000**	**Ω**	
Shield type	Active shield	-	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

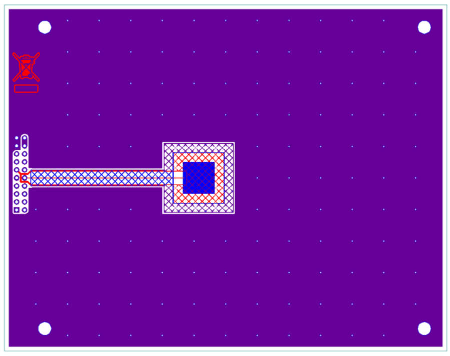


Figure 5-46 Evaluation Board Pattern

Figure 5-47 shows the Damping Resistance Value and Sensitivity of Active Shield Pin.

When changing the damping resistance value of the active shield pin for the same electrode pattern, the button capacitance and SNR remain constant, regardless of the damping resistance of the active shield. Since the role of the damping resistor is to attenuate external noise, reducing the resistance value may result in unstable measurement values due to external noise or run the risk of stopping CTSU operations due to TSCAP voltage errors, etc. Always be sure to evaluate the resistance value thoroughly, especially if it is smaller than the recommended value of 560 Ω.

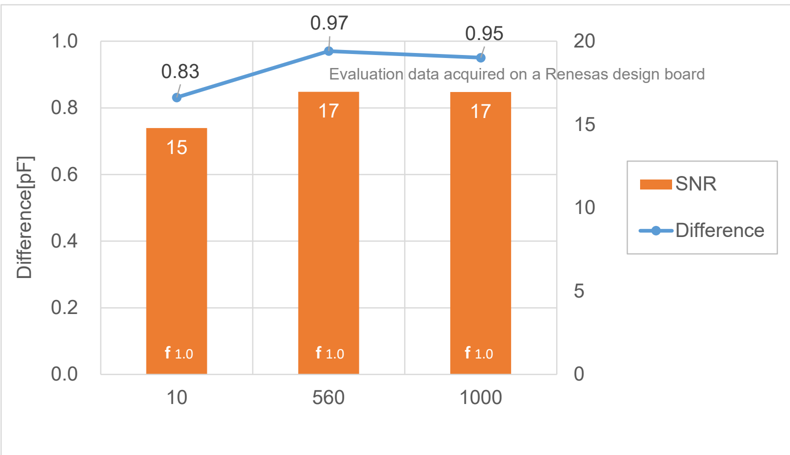


Figure 5-47 Damping Resistance Value and Sensitivity of Active Shield Pin Characteristics

5.3.6 Parameters Unrelated to Board Design

5.3.6.1 Overlay Panel Design and Sensitivity Characteristics

Table 5-24 lists Board Specifications for Overlay panel thickness and Air Gap Layer Variations. For evaluation purposes, all other design parameters remained fixed.

Table 5-24 Board Specifications for Overlay panel thickness and Air Gap Layer Variations

Design Parameter	Specification	Unit	Notes
Overlay panel thickness	**2.0, 10.0**	**mm**	Acrylic
Air gap	**0, 1.0, 3.0, 5.0**	**mm**	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

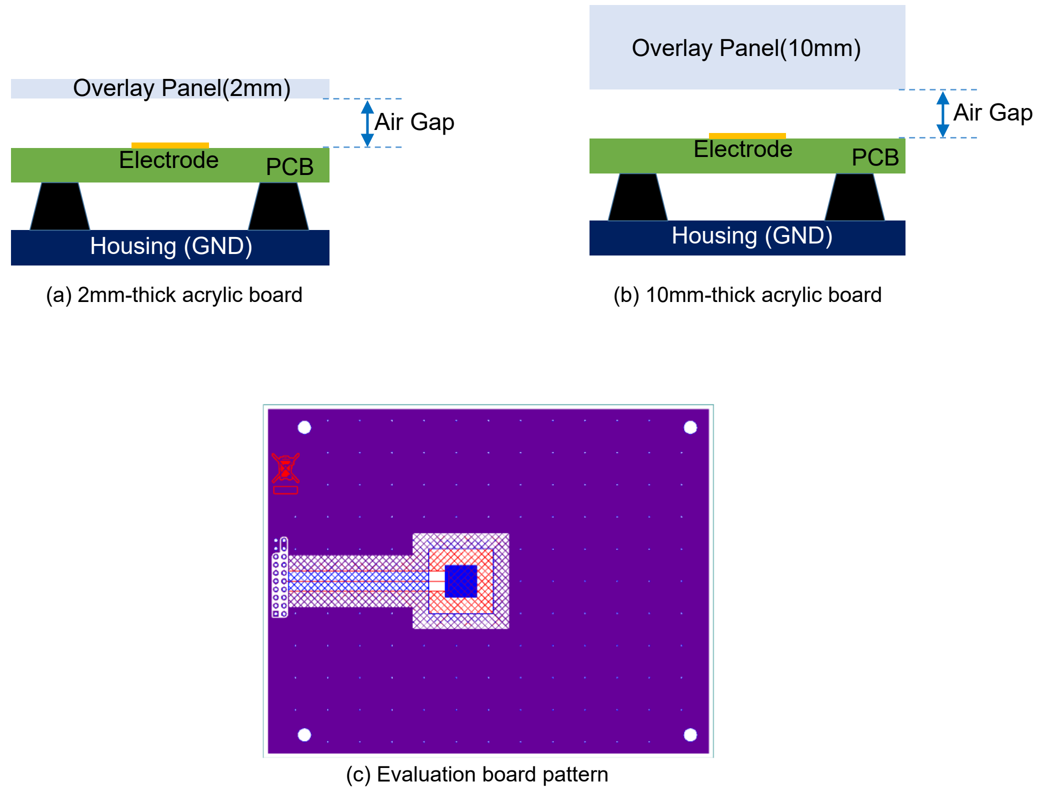


Figure 5-48 Evaluation condition

Figure 5-49 shows overlay panel air gap and parasitic capacitance. Figure 5-50 shows overlay panel air gap and sensitivity capacitance. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

The thicker the overlay panel, the more the parasitic capacitance increases, but the difference in detected capacitance decreases, resulting in a lower SNR.
The wider the air gap, the lower the detected capacitance difference of the board and the lower the SNR.
For capacitive touch, the electrode and finger are the equivalent of the electrodes of a capacitor, so the thicker the overlay panel, the lower the SNR. Also, because the dielectric constant is lower for the air gap than for the acrylic overlay panel, the wider the air gap, the lower the detected capacitance and SNR.

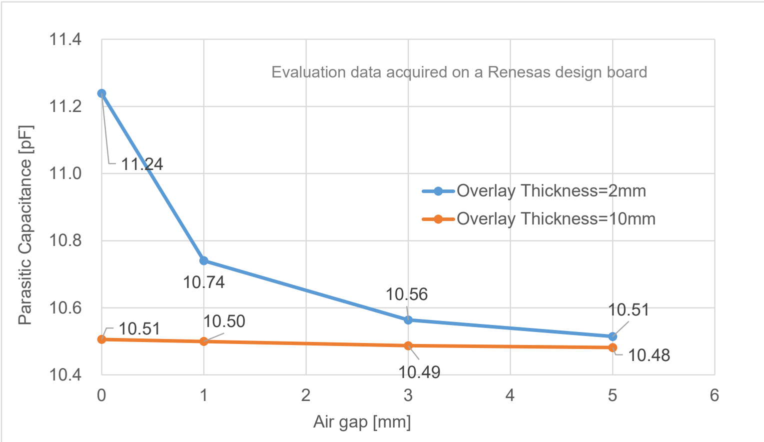


Figure 5-49 Overlay Panel Air Gap and Parasitic Capacitance

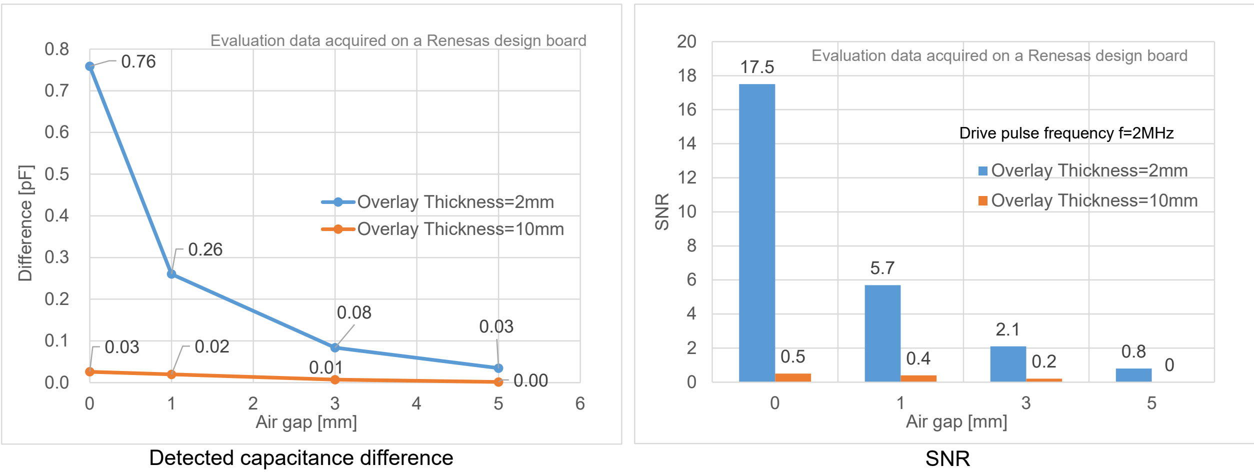


Figure 5-50 Overlay Panel Air Gap and Sensitivity Characteristics

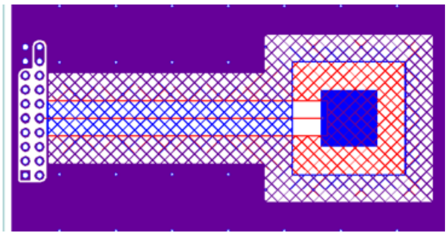
5.3.6.2 Electrode Damping Resistance Value and Sensitivity Characteristics

Table 5-25 lists Board Specifications for Damping Resistance. For evaluation purposes, all other design parameters remained fixed.

Table 5-25 Board Specifications for Damping Resistance Variations

Design Parameter	Specification	Unit	Notes
Damping resistance value	**10、560、1000**	Ω	
Shield type	Cross-hatched GND	-	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

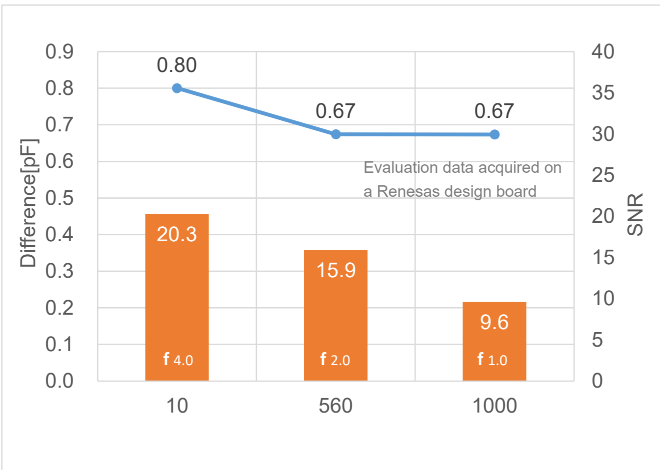


Layer indication ■ : Top layer, ■ : Bottom layer

Figure 5-51 Evaluation Board Pattern

Figure 5-52 shows Damping Resistance Value and Sensitivity.

- The time constant and the charging/discharging time of the circuit increase in proportion to the damping resistance value. It is necessary to ensure sufficient charging and discharging time for the parasitic capacitance of the TS pin to ensure successful CTSU measurements. Insufficient charging/discharging will result in unstable measurement values. Therefore, the drive pulse frequency must be lowered in order to secure sufficient charging/discharging time.
- The automatic adjustment function of QE for Capacitive Touch determines the most suitable drive pulse frequency based on the largest parasitic capacitance at non-touch.
- Since the role of the damping resistor is to attenuate external noise, reducing the resistance value may result in unstable measurement values due to external noise or run the risk of stopping CTSU operations due to TSCAP voltage errors, etc. Always be sure to evaluate the resistance value thoroughly, especially if it is smaller than the recommended value of 560 Ω.



Note: f = drive pulse frequency

Figure 5-52 Damping Resistance Value and Sensitivity Characteristics

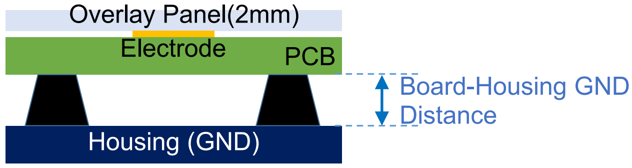
5.3.6.3 Board-Housing GND Distance and Sensitivity

Table 5-26 lists Board Specifications for Board-Housing GND Distance Variations. For evaluation purposes, all other design parameters remained fixed.

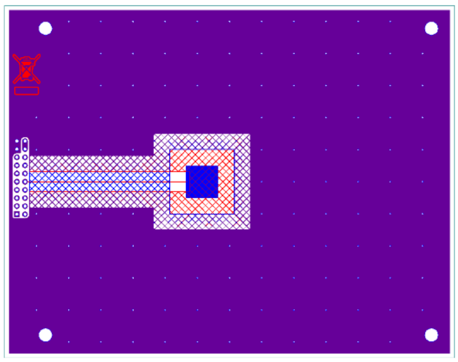
Table 5-26 Board Specifications for Board-Housing GND Distance Variations

Design Parameter	Specification	Unit	Notes
Distance between board and housing GND (board spacer height)	**2.0, 5.0, 20.0**	**mm**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.



Board-Housing GND Distance

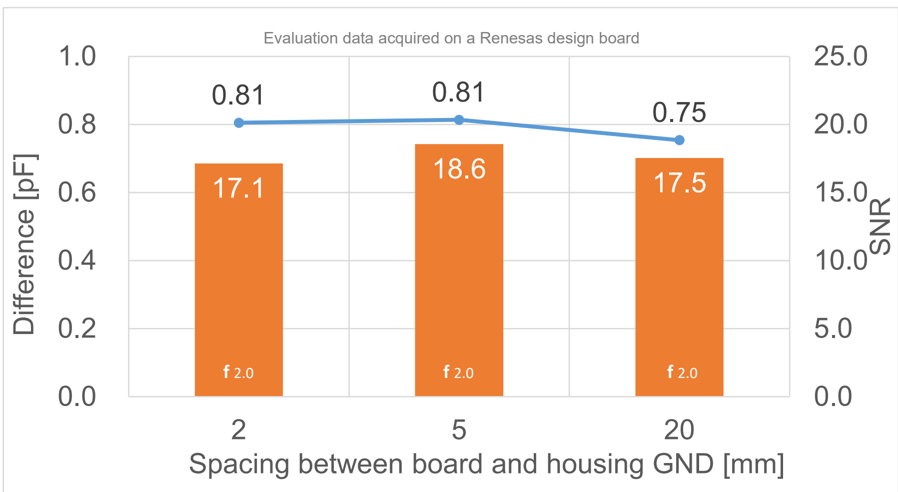


Evaluation board pattern

Figure 5-53 Evaluation Condition

Figure 5-54 shows Board-Housing GND Distance and Sensitivity Characteristics。 Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The shorter the distance from board surface to housing (assuming GND level conductors), the lower the sensitivity. Capacitive coupling becomes stronger the closer the board is to the housing, making it difficult for capacitance changes to occur when the electrode is touched.



Distance between board and housing GND [mm]

Figure 5-54 Board-Housing GND Distance and Sensitivity Characteristics

5.3.6.4 Sensitivity Characteristics with ESD Protection Diode Connected

Table 5-27 lists Board Specifications for Parasitic Capacitance Variations of ESD Protection Diode. For evaluation purposes, all other design parameters remained fixed. Note that this table indicates the sensitivity characteristics when an ESD protection diode is connected to the TS pin, but ESD tests have not been conducted. Also note that specifications such as location of the ESD protection diode and required pressure resistance differ according to system. Please keep this in mind when designing the pattern and selecting materials.

Table 5-27 Board Specifications for Parasitic Capacitance Variations of ESD Protection Diode

Design Parameter	Specification	Unit	Notes
ESD protection diode capacitance (Typ. value)	**0 (not connected), 0.75, 10, 30**	**pF**	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

Figure 5-55 shows Circuit Diagram for ESD Protection Diode Parasitic Capacitance Evaluation Board

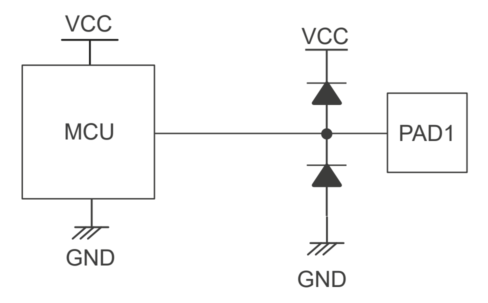


Figure 5-55 Circuit Diagram for ESD Protection Diode Parasitic Capacitance Evaluation Board

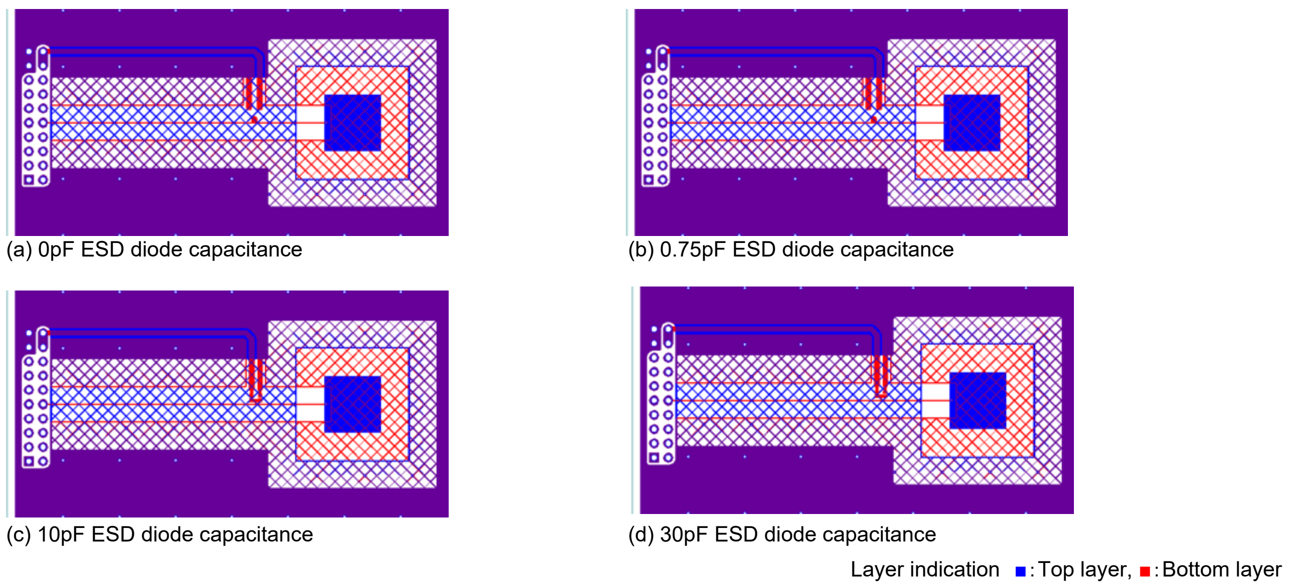
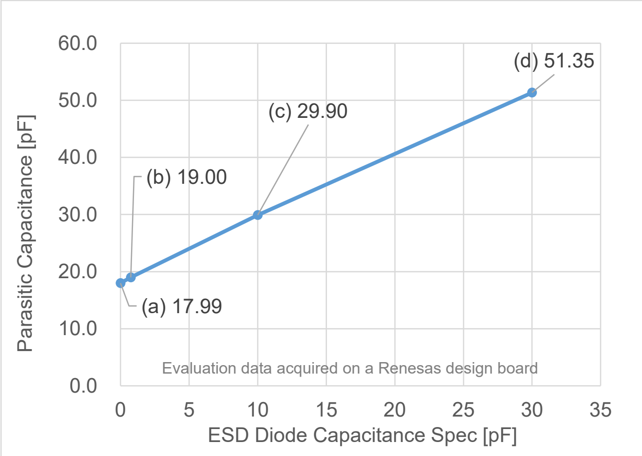


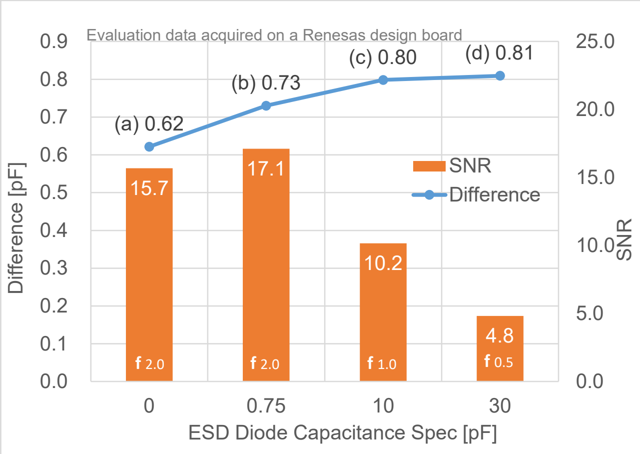
Figure 5-56 Evaluation Board Pattern

Figure 5-57 shows ESD Protection Diode Parasitic Capacitance and Sensitivity Characteristics. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

When an ESD protection diode is connected to the TS pin, the capacitance of the connected element is added; if the capacitance is large, the drive pulse frequency drops, making the sensitivity lower as well. Since the CTSU estimates capacitance from the amount of current applied to parasitic capacitance, if you plan to use an ESD protective diode, make sure to select a product with a low capacitance value and minimal leakage current.



(i) Parasitic capacitance including CPU board



(ii) Detected capacitance difference and SNR

Figure 5-57 ESD Protection Diode Parasitic Capacitance and Sensitivity Characteristics

5.3.6.5 Supply Voltage and Sensitivity Characteristics

Table 5-28 lists Electrode Specifications for Supply Voltage Variations. For evaluation purposes, only the supply voltage was varied; all other design parameters remained fixed.

Table 5-28 Electrode Specifications for Supply Voltage Variations

Design Parameter	Specification	Unit	Notes
Supply voltage	**1.8, 3.3, 5.0**	**V**	
Shield type	Cross-hatched GND	-	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

Table 5-29 lists CTSU1 Device Evaluation Conditions and Table 5-30 lists CTSU2 Device Evaluation Conditions. This evaluation was conducted for the CTSU1 device and CTSU2 device.

Table 5-29 CTSU1 Device Evaluation Conditions

Item	Specifications
CPU board	RX130 Cap Touch CPU Board (RTK0EG0004C01002BJ) (RX130 Capacitive Touch Evaluation System (RTK0EG0003S02001BJ) accessory)
MCU	RX130 (R5F51305ADFN)
Operating frequency	32MHz

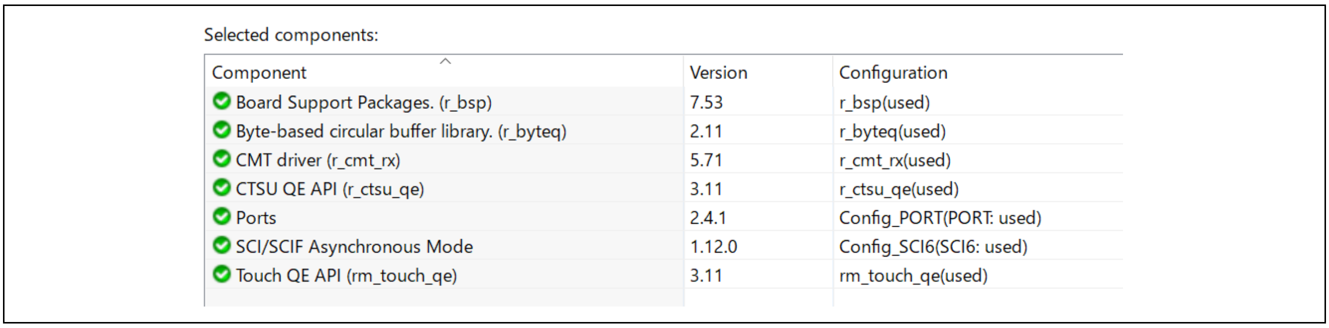
Table 5-30 CTSU2 Device Evaluation Conditions

Item	Specifications
CPU board	RX140 Cap Touch CPU Board (RTK0EG0038C01001BJ) (RX140 Capacitive Touch Evaluation System (RTK0EG0039S01001BJ) accessory)
MCU	RX140 (R5F51406ADFN)
Operating frequency	48MHz

Table 5-31 provides the Evaluation Software Development Environment (RX MCU) and Figure 5-58 shows the List of Selected Components.

Table 5-31 Evaluation Software Development Environment (RX MCU)

Item	Specifications
Integrated Development Environment	Renesas e² studio Version: 2025-04
Compiler	Renesas CC-RX v3.07.00
Development support tool for capacitive method touch sensor	QE for Capacitive Touch V4.1.0
Emulator	Renesas E2 Lite emulator


Selected components:

Component	Version	Configuration
Board Support Packages. (r_bsp)	7.53	r_bsp(used)
Byte-based circular buffer library. (r_byteq)	2.11	r_byteq(used)
CMT driver (r_cmt_rx)	5.71	r_cmt_rx(used)
CTSU QE API (r_ctsu_qe)	3.11	r_ctsu_qe(used)
Ports	2.4.1	Config_PORT(PORT: used)
SCI/SCIF Asynchronous Mode	1.12.0	Config_SCI6(SCI6: used)
Touch QE API (rm_touch_qe)	3.11	rm_touch_qe(used)

Figure 5-58 List of Selected Components

Figure 5-59 shows Automatic Adjustment Results by QE for Capacitive Touch. "Scan Time[ms]" indicates the measurement time for each channel including software overhead processing. The hardware measurement time is 0.526ms for CTSU1 and 0.256ms for CTSU2. CTSU2 supports the multi-frequency measurements in hardware and configures three frequencies of multi-frequency measurements with automatic tuning of QE for Capacitive Touch. At this time, the measurement time for each frequency is 0.128ms. Measurement result of the multi-frequency measurement is calculated from the two frequencies of measurement value selected by majority decision, so the measurement time is equivalent to 0.256 ms. CTSU1 measures at only one frequency.

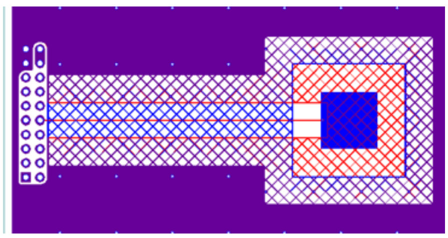
Method	Kind	Name	Touch Sensor	Parasitic Capacitance[pF]	Sensor Drive Pulse Frequency[MHz]	Threshold	Scan Time[ms]	Overflow
config01	Button(self)	Button00	TS29	14.488	1.886 (BASE: 2.0)	1594	0.559	None

(a) CTSU1 (RX130)

Method	Kind	Name	Touch Sensor	Parasitic Capacitance[pF]	Sensor Drive Pulse Frequency[MHz]	Threshold	Scan Time[ms]	Overflow
config01	Button(self)	Button00	TS29	16.188	2.0	967	0.576	None

(b) CTSU2 (RX140)

Figure 5-59 Automatic Adjustment Results by QE for Capacitive Touch



Layer indication ■ : Top layer, ■ : Bottom layer

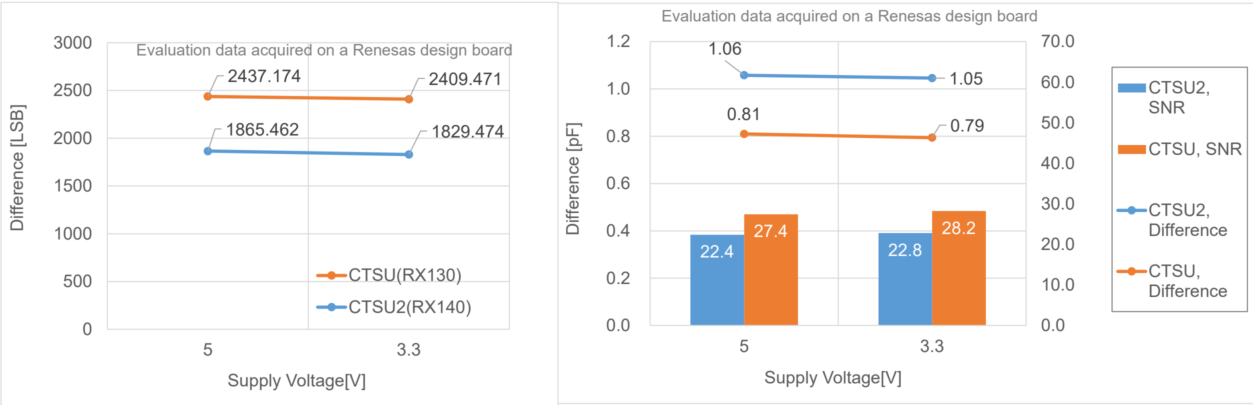
Figure 5-60 Evaluation Board Pattern

(1) Normal Mode Operations

Figure 5-61 shows Normal Mode Supply Voltage and Sensitivity Characteristics. Normal mode operations indicate conditions in which the CTSU operates with the CTSUCR1.CTSUATUNE0 bit set to ‘0’ for RX130 and the CTSUCRA.ATUNE0 bit is set to ‘0’ for RX140.

- Supply voltage does not cause changes in the measured values or sensitivity.
- The difference in the measured values and SNR of CTSU1 and CTSU2 is due to the difference in measurement time. The measurement time of CTSU2 is about 1/2 that of CTSU1, but the measured value and SNR are about 2/3, so the measurement accuracy per unit time is improved.

Note : If the power supply voltage of the MCU is less than 2.4V, the normal operation mode is not allowed. Therefore, Figure 5-61 does not have data for a supply voltage of 1.8 V.



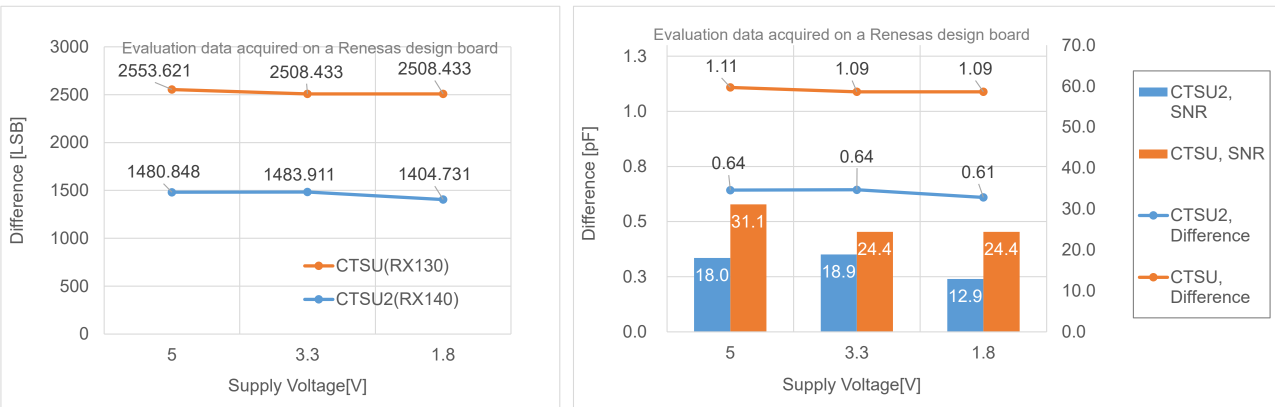
Supply Voltage and Measured Value Detected capacitance difference and SNR

Figure 5-61 Normal Mode Supply Voltage and Sensitivity Characteristics

(2) Low Voltage Mode

Low voltage mode operations indicate conditions in which the CTSU operates with the CTSUCR1.CTSUATUNE0 bit set to ‘1’ for RX130 and the CTSUCRA.ATUNE0 bit is set to ‘1’ for RX140. Not all MCUs support low voltage mode operations. Please confirm whether the MCU you plan on using supports low voltage mode in the corresponding MCU User’s Manual. Operations are not guaranteed when the related registers are set on MCUs that do not support this feature.

- Supply voltage does not cause changes in the measured values or sensitivity.
- The difference in the measured values and SNR of CTSU1 and CTSU2 is due to the difference in measurement time. The measurement time of CTSU2 is about 1/2 that of CTSU1, but the measured value and SNR are about 2/3, so the measurement accuracy per unit time is improved.



Supply voltage and measured value Detected capacitance difference and SNR

Figure 5-62 Low Voltage Mode Supply Voltage and Sensitivity Characteristics

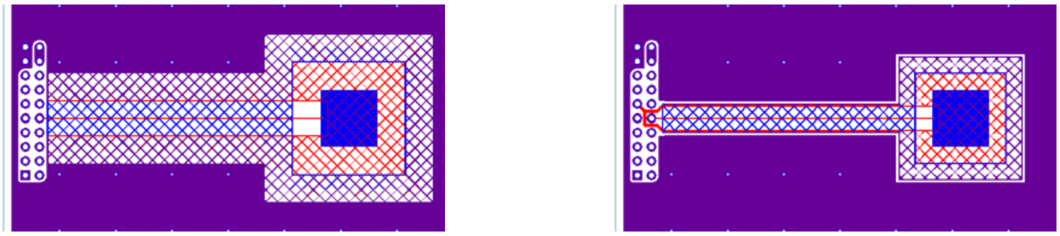
5.3.6.6 Sensitivity at Wire Touch

Table 5-32 lists Board Specifications at Electrode Wire Touch. For evaluation purposes, all other design parameters remained fixed.

Table 5-32 Board Specifications at Electrode Wire Touch

Design Parameter	Specification	Unit	Notes
Shield type	**Cross-hatched GND, active shield**	-	
Overlay panel thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

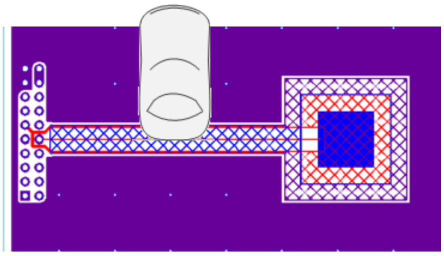
Note: Recommended design values shown in Table 5-5, except as noted.



(a) Cross-hatched GND (b) Active shield

Layer indication ■:Top layer, ■: Bottom layer

Figure 5-63 Evaluation Board Pattern



Note: touch via a 2mm-overlay panel

Figure 5-64 Wire Touch Position

Figure 5-65 shows Sensitivity at Wire Touch. Wire touch on the overlay panel above the shield pattern does not generate a touch-detectable SNR.

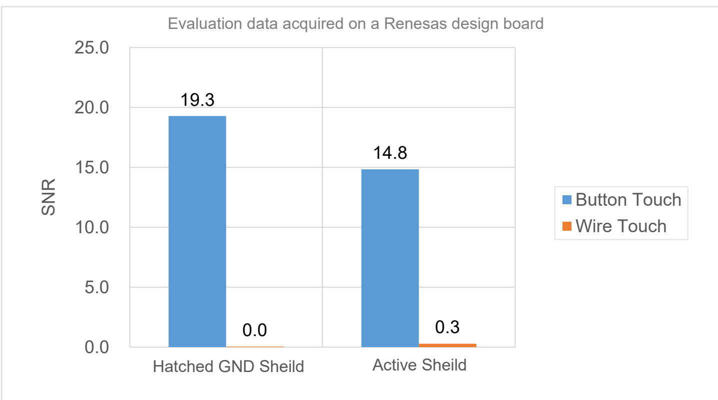


Figure 5-65 Sensitivity at Wire Touch

6. Characteristic Data for Coil Spring Buttons

6.1 Evaluation Criteria

Table 6-1 Hardware Environment

Item	Specification
CPU board	RA2L1 Cap Touch CPU board（RTK0EG0018C01001BJ） （RA2L1 Capacitive Touch Evaluation System（RSSK-RA2L1 / RTK0EG0022S01001BJ）Accessories）
Applied Micro	RA2L1（R7FA2L1AB2DFP）
Operating Frequency	48MHz
Battery	5.0V （Supplied from a stabilized power supply）
Artificial Finger	Φ10.0×50mm stainless steel rod

Table 6-2 Software Development Environment

Item	Specification
Integrated Development Environment	Renesas e² studio Version: 2025-10
Complier	GCC ARM Embedded 13.2
RA FSP	Version 6.2.0
Capacitive Touch Sensor Development Support Tool	QE for Capacitive Touch V4.2.0
Emulator	Renesas E2 emulator Lite

Table 6-3 Software Development Environment

Item	Settings
CTSU Register Setting	Results obtained through automatic adjustment processing of QE's Capacitive Touch. (Sensor drive pulse frequency determined by automatic adjustment; Match clock measurement count: 3 times; measurement time: 0.128 ms × multiple frequency measurement count)
Measurement period	20ms（Generated by the hardware timer (AGT)）
Data acquisition points	1000
Data determination method	Averaging 1000 data package
TS pin parasitic capacitance measurement method	Using the log for the automatic adjustment process of QE for Capacitive Touch
Touch Judgement Method (Method for determining measurement Values in multi-Clock measurement)	Value majority mode (VMM)

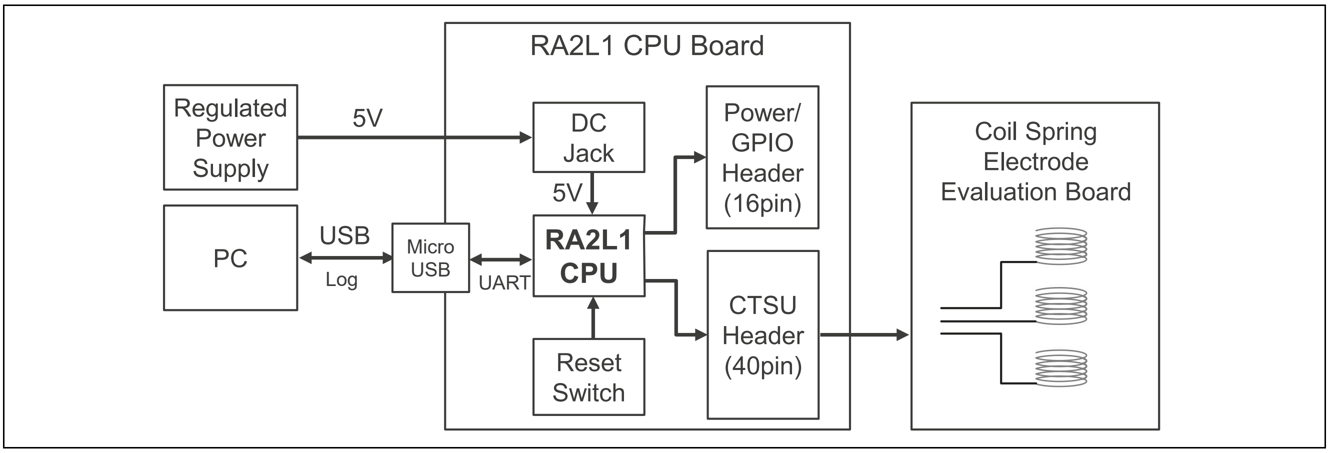
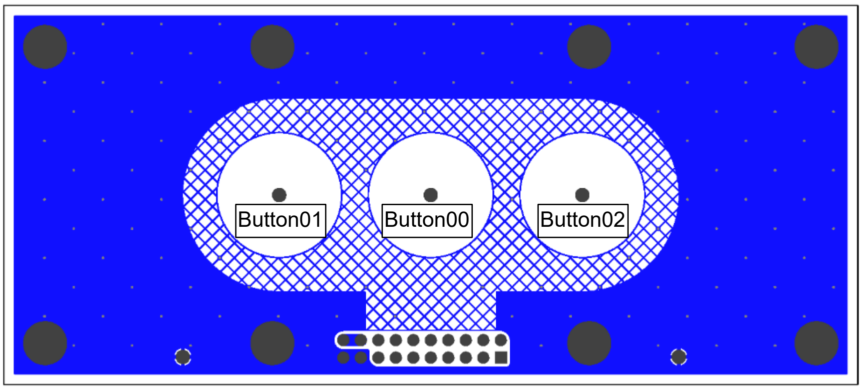
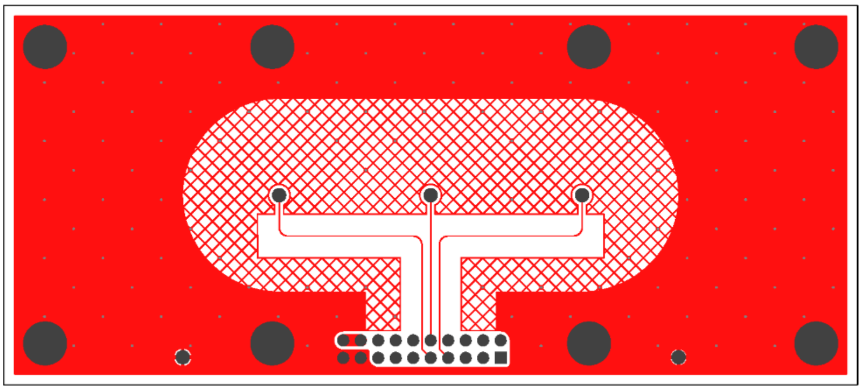


Figure 6-1 Evaluation Board Block Diagram

Figure 6-2 shows an example evaluation board pattern. All boards in this evaluation implemented three buttons.



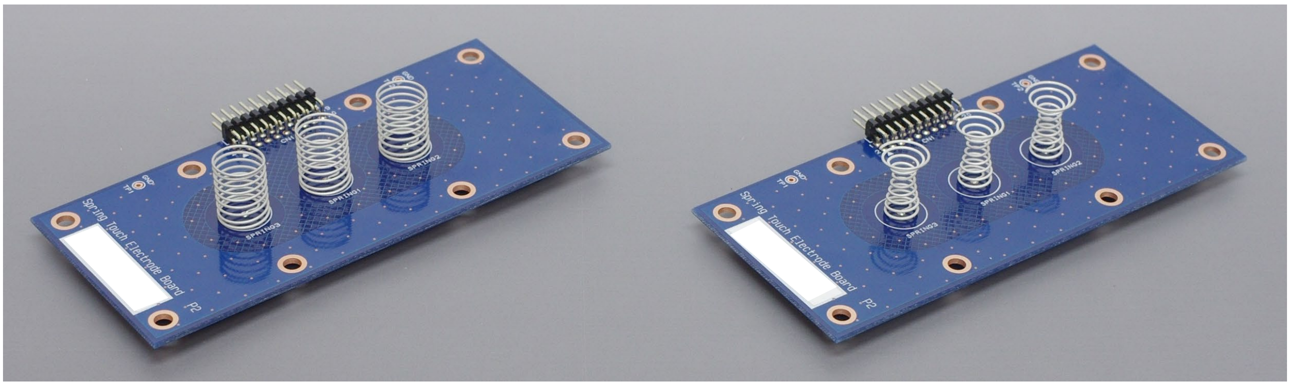
Top Layer



Bottom Layer

Figure 6-2 Example for Evaluation Board Pattern

Figure 6-3 shows examples of coil spring shapes evaluated. In this evaluation, cylindrical and Drum-shape (with a concave touch button section) springs were used. The “drum-shape” mentioned in this guide means the shape of Japanese Tsuzumi Drum or Bongo Drum.



Cylinder-shape Coil Spring Drum-shape Coil Spring

Figure 6-3 Example of Evaluated Coil Spring Shapes

6.2 Design Parameters and Sensitivity Characteristics

6.2.1 Button Size

Table 6-4 shows the board specifications when the button size varies.

Table 6-4 Board Specification for Button Size Variation

Parameter	Specification	Unit	Remark
Touch area size of coil spring (button size)	8、12、16、20	mm	
Distance between touch buttons	10	mm	
Wire diameter of coil spring	0.6	mm	
Winding spacing at the button section of coil spring	0.6	mm	Only drum-shaped
Natural length of coil spring	15.5	mm	
Air gap (distance between substrate and overlay panel)	12.0	mm	
Overlay Panel Thickness	2.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	

Figure 6-4 shows the board pattern when the button size varies.

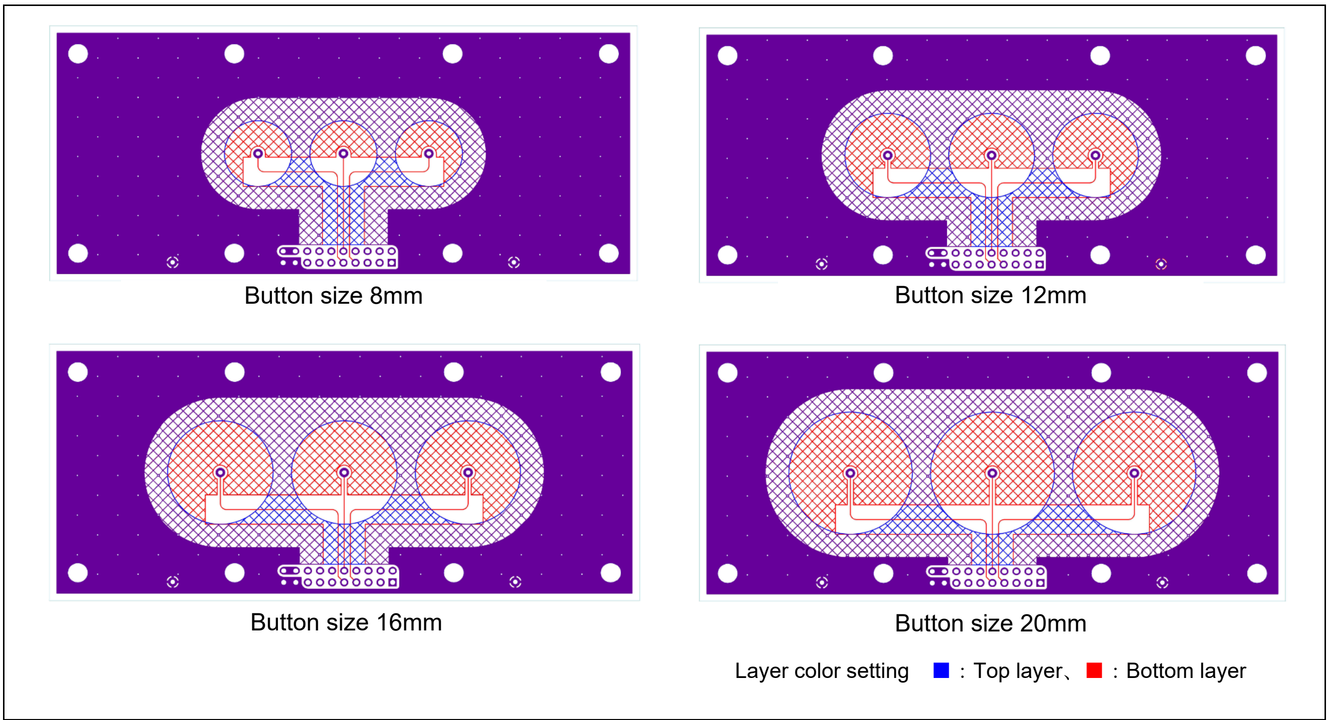


Figure 6-4 Evaluation Board for Button Size Variation

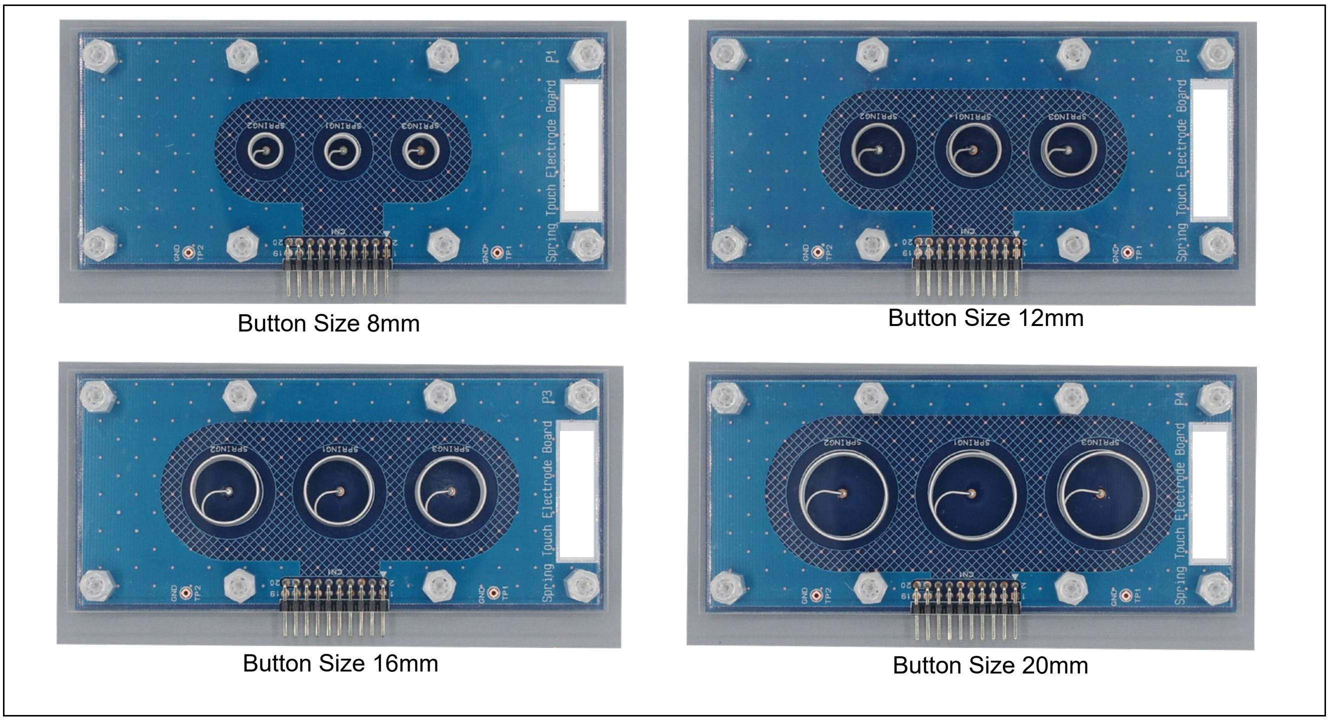


Figure 6-5 Button Size Appearance of Cylindrical Coil Springs

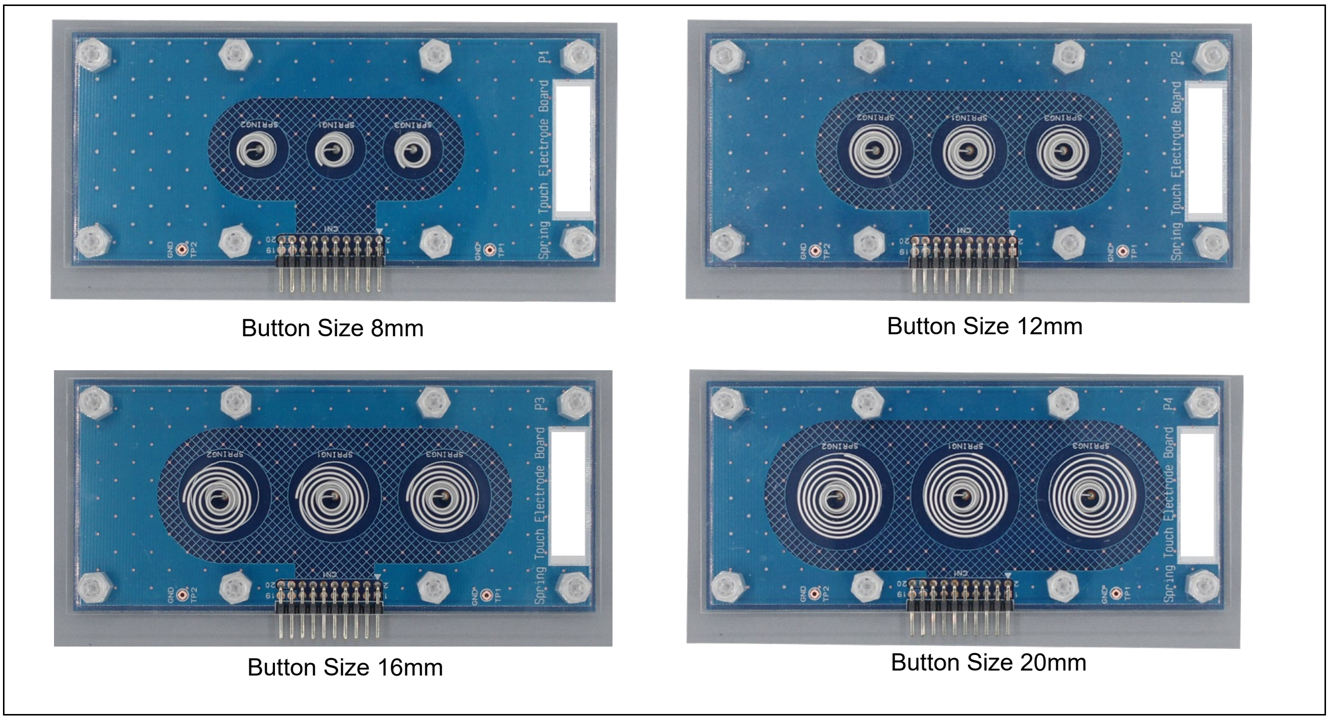
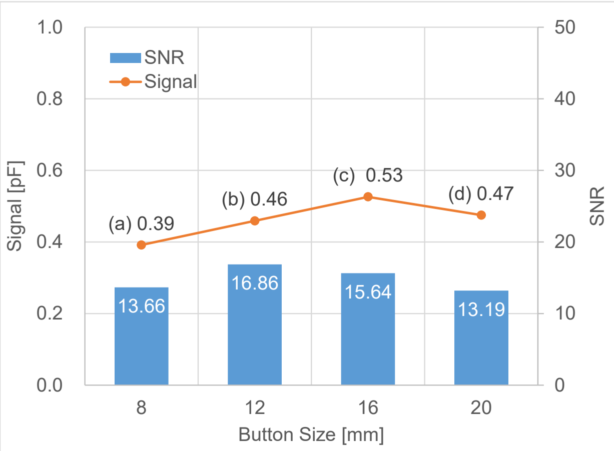


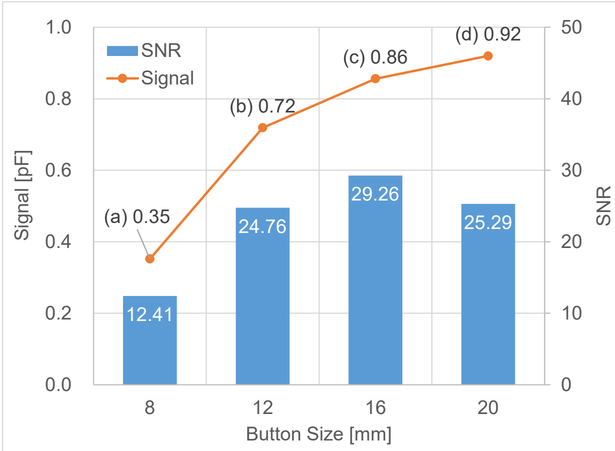
Figure 6-6 Button Size Appearance of Drum-Type Coil Springs

Figure 6-7 shows the SNR characteristics when the button size varies.

- Cylindrical designs without wire filling inside the button cavity exhibit reduced SNR as the button size increases, since the distance between the pseudo finger and the coil spring increases
- Drum-shaped design features spiral-shaped wire filling downside the button. This increases the contact area with the finger, resulting in higher signal values compared to cylindrical designs. Signal values tend to increase as the button size becomes larger. However, button size is also a factor that increases parasitic capacitance, and the SNR may decrease when the sensor drive pulse frequency is reduced. In this evaluation, the sensor drive pulse frequency is 2.69 MHz for button sizes from 8 mm to 12 mm, and 2.29 MHz for the 20 mm button



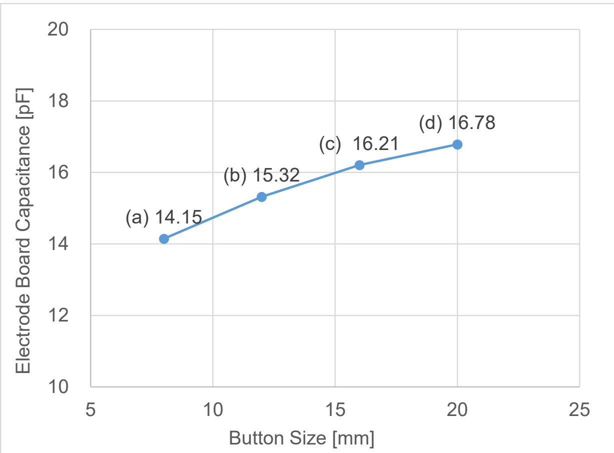
Cylinder-shape coil spring with ring shape button



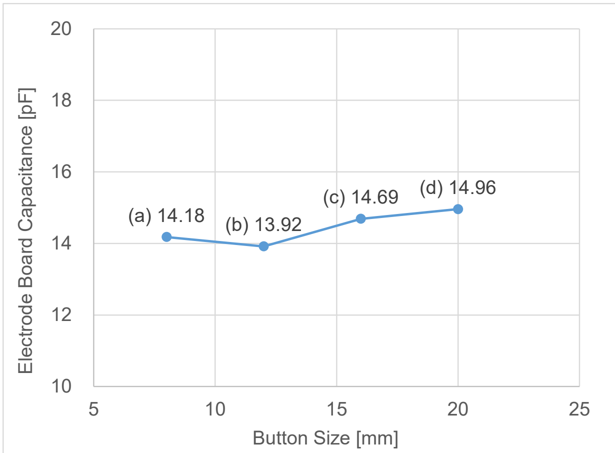
Drum-shape coil spring with spiral shape button

Figure 6-7 SNR Characteristic

Figure 6-8 shows the parasitic capacitance of the touch OFF function when the button size varies. This parasitic capacitance includes approximately 10.79 pF from the CPU board.



Cylinder-shape spring connected with ring shape button



Drum-shape spring connected with spiral shape button

Figure 6-8 Parasitic Capacitance during Touch Off

6.2.2 Button Crosstalk

Table 6-5 shows the board specifications for button crosstalk evaluation.

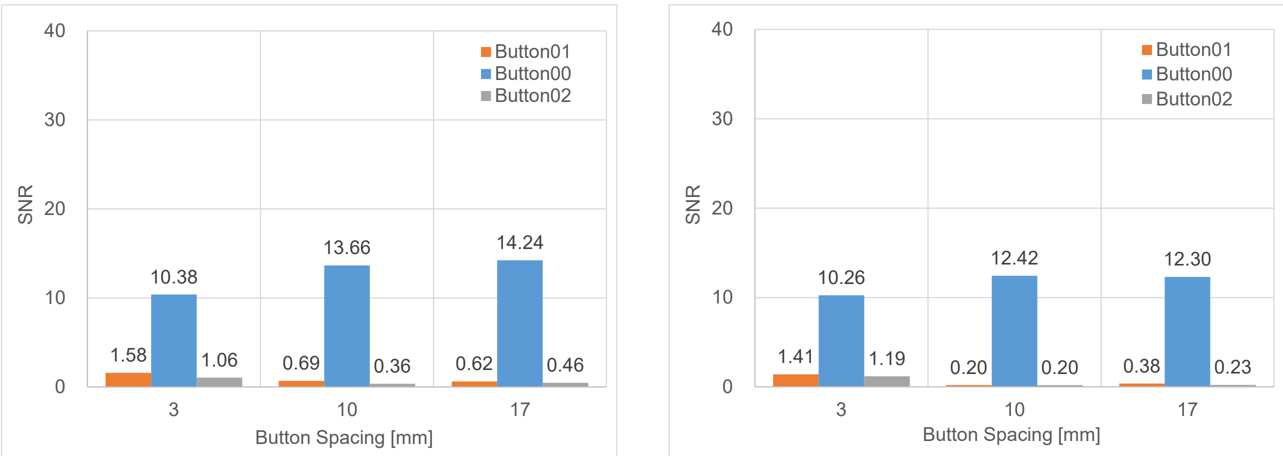
Table 6-5 Board Specifications for Button Crosstalk Evaluation

Parameter	Specification	Unit	Remark
Touch area size of coil spring (button size)	8、12、16、20	mm	
Distance between touch buttons	3、10、17	mm	
Wire diameter of coil spring	0.6	mm	
Winding spacing at the button section of coil spring	0.6	mm	Only drum-shaped
Natural length of coil spring	15.5	mm	
Air gap (spacer between substrate and overlay panel)	12.0	mm	
Overlay Panel Thickness	2.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	

6.2.2.1 Button Size 8mm

Figure 6-9 shows the crosstalk characteristics for buttons with an 8 mm size.

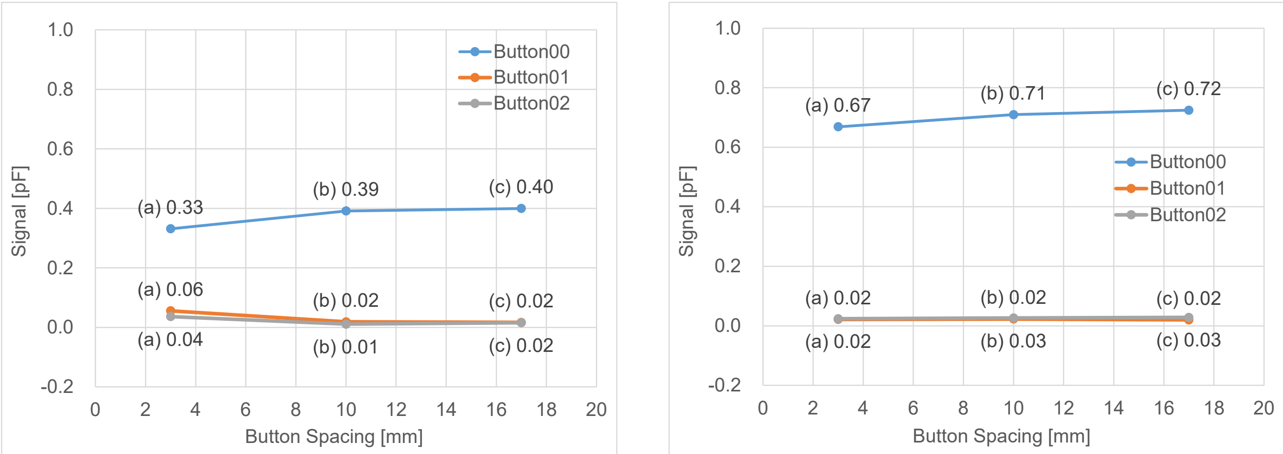
- When the distance between buttons is 3mm, crosstalk occurs to adjacent buttons, but no false responses are detected. Furthermore, the capacitance is divided due to capacitive coupling between adjacent buttons and the Pseudo finger, causing the signal value of the pressed button to decrease and the SNR to also decrease.



Cylinder-shape Drum-shape

Figure 6-9 Crosstalk characteristics (SNR) when Pressing 8mm Button00

Figure 6-10 shows the crosstalk characteristics when pressing Button00 with an 8mm button size.

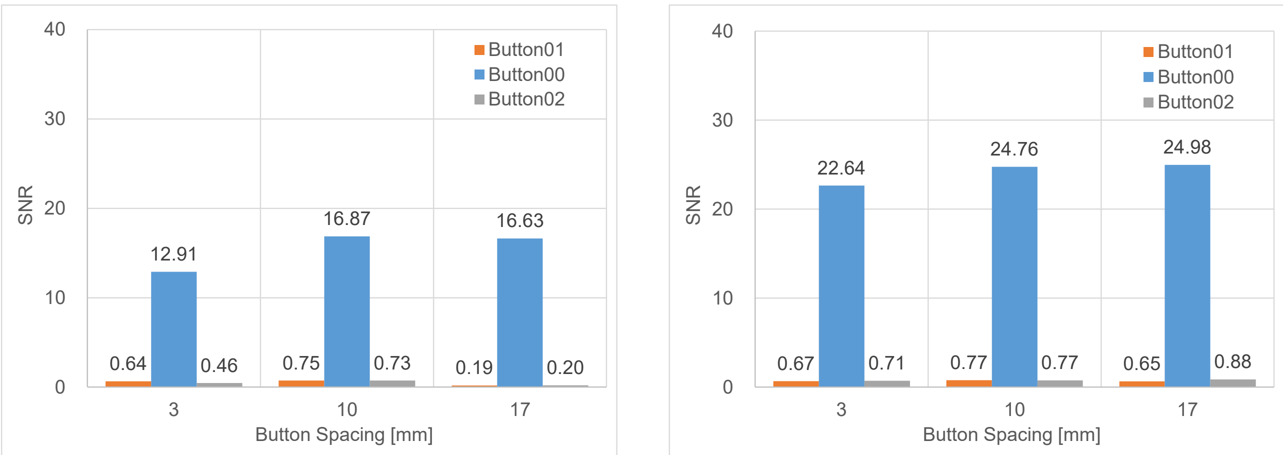


Cylinder-shape Drum-shape

Figure 6-10 Crosstalk characteristics (Signal value [pF]) when Pressing 8mm Button00

6.2.2.2 Button Size 12mm

- Even with only 3 mm spacing between buttons, no crosstalk was observed between adjacent buttons. However, capacitive coupling between adjacent buttons and the pseudo finger likely caused capacitance division, resulting in a decrease in the pressed button's signal value and a corresponding reduction in SNR.



Cylinder-shape Drum-shape

Figure 6-11 Crosstalk Characteristics (SNR) when Pressing 12mm Button00

Figure 6-12 shows the crosstalk characteristics when pressing Button00 with a button size of 12 mm.

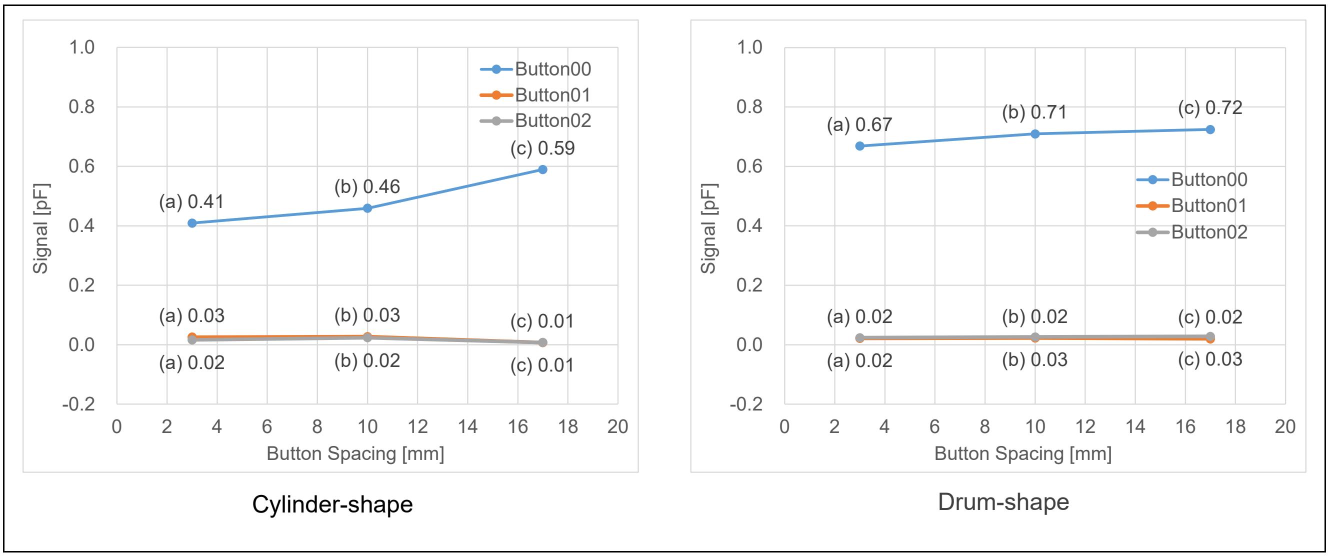


Figure 6-12 Crosstalk Characteristics (Signal value [pF]) when Pressing 12mm Button00

6.2.2.3 Button Size 16mm

- Even with only 3 mm spacing between buttons, no crosstalk was observed between adjacent buttons. However, capacitive coupling between adjacent buttons and the pseudo finger likely caused capacitance division, resulting in reduced signal values for pressed buttons and decreased SNR.

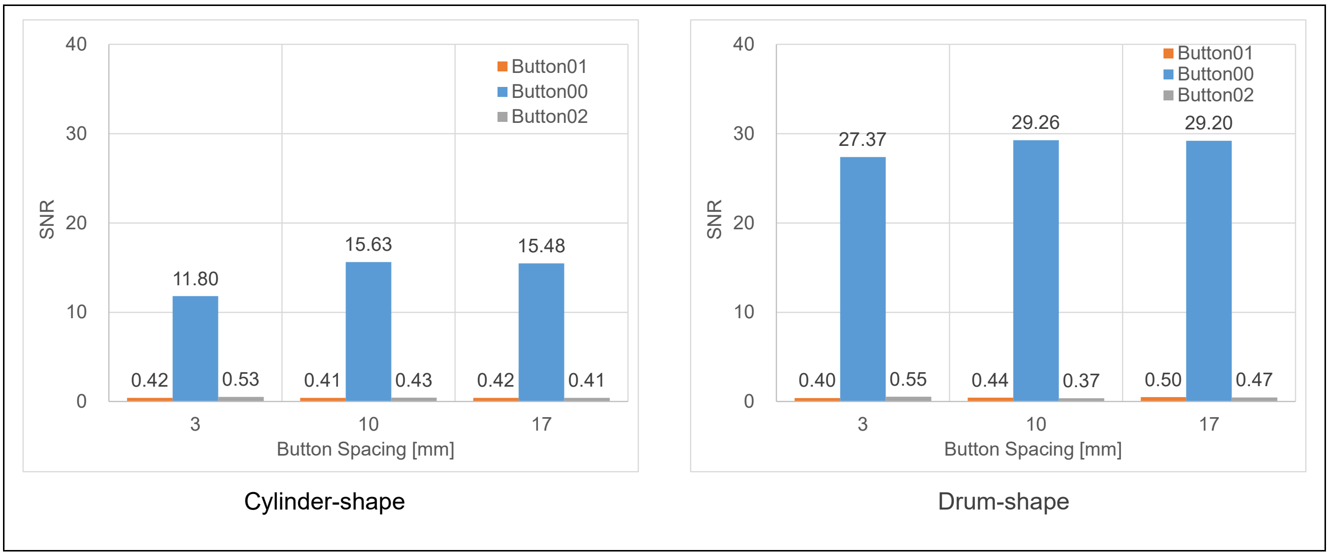


Figure 6-13 Crosstalk Characteristics (SNR) when Pressing 16mm Button00

Figure 6-14 shows the crosstalk characteristics when pressing Button00 whose button size is 16 mm.

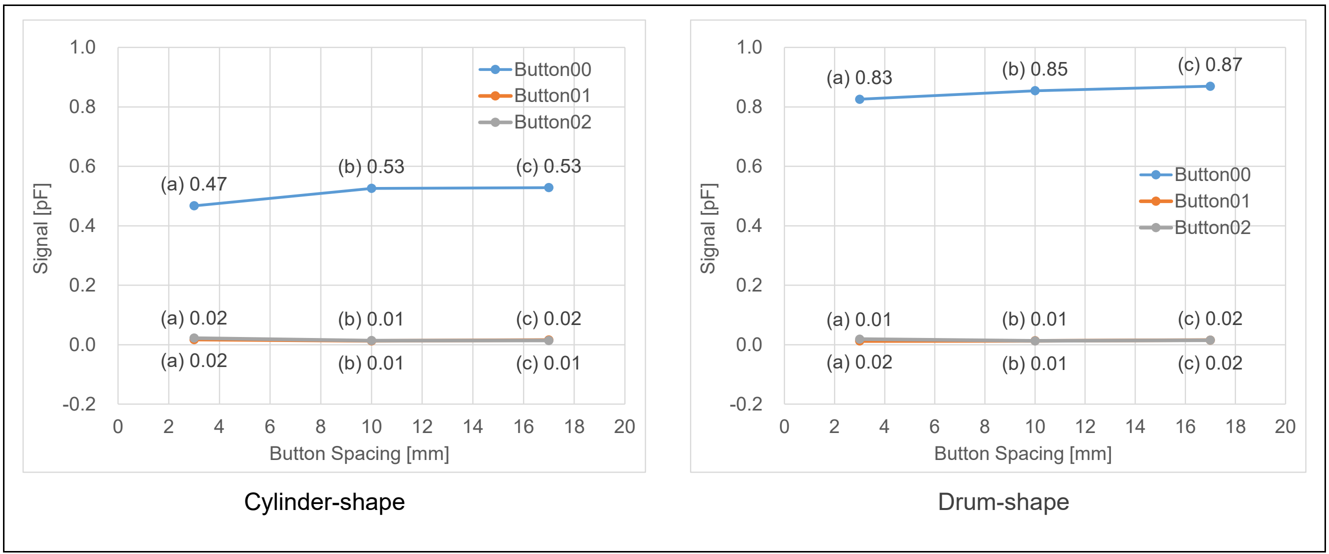


Figure 6-14 Crosstalk Characteristics (Signal value [pF]) when Pressing 16mm Button00

6.2.2.4 Button Size 20mm

- Even with only 3 mm spacing between buttons, no crosstalk was observed between adjacent buttons, there was no effect from capacitance division due to capacitive coupling between adjacent buttons and the simulated finger.

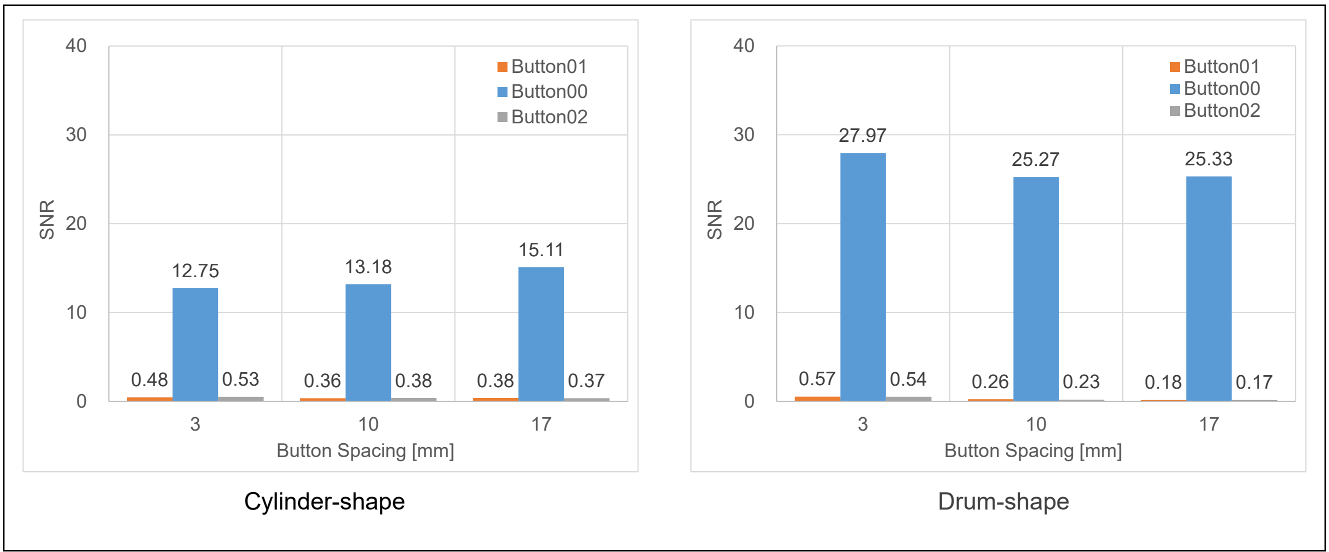


Figure 6-15 Crosstalk Characteristics (SNR) when Pressing 20mm Button00

Figure 6-16 shows the crosstalk characteristics when pressing Button00 whose button size is 20 mm.

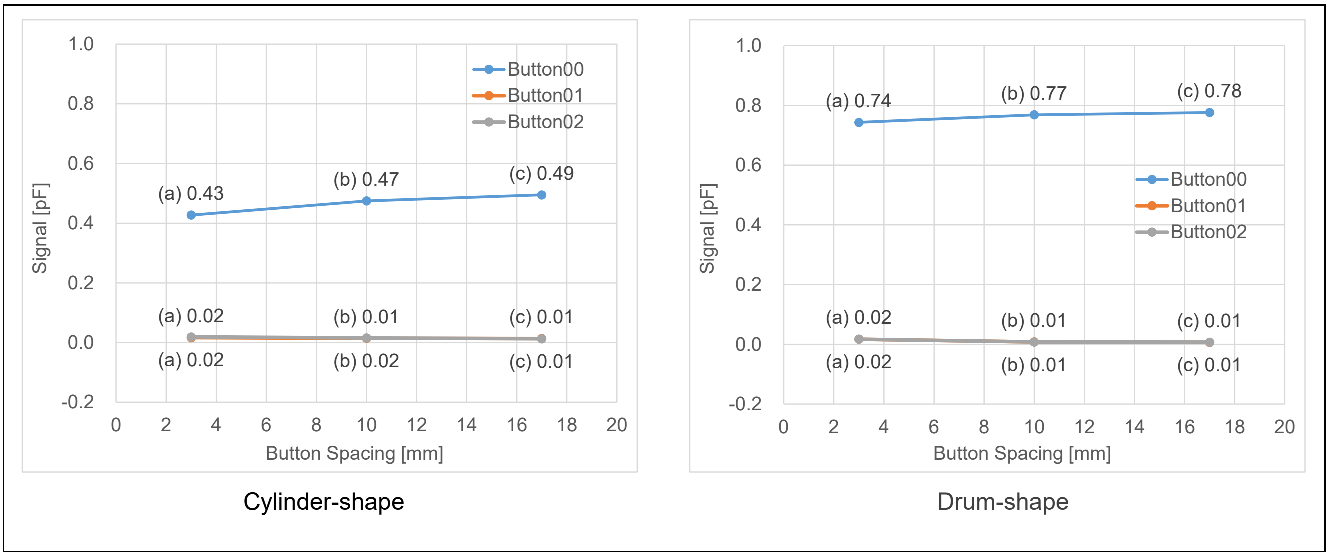


Figure 6-16 Crosstalk Characteristics (Signal value [pF]) when Pressing 20mm Button00

6.2.3 Air Gap

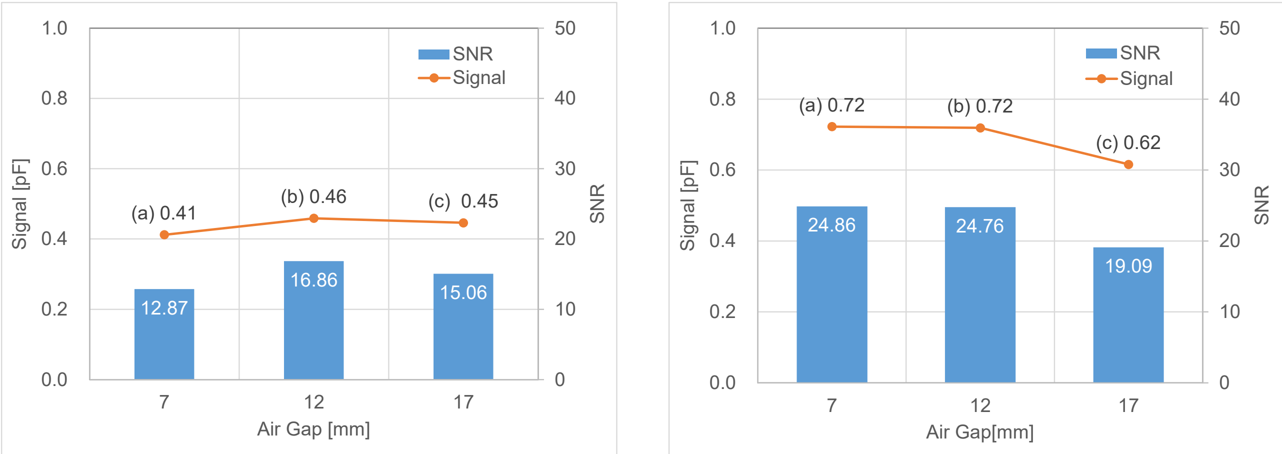
Table 6-6 shows the substrate specifications during air gap fluctuations.

Table 6-6 Board Specifications for Air Gap Variation

Parameter	specification	Unit	Remark
Touch area size of coil spring (button size)	12	mm	
Distance between touch buttons	10	mm	
Wire diameter of coil spring	0.6	mm	
Winding spacing at the button section of coil spring	0.6	mm	Only Drum-shape
Natural length of coil spring	10.5、15.5、18.5	mm	
Air gap (spacer between substrate and overlay panel)	7.0、12.0、17.0	mm	
Overlay Panel Thickness	2.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	

Figure 6-17 shows the SNR characteristics during air gap fluctuations.

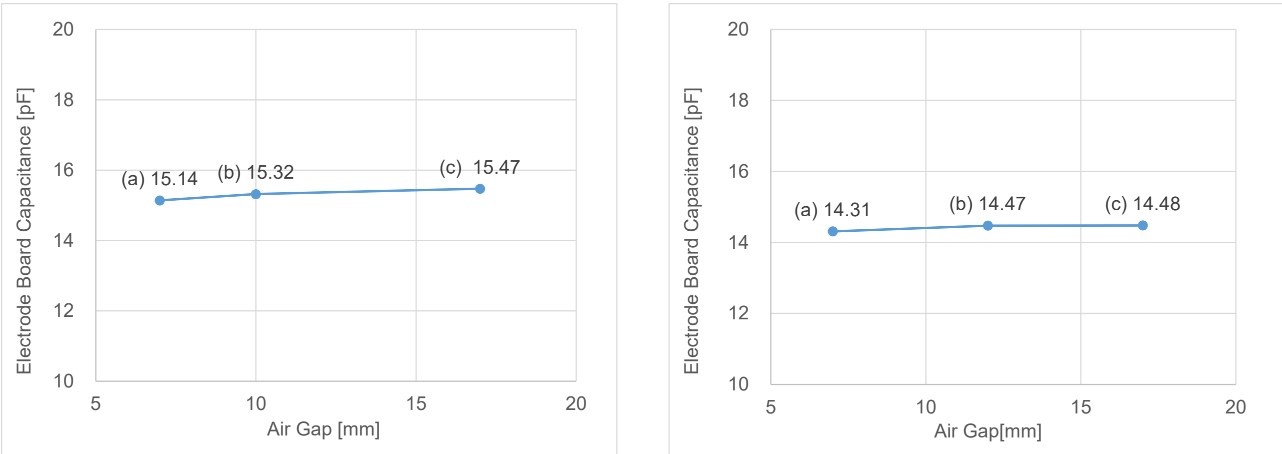
- Using a coil spring ensures sufficient SNR even when an air gap is present.
  For the SNR characteristics related to the PCB electrode pads and the air gap, refer to "Figure 5-50 Overlay Panel Air Gap and Sensitivity Characteristics"



Cylinder-shape Drum-shape

Figure 6-17 SNR Characteristic

Figure 6-18 shows the parasitic capacitance during touch OFF when the air gap varies. This parasitic capacitance includes approximately 10.79 pF from the CPU board.



Cylinder-shape Drum-shape

Figure 6-18 Touch-OFF parasitic capacitance

6.2.4 Overlay Panel Thickness

Table 6-7 shows the substrate specifications when the overlay panel thickness varies.

Table 6-7 Board Specifications for Overlay Panel Thickness Variation

Parameter	Specification	Unit	Remark
Touch area size of coil spring (button size)	12	mm	
Distance between touch buttons	10	mm	
Wire diameter of coil spring	0.6	mm	
Winding spacing at the button section of coil spring	0.6	mm	Only Drum-shape
Natural length of coil spring	15.5	mm	
Air gap (spacer between substrate and overlay panel)	12.0	mm	
Overlay Panel Thickness	2.0、4.0、6.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	

Figure 6-19 shows the SNR characteristics when the thickness of the overlay panel varies.

- Using a coil spring ensures sufficient SNR even when an air gap is present.
  Signal values and SNR degradation may occur depending on the overlay panel thickness.
- When the coil spring's interior is not filled with a helical shape (cylindrical type), the impact of thickness on SNR degradation becomes stronger. Filling with a helical shape, SNR degradation tends to be more gradual.

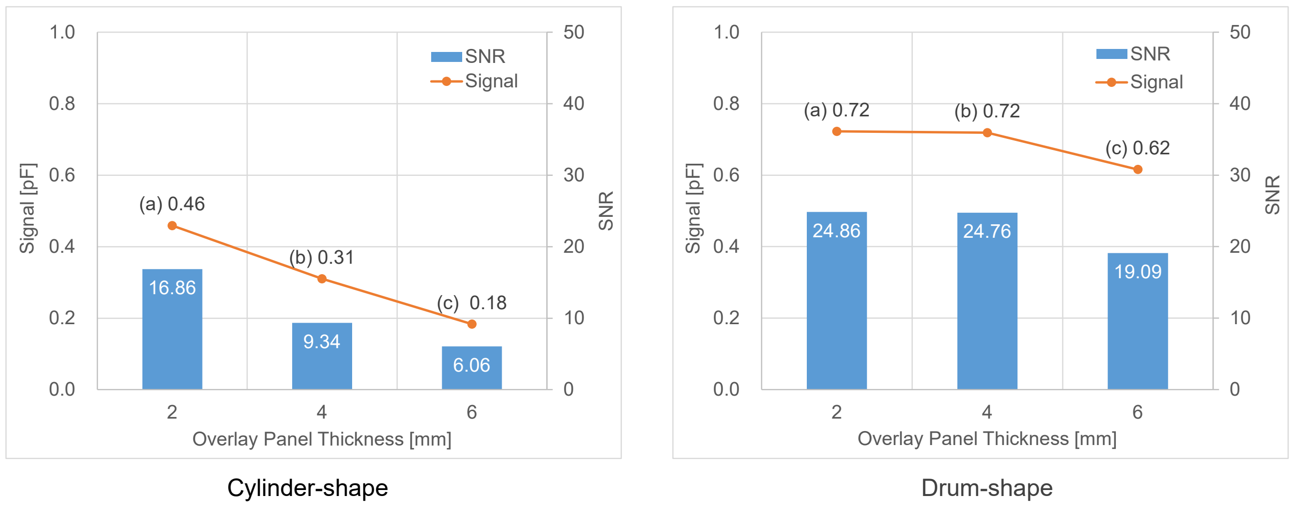


Figure 6-19 SNR Characteristic

Figure 6-20 shows the parasitic capacitance during touch OFF for the overlay panel thickness evaluation. This parasitic capacitance includes approximately 10.79 pF from the CPU board.

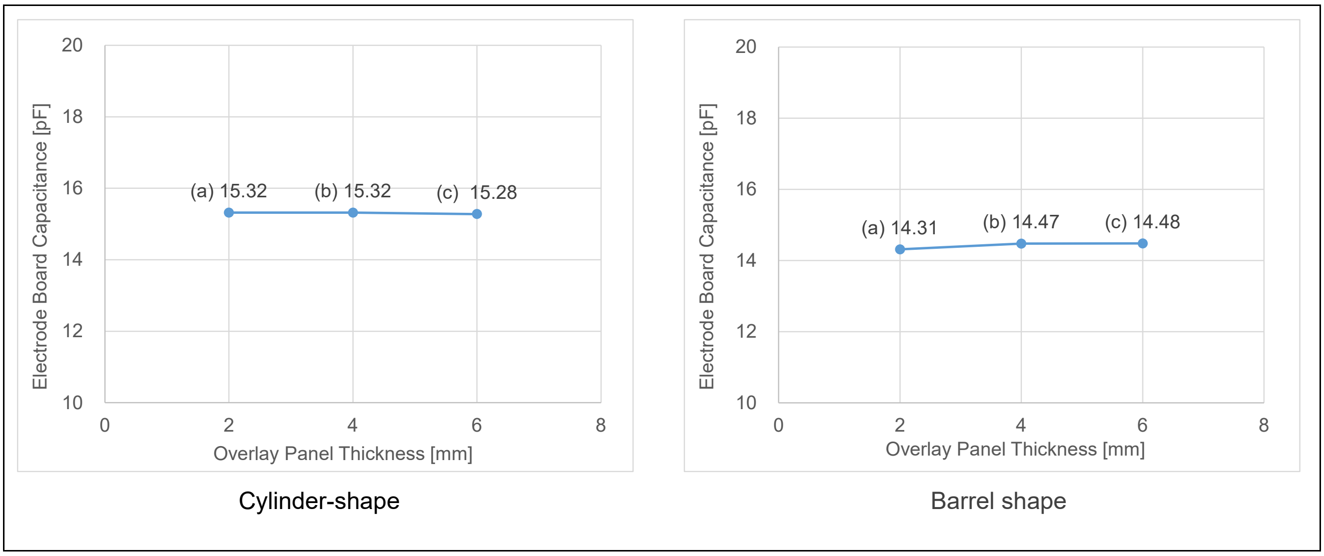


Figure 6-20 Touch-OFF parasitic capacitance

6.2.5 Spring Wire Diameter

Table 6-8 shows the substrate specifications when the Wire diameter of coil spring varies.

Table 6-8 Board Specifications for Wire Diameter Variation of Coil Spring

Parameter	Specification	Unit	Remark
Touch area size of coil spring (button size)	12.0	mm	
Distance between touch buttons	10.0	mm	
Wire diameter of coil spring	0.3、0.6、0.9	mm	
Winding spacing at the button section of coil spring	0.3、0.6、0.9	mm	Only Drum-shape
Natural length of coil spring	15.5	mm	
Air gap (spacer between substrate and overlay panel)	12.0	mm	
Overlay Panel Thickness	2.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	

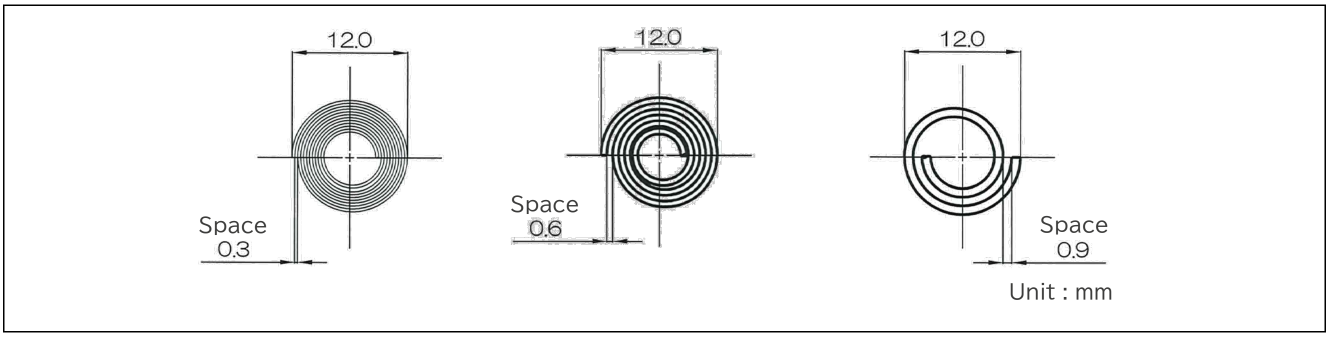


Figure 6-21 Design of the Touch Button Section for Coil Spring Wire Diameter Evaluation

Figure 6-22 shows the SNR characteristics when the Wire diameter of coil spring varies.

- There is a tendency for SNR to increase or decrease depending on the coil spring wire diameter.

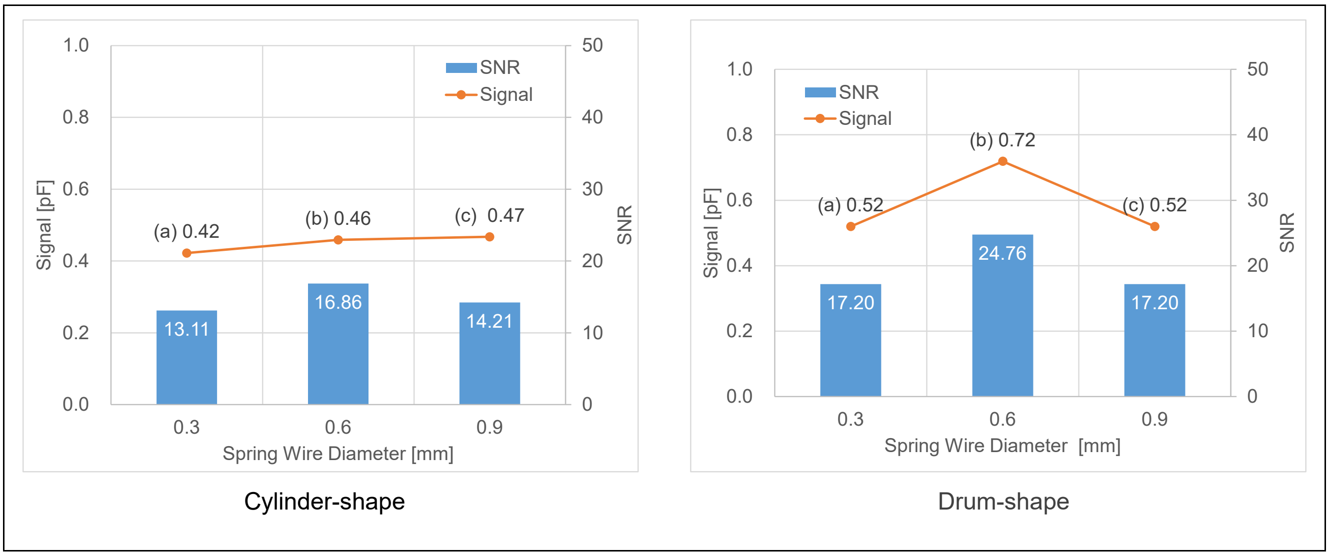


Figure 6-22 SNR Characteristic

Figure 6-23 shows the touch-off parasitic capacitance for Wire diameter of coil spring evaluation. This parasitic capacitance includes approximately 10.79 pF from the CPU board.

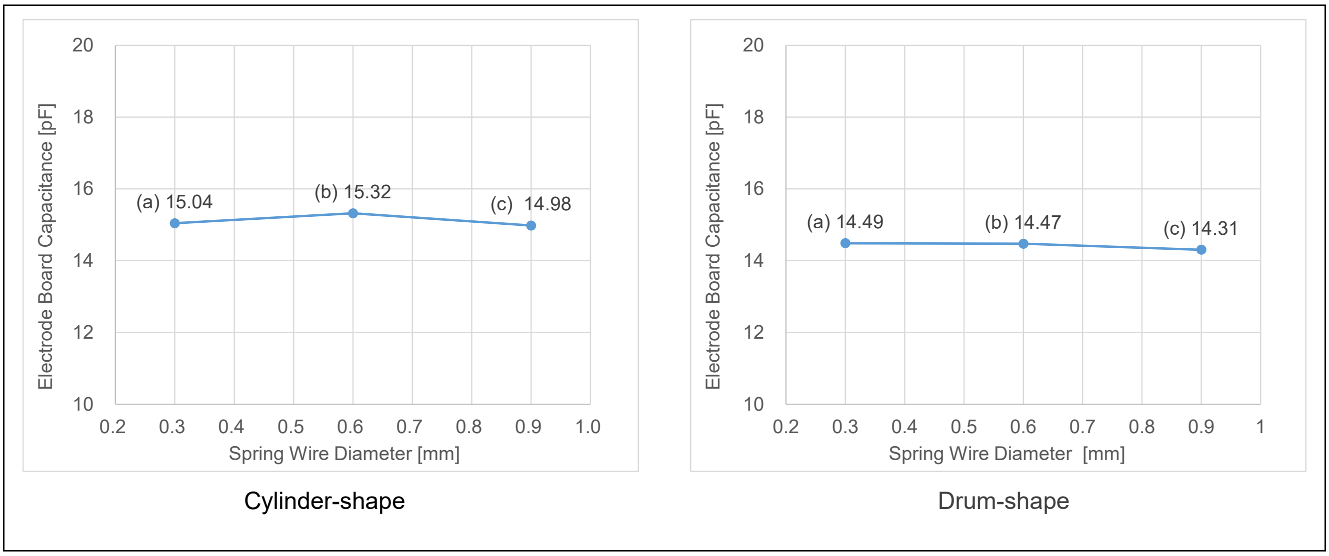


Figure 6-23 Touch-OFF parasitic capacitance

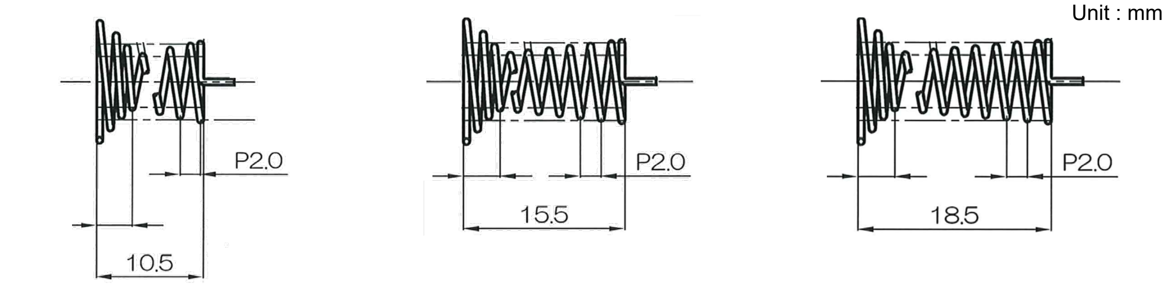
6.2.6 Spring Compression

Table 6-9 shows the board specifications when the coil spring compression varies.

Table 6-9 Board Specifications for Compression Variation of Coil Spring

Parameter	Specification	Unit	Remark
Touch area size of coil spring (button size)	12.0	mm	
Distance between touch buttons	10.0	mm	
Wire diameter of coil spring	0.6	mm	
Winding spacing at the button section of coil spring	0.6	mm	Only Drum-shape
Conditions for coil springs (natural length of coil spring)	(1)10.5 (2)15.5 (3)18.5	mm	The spring pitch (value P shown in Figure 6-24) is standardized at 2.0 mm
Air gap (spacer between substrate and overlay panel)	7.0	mm	
Overlay Panel Thickness	2.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	

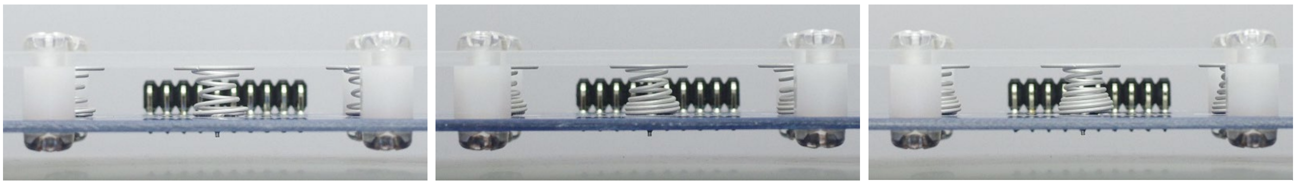
Figure 6-24 shows the conditions for the coil spring.



(1) Natural length 10.5mm (2) Natural length 15.5mm (3) Natural length 18.5mm

Figure 6-24 Conditions for Coil Springs (Drum-shape example)

Figure 6-25 shows the spring compression evaluation board.



Natural Length 10.5mm Natural Length 15.5mm Natural Length 18.5mm

Figure 6-25 Evaluation board with spring pitch variation (Drum-shape)

Figure 6-26 shows SNR characteristics when the Wire diameter of coil spring varies.

- The narrower the pitch in the natural length direction of the coil spring, the greater the tendency for SNR to improve.

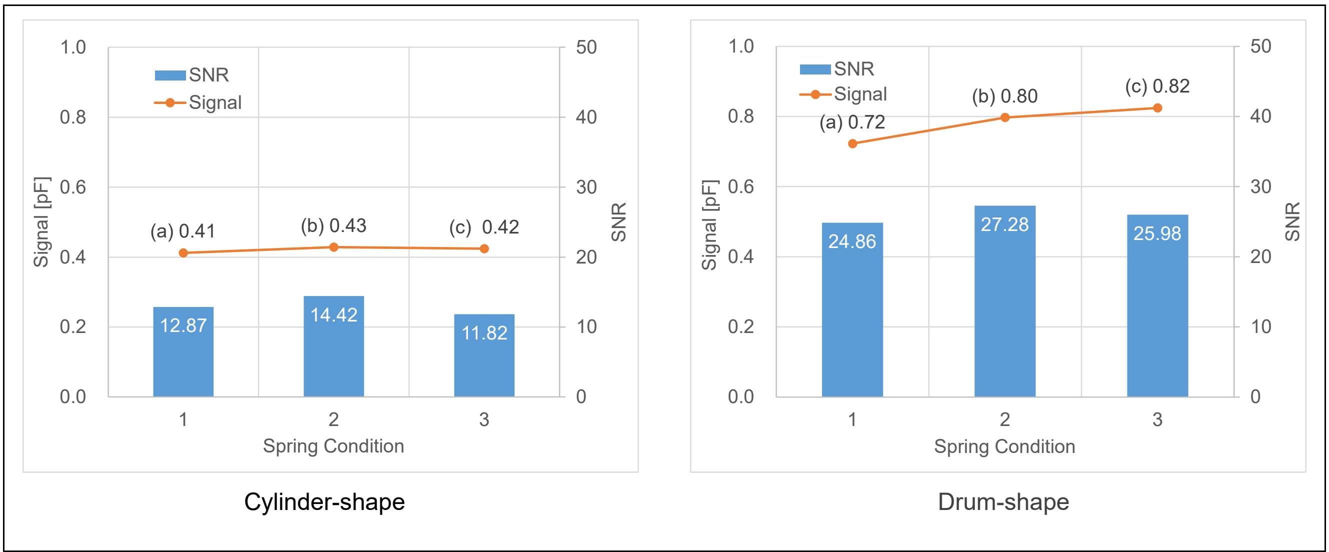


Figure 6-26 SNR Characteristic

Figure 6-27 shows parasitic capacitance variation with the Wire diameter of coil spring during Touch-OFF mode. This parasitic capacitance includes approximately 10.79 pF from the CPU board.

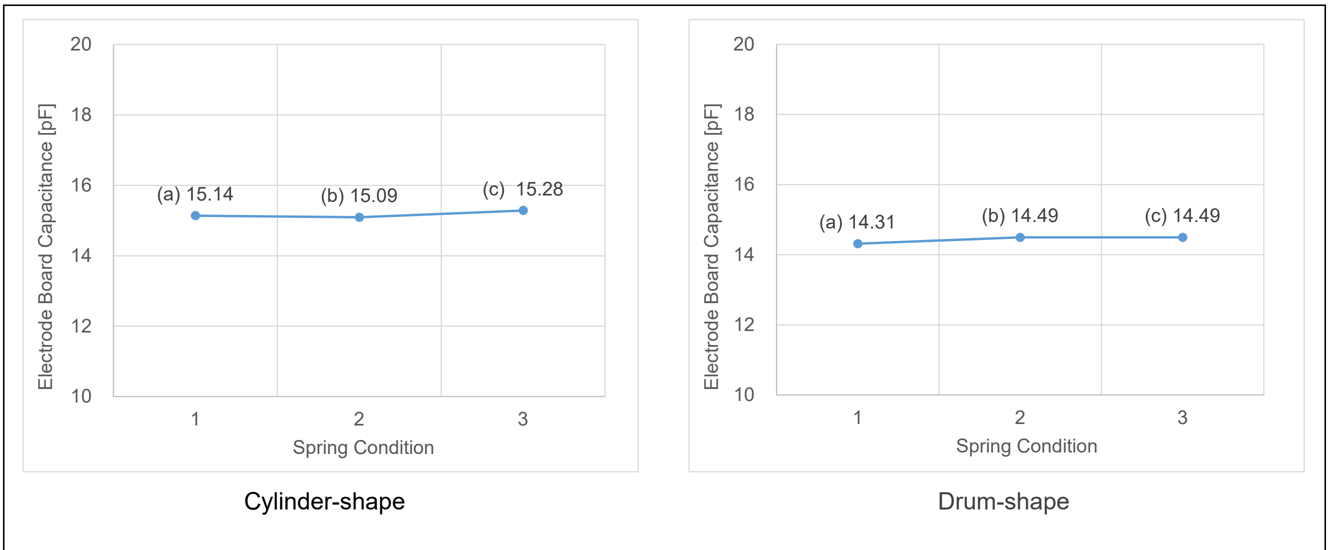


Figure 6-27 Touch-OFF parasitic capacitance

6.2.7 Button Spiral Winding Density

Table 6-10 shows the board specifications for the button section winding density evaluation.

Table 6-10 Board Specifications for Button Section Spiral Winding Evaluation

Parameter	Specification	Unit	Remark
Touch area size of coil spring (button size)	12	mm	
Distance between touch buttons	10	mm	
Wire diameter of coil spring	0.6	mm	
Winding spacing at the button section of coil spring	0.1、0.6、1.2	mm	Only Drum-shape
Natural length of coil spring	15.5	mm	
Air gap (spacer between substrate and overlay panel)	12.0	mm	
Overlay Panel Thickness	2.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	

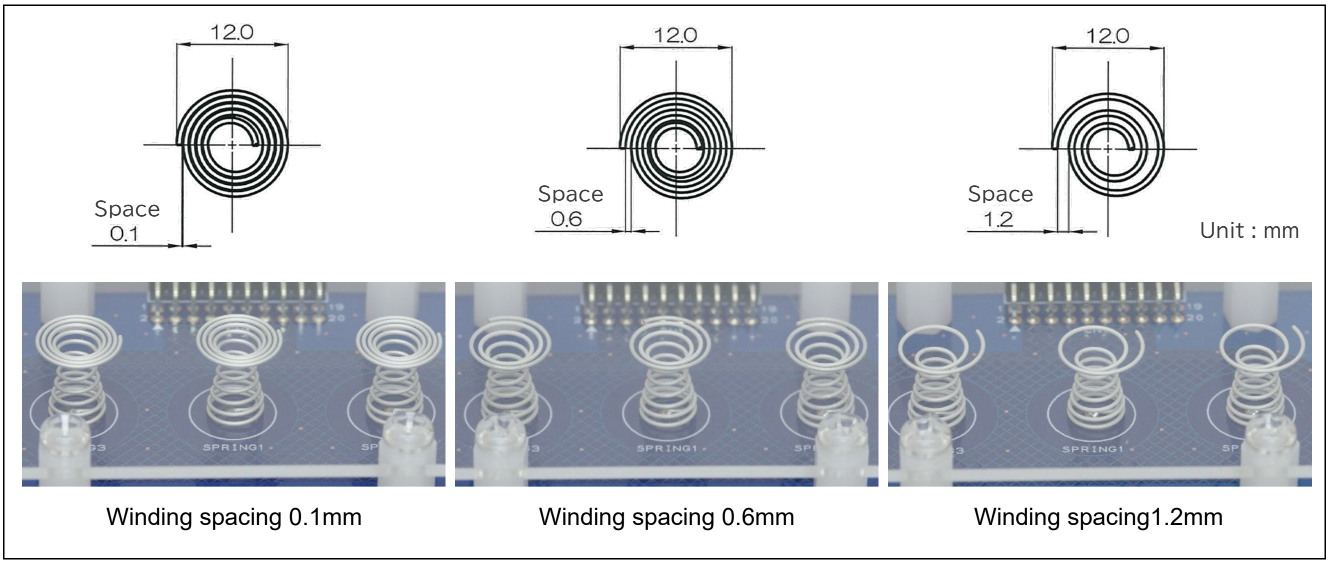


Figure 6-28 Evaluation board with variable spring pitch (drum-shape)

Figure 6-29 shows the SNR characteristics evaluation for winding spacing of button section.

- The narrower the spiral line spacing in the button, the SNR becomes better.

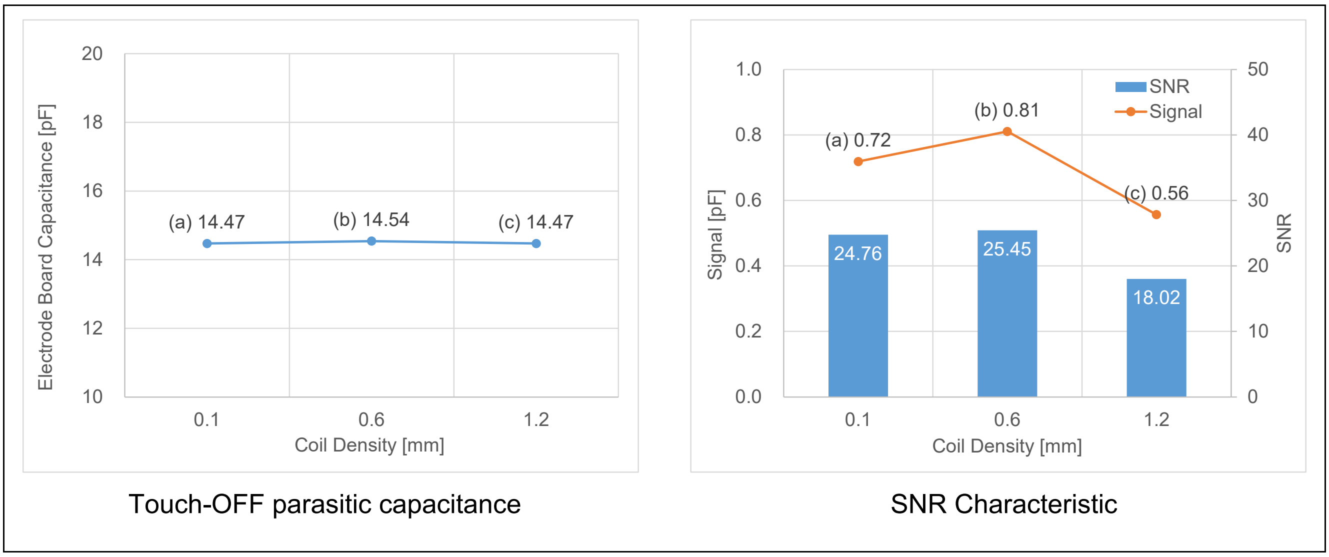


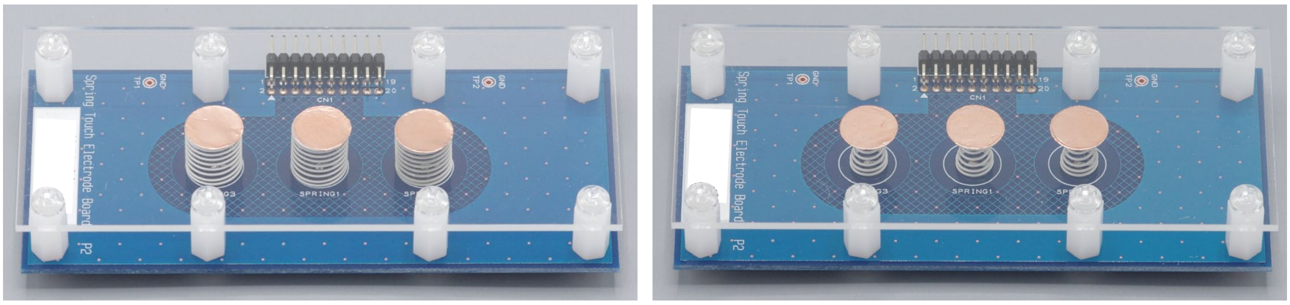
Figure 6-29 Evaluation Result

6.2.8 Touch Surface Metal Pad

Table 6-11 shows the board specifications with and without touch surface metal pads.

Table 6-11 Board Specification for Touch Surface Metal Pad Presence/Absence

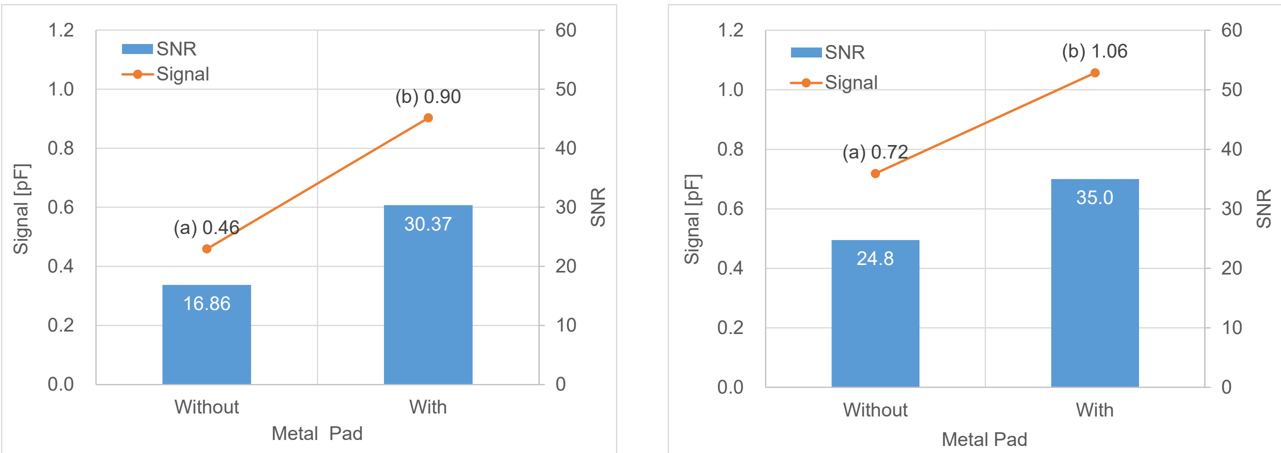
Parameter	Specification	Unit	Remark
Coil spring and overlay panel contact surface metal pad size	12.0	mm	Attach the circular copper foil tape to the overlay panel
Touch area size of coil spring (button size)	12	mm	
Distance between touch buttons	10	mm	
Wire diameter of coil spring	0.6	mm	
Winding spacing at the button section of coil spring	0.1、0.6、1.2	mm	Only Drum-shape
Natural length of coil spring	15.5	mm	
Air gap (spacer between substrate and overlay panel)	12.0	mm	
Overlay Panel Thickness	2.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	



Cylinder-shape coil spring Drum-shape coil spring

Figure 6-30 Metal Pad Evaluation Board

Figure 6-31 shows the SNR characteristics with and without a metal pad on the touch surface. Installing a metal pad (conductor) between the coil spring and the overlay panel improves the SNR.



Cylinder-shape Drum-shape

Figure 6-31 SNR Characteristic

Figure 6-32 shows the touch-off parasitic capacitance with and without the touch surface metal pad placement. The parasitic capacitance includes approximately 10.79 pF from the CPU board.

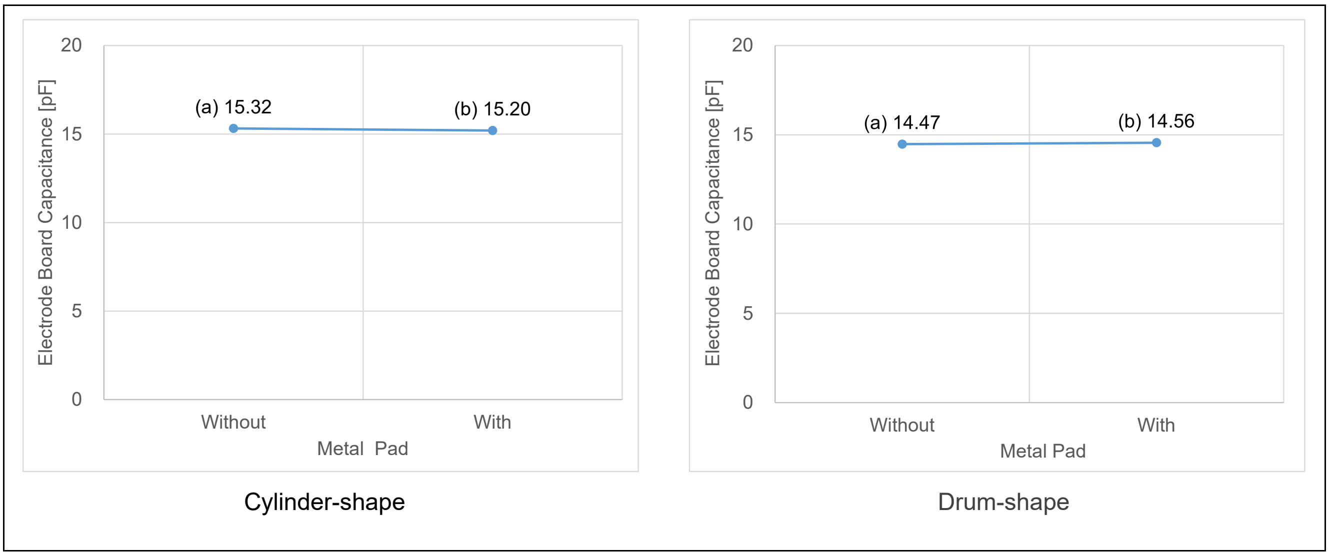


Figure 6-32 Touch-OFF parasitic capacitance

6.2.9 Shielding Pattern Directly related to Coil Spring

Table 6-12 shows the board specifications with and without shielding patterns directly beneath the coil spring.

Table 6-12 Board Specifications for Presence/Absence of Shielding Pattern Directly Below Coil Spring

Parameter	Specification	Unit	Remark
Touch area size of coil spring (button size)	12	mm	
Distance between touch buttons	10	mm	
Wire diameter of coil spring	0.6	mm	
Winding spacing at the button section of coil spring	0.1、0.6、1.8	mm	Only Drum-shape
Natural length of coil spring	15.5	mm	
Air gap (spacer between substrate and overlay panel)	12.0	mm	
Overlay Panel Thickness	2.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	

Figure 6-33 shows the PCB patterns with and without shielding patterns directly beneath the coil spring.

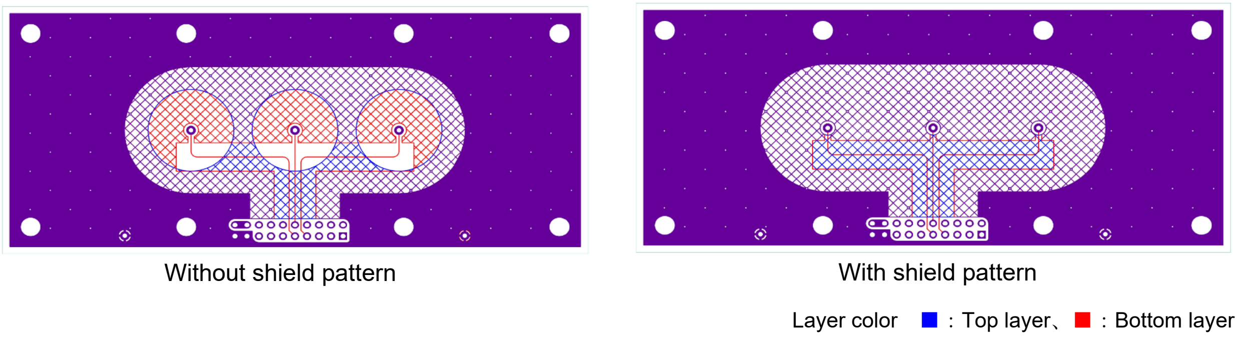


Figure 6-33 Evaluation board for assessing the presence or absence of a shield pattern directly beneath the coil spring

Figure 6-34 shows the SNR characteristics with and without a shield pattern directly beneath the coil spring. Placing a mesh pattern shield directly beneath the coil spring reduces the SNR.

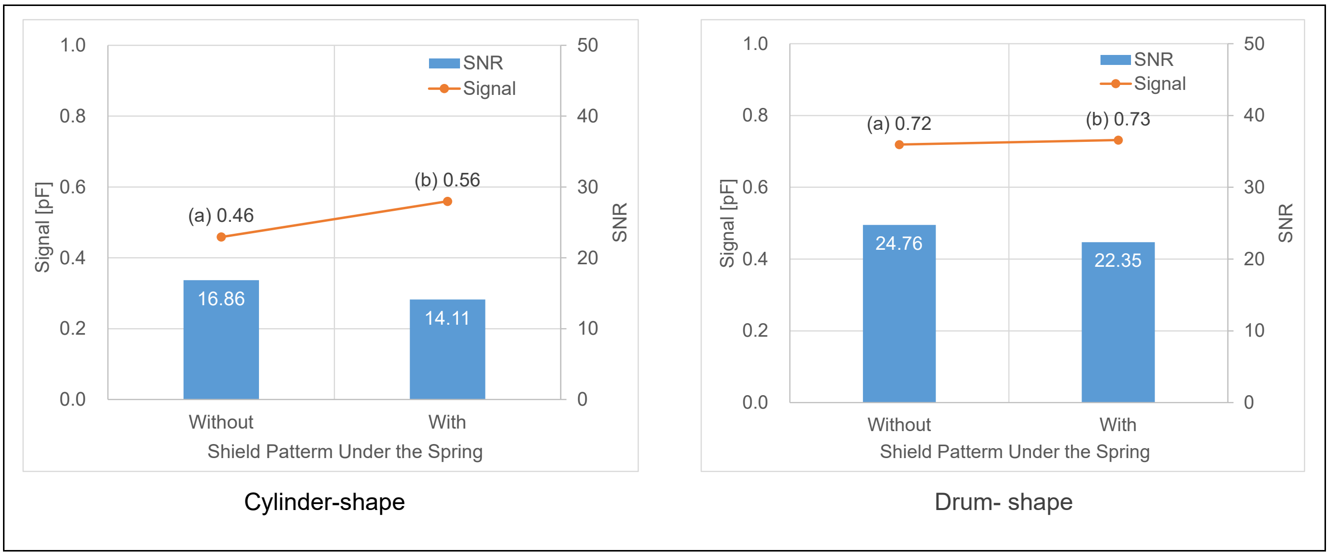


Figure 6-34 SNR Characteristic

Figure 6-35 shows the touch-off parasitic capacitance with and without the shield pattern directly beneath the coil spring. This parasitic capacitance includes approximately 10.79 pF from the CPU board.

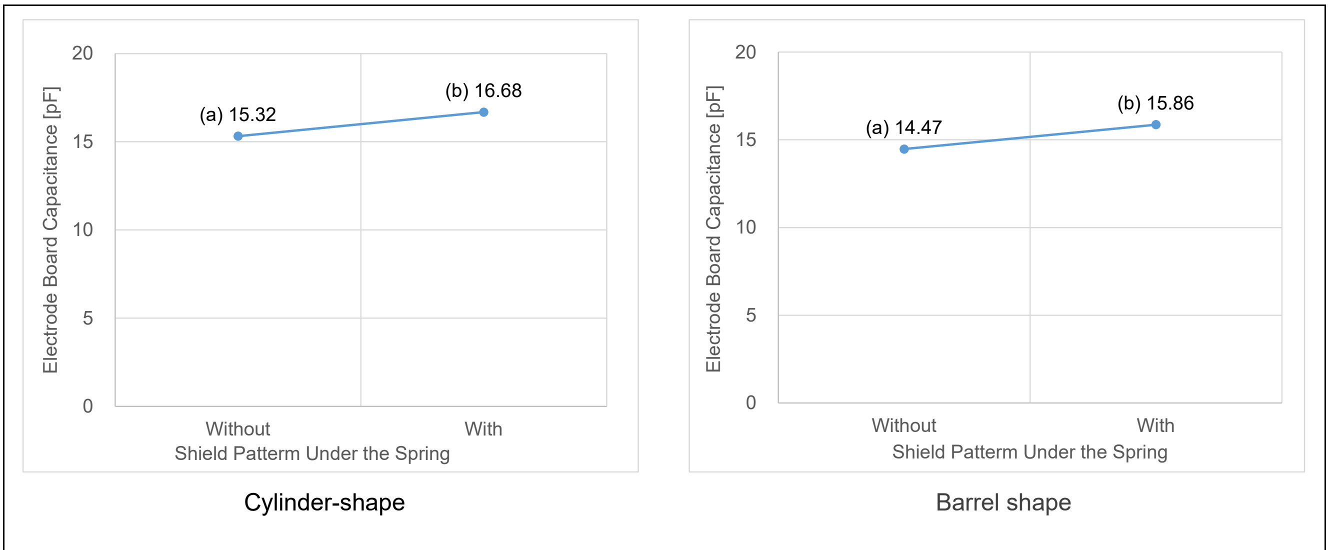


Figure 6-35 Touch-OFF parasitic capacitance

6.2.10 Active Shield

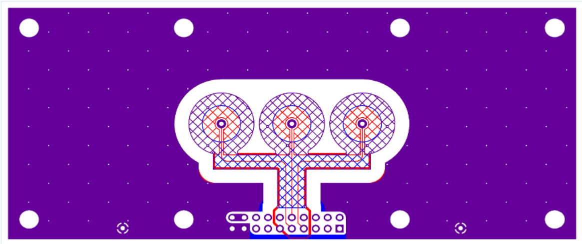
Table 6-13 shows the board specifications related to active shield.

Table 6-13 Design Parameter List for Active Shield

Parameter	Specification	Unit	Remark
Active Shield Pattern Width	1.0、3.0、5.0	mm	
Touch area size of coil spring (button size)	12	mm	
Distance between touch buttons	10	mm	
Wire diameter of coil spring	0.6	mm	
Winding spacing at the button section of coil spring	0.1、0.6、1.8	mm	Only Drum-shape
Natural length of coil spring	15.5	mm	
Air gap (spacer between substrate and overlay panel)	12.0	mm	
Overlay Panel Thickness	2.0	mm	Acrylic material
PCB - Desktop Spacer	5.0	mm	

6.2.10.1 Distance Between Buttons for 3mm

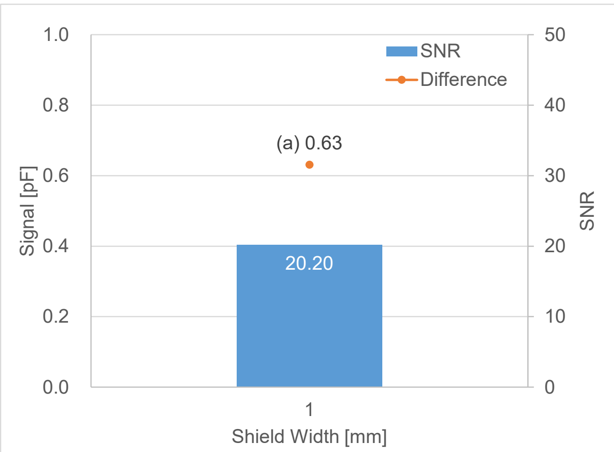
Figure 6-36 shows the pattern of the active shield evaluation board with a distance between buttons of 3 mm.



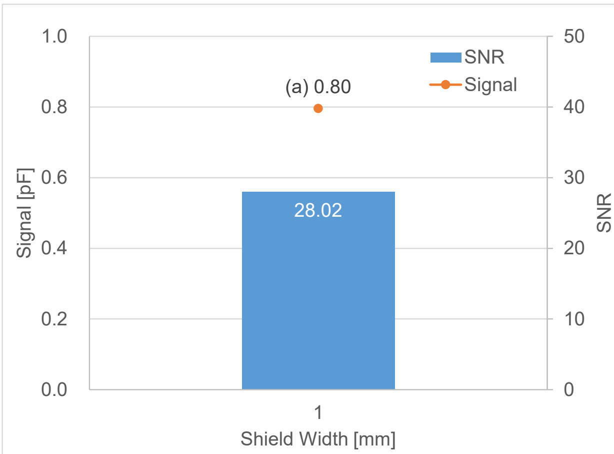
Layer color:
■ : Top layer ■ : Bottom layer

Figure 6-36 Active Shield Evaluation Board Pattern with 3mm Distance Between Buttons (a)

Figure 6-37 shows the SNR characteristics with a distance between buttons of 3 mm. Due to the narrow distance between buttons, widening the active shield width causes it to merge with the shield pattern of adjacent buttons. The CTSU sensor drive pulse frequency is often limited by the capacitance of the shield terminals. Widening the shield width increases capacitance, necessitating a lower sensor drive pulse frequency setting. In such cases, the SNR may decrease.



Cylinder-shape



Drum-shape

Figure 6-37 SNR Characteristics

Figure 6-38 shows the touch-off parasitic capacitance with a distance between buttons of 3 mm. This parasitic capacitance includes approximately 10.79 pF (Button00) from the CPU board.

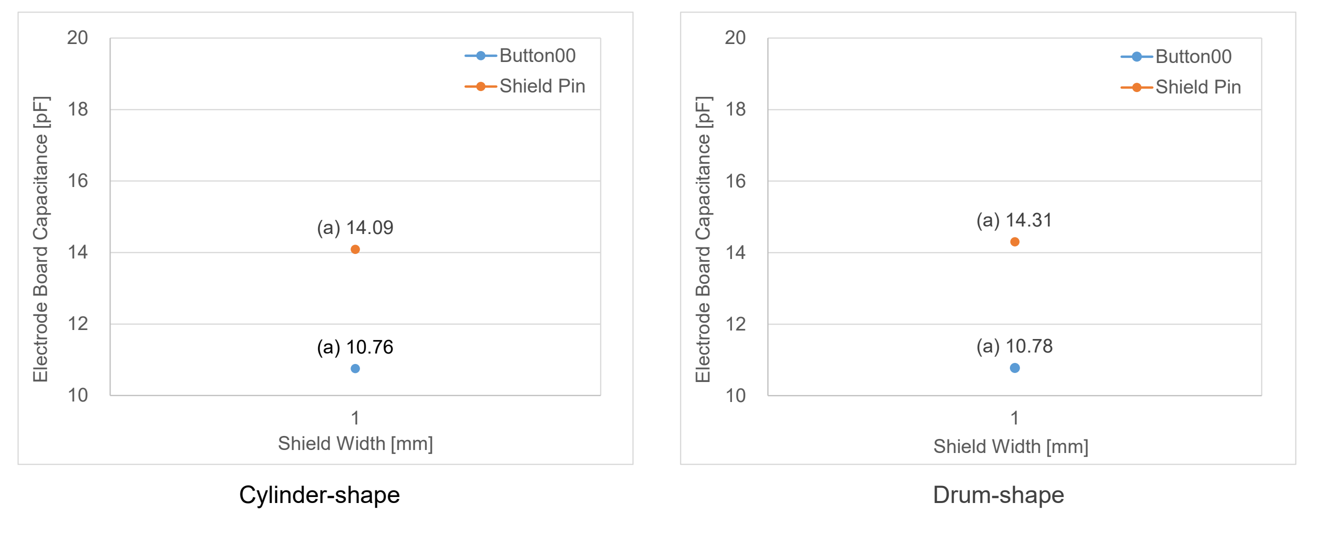


Figure 6-38 Touch-OFF parasitic capacitance

6.2.10.2 Distance Between Buttons for 10mm

Figure 6-39 shows the pattern of the active shield evaluation board with a distance between buttons of 10 mm.

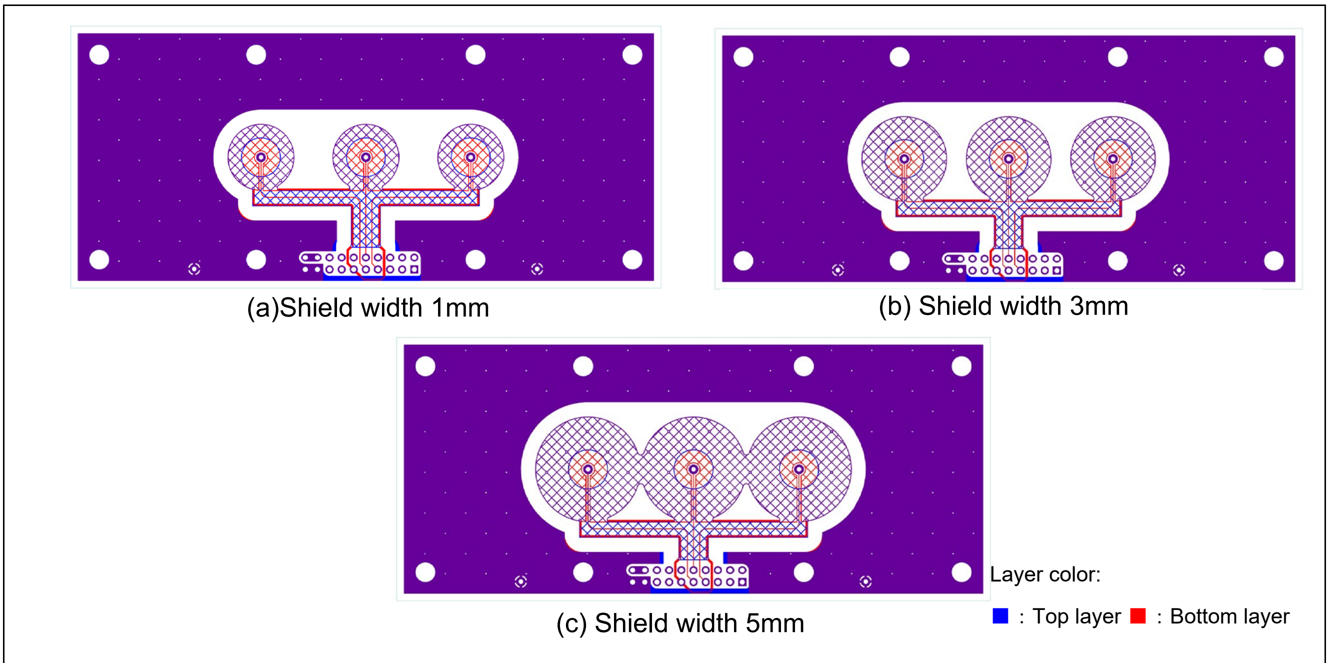


Figure 6-39 Active Shield Evaluation Board Pattern with 10mm Distance Between Buttons

Figure 6-40 shows the SNR characteristics for a 10mm distance between buttons.

- The width of the active shield has little effect on SNR. However, the CTSU sensor drive pulse frequency is often limited by the capacitance of the shield terminals. Increasing the shield width raises capacitance, requiring a lower sensor drive pulse frequency setting. In such cases, SNR may decrease.

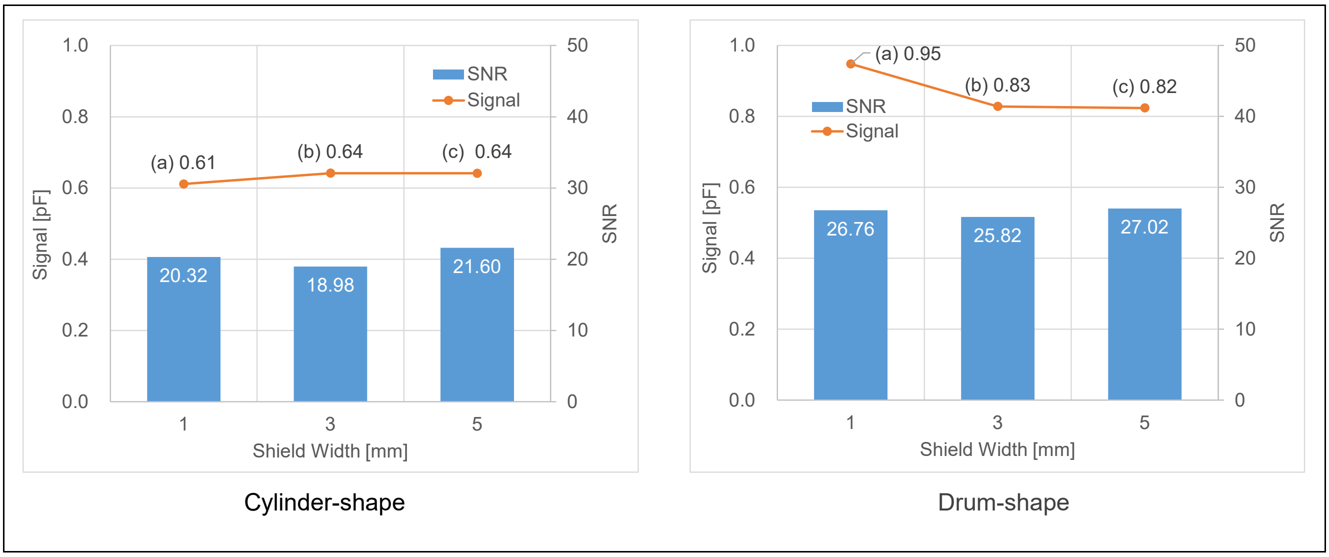


Figure 6-40 SNR Characteristics

Figure 6-41 shows the touch-off parasitic capacitance with a distance between buttons of 10 mm. This parasitic capacitance includes approximately 10.79 pF (Button00) from the CPU board.

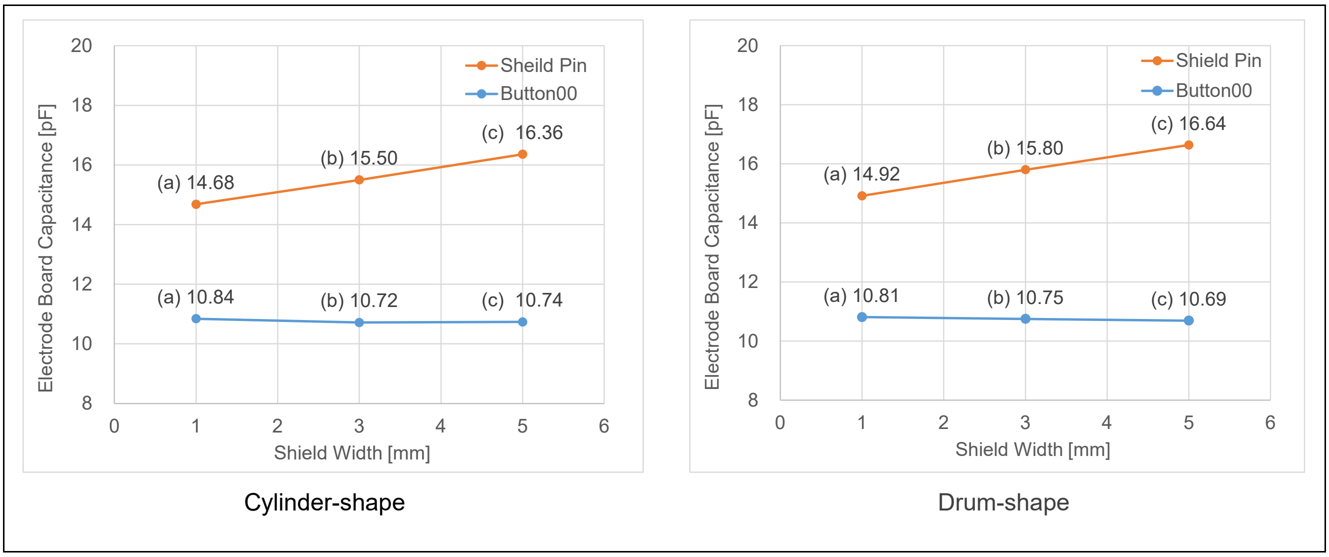


Figure 6-41 Touch-OFF parasitic capacitance

6.2.10.3 Distance Between Buttons for 17mm

Figure 6-42 shows the pattern of the active shield evaluation board with a distance between buttons of 17 mm.

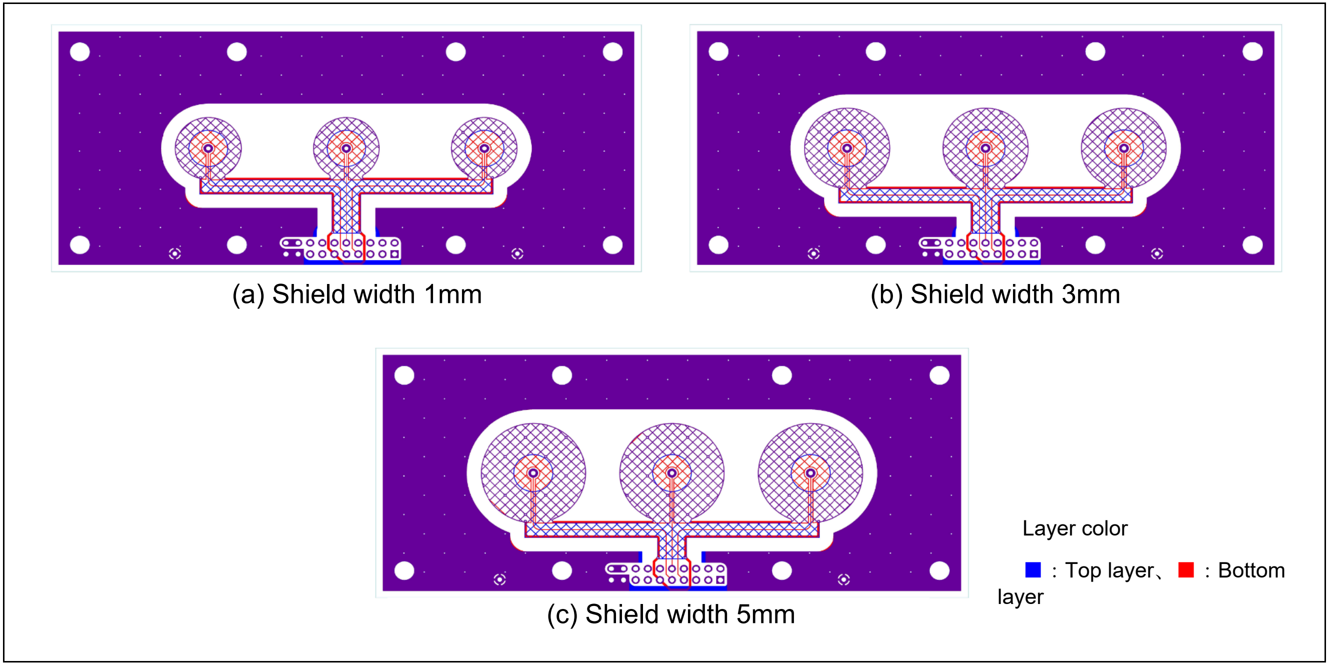


Figure 6-42 Active Shield Evaluation Board Pattern with 17mm Distance Between Buttons

Figure 6-43 shows the SNR characteristics for a 17mm distance between buttons.

- The width of the active shield has little effect on SNR. However, the CTSU sensor drive pulse frequency is often limited by the capacitance of the shield terminals. Increasing the shield width raises capacitance, requiring a lower sensor drive pulse frequency setting. In such cases, SNR may decrease.

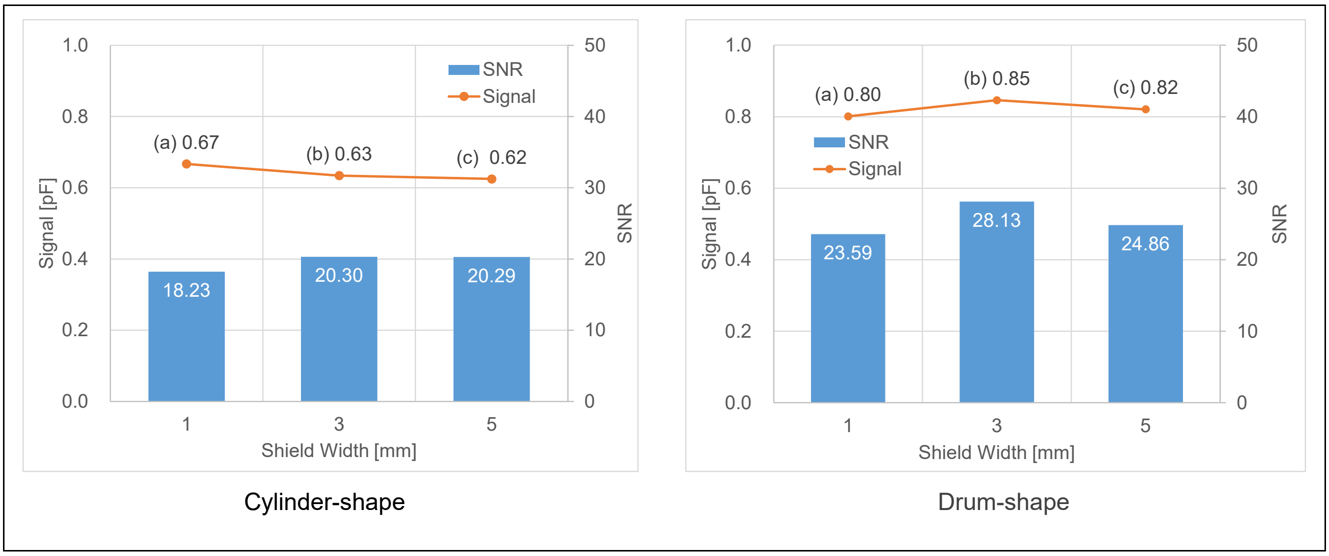


Figure 6-43 SNR Characteristics

Figure 6-44 shows the touch-off parasitic capacitance with a distance between buttons of 17 mm. This parasitic capacitance includes approximately 10.79 pF (Button00) from the CPU board.

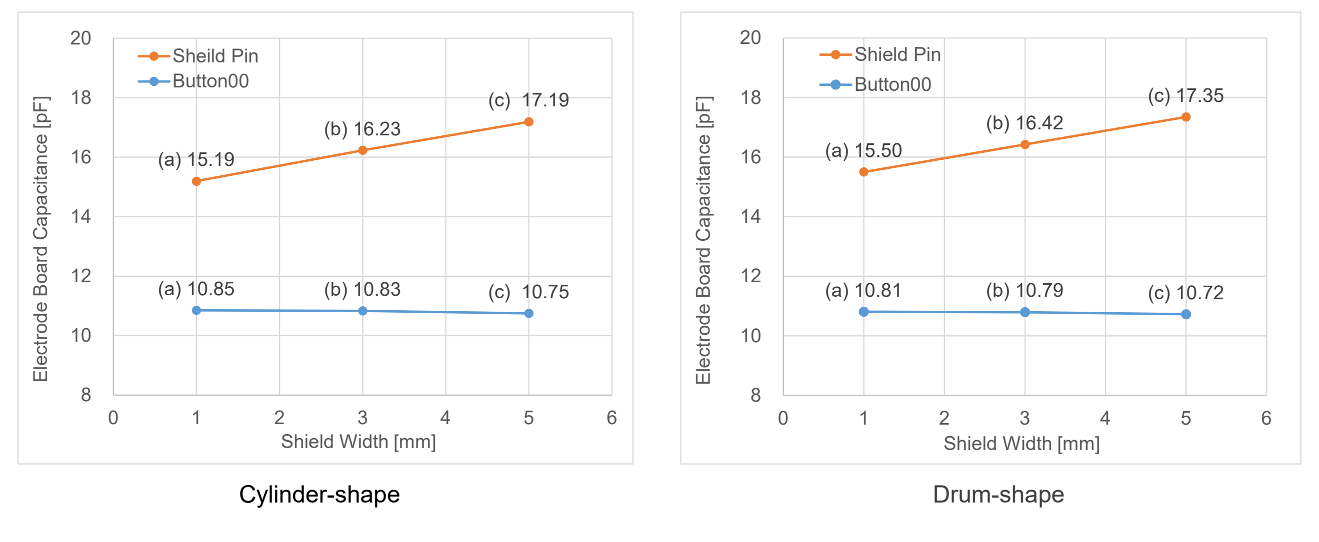


Figure 6-44 Touch-OFF parasitic capacitance

Glossary

Glossary	Description
CTSU	The abbreviation for Capacitive Touch Sensing Unit. Also used a collective term for CTSU1 and CTSU2.
CTSU1	The 2nd generation of the CTSU IP. Used to differentiate from CTSU2.
CTSU2	The collective term used for 3rd generation CTSU IP.
CTSU driver	The CTSU driver software that is included in the Renesas software package.
CTSU module	The unit of CTSU driver software that can be embedded by the Smart Configurator.
TOUCH middleware	The middleware for touch detection processing that uses the CTSU included in the Renesas software package.
TOUCH module	The unit of TOUCH middleware that can be embedded by the Smart Configurator.
r_ctsu module	The name of the CTSU driver displayed in the Smart Configurator,
rm_touch module	The name of the TOUCH module displayed in the Smart Configurator,
CCO	The Current Controlled Oscillator (CCO) used in capacitive touch sensors. Somes documents use the term ICO.
ICO	Same as CCO.
TSCAP	The capacitor which stabilizes the CTSU's internal voltage.
Damping resistor	The resistor used to reduce damage to pins due to external noise and suppress the effects of noise.
VDC	The Voltage Down Converter (VDC); a power supply circuit integrated into the CTSU to provide voltage for capacitive sensor measurements.
Multi-clock measurement	The function for measuring multiple sensor unit clocks with differing frequencies.
Sensor drive pulse	The signal that drives the switched capacitor.
Synchronized noise	Noise with a frequency that matches the sensor drive pulse.
EUT	The abbreviation for Equipment Under Test. It indicates the device is under, or is to be, tested.
LDO	The abbreviation for Low Dropout Regulator.
PSRR	The abbreviation for Power Supply Rejection Ration.
FSP	The abbreviation for Flexible Software Package.
FIT	The abbreviation for Firmware Integration Technology.
SIS	The abbreviation for Software Integration System.

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	Apr.12.21	-	First edition issued
2.0	Sep.30.22	9	Corrections to recommended dimension descriptions and values Figure2-9 (a): dimensions corrected, Figure2-11: added (b)
		16	Figure2-23: added notes to calculation method Added Table 2-4
		24	Figure3-5: corrected Type C electrode dimensions
		34	Added 5. Self-capacitance Method Button Patterns and Characteristics Data
2.1	Apr.28.25	Entire document	Corrected and standardized all CTSU-related terminology Corrected TS pin recommended resistance to 1kΩ (maximum possible setting in QE for Capacitive Touch)
		4	Section 2.1: added description
		5	Table 2 1 and Table2-2: added tables
		6	Figure 2-3: added Button Sensitivity (SNR) Derivation Method, added SNR description Figure 2-5: corrected CTSU measurement image and corrected figure description Moved contents of previous section 5.2 to current section 2.3 ・Changed previous Figure 5-3 to current Figure 2-6 and corrected description ・Changed previous Figure 5-2 to current Figure 2-7 and corrected description
		9	Section 2.4.1: corrected and added to description
		10	Section 2.4.2: added to description
		11	Section 2.4.3: added to description
		13	Figure 2-13: corrected GND shield pattern around wiring vias Figure 2-14: modified GND shield pattern around wiring vias and adjusted space between electrode vias and GND shield
		14	Section 2.5: added to description of shield method, added anti-noise countermeasure reference document Section 2.5.1: changed title Section 2.5.1.1: changed title and added to description Changed previous Figure 2-5 to current Figure 2-16, moved description of GND pattern and parasitic capacitance image from section 2.3 to section 2.5.1.1 Figure 2-17: added list of recommended cross-hatched pattern dimensions
			Section 2.5.1: changed title Section 2.5.1.1: changed title and added to description
		15	Section 2.5.1.2: added to description Added recommended GND shield conditions and layout conditions
		16	Section 2.5.1.3: added to description of active shields and recommended setting information

Rev.	Date	Description	
		Page	Summary
2.1	Apr.28.25	20	Section 2.6: added to description Section 2.6.1: added to description, corrected and changed title of Figure 2.25
		21	Section 2.6.2: added to description
		22	Section 2.7.3: updated description of film-type circuit boards Section 2.7.3.1: added to description of flexible printed circuit (FPC) boards Section 2.7.3.2: added to description of film devices
		24	Section 2.7.3.3: added a design example for film-type circuit boards
		26	Section 2.7.5: added description Section 2.7.6: added self-capacitance matrix Section 2.7.7: added precautions for using RF communication device Section 2.7.8: added design example for metal overlay panel
		28	Section 3.3: added description Section 3.4: subdivided headings for mutual capacitance electrode pattern designs ・Added “Section 3.4.1 Eelectrode Circuit Configuration ・Added “Section 3.4.2: Electrode Pads” (page 29) ・Added “Section 3.4.3: Wiring (page 32) Figure 3-5 (b): added missing dimension notations
		31	Figure 3-7: correction description
		32	Added considerations for mutual capacitance button design
		33	Moved previous section 3.8 to current section 3.4.3
		34	Figure 3-9: moved Tx wiring to bottom layer Figure 3-10: added precautions for Tx/Rx wiring capacitance , and resistance value
		35	Combined contents of previous sections 3.6 and 3.7 to current section 3.5 and changed title of section 3.5.
		36	Section 3.6: added reference document related to anti-noise measurements Section 3.6: changed subheading configuration as follows ・Section 3.6.1: added shield patterns ・Changed previous section 3.9.1 to current section 3.6.1.1. changed title, moved Figures 3-14/3-15 and related descriptions to section 3.6.1.2 ・Changed previous section 3.9.2 to current section 3.6.1.2. changed title, and added to description
		41	Added and updated reference documents
		42	Section 4.2: added Base Clock Frequency/Sensor Drive Pulse Frequency Settings chart
		45	Figure 5-1: corrected SNR formula to match QE for Capacitive Touch formula Table 5-1: updated SNR value
		46	Table 5-3: added method for confirming the multi-clock measurements
		48	Section 5.3: updated SNR value for entire sensitivity characteristics graph with results after applying QE for Capacitive Touch formula
		80	Section 5.3.6.1 title fixed

Rev.	Date	Description	
		Page	Summary
2.2	Jan.30.26	5	Revised Outline of Design Recommendations⑩
		6	Table2.1: Added RL78/L23, RL78/F22, RL78/F25, RA0L1
		10	Added an explanation regarding sensor drive pulse frequency settings when using QE for Capacitive Touch V4.2.0 or later.
		27	Added section 2.7.5.1
		30	Added section 2.8
		46	Added section 3.8
		48	Table4.1: added RL78/L23, RL78/F22, RL78/F25, RA0L1
		51	Added section 4.2.1.2
		54	Added section 4.2.2.2
		56	Chapter 5: evaluation environment and all data were renewed to RA FSP5.9.0+QE for Capacitive Touch 4.1.0
		87	Section 5.3.5.5: revised the PCB specifications and pattern design and updated related data
		101	Added chapter 6.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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