Capacitive Sensor MCU

Capacitive Touch Noise Immunity Guide

Introduction

The Renesas Capacitive Touch Sensor Unit (CTSU) can be susceptible to noise in its surrounding environment because it can detect minute changes in capacitance, generated by unwanted spurious electrical signals (noise). The effect of this noise can depend on the hardware design. Therefore, taking countermeasures at the design stage will lead to a CTSU MCU that is resilient to environmental noise and an effective product development.

This application note describes ways to improve noise immunity for products using the Renesas Capacitive Touch Sensor Unit (CTSU) in accordance with the IEC's noise immunity standards (IEC61000-4).

Target Device

RX Family, RA Family, RL78 Family MCUs and Renesas Synergy™ embedding the CTSU

(CTSU, CTSU2, CTSU2L, CTSU2La, CTSU2SL)

Standards covered in this application note

- IEC-61000-4-3
- IEC-61000-4-6
- IEC-61000-4-4
- IEC-61000-4-2

Contents

1. Overview

The CTSU measures the amount of static electricity from the electric charge when an electrode is touched. If the potential of the touch electrode changes due to noise during measurement, the charging current also changes, affecting the measured value. Specifically, a large fluctuation in the measured value may exceed the touch threshold, causing the device to malfunction. Minor fluctuations in the measured value may affect applications that require linear measurements.

Knowledge about CTSU capacitive touch detection behavior and board design are essential when considering noise immunity for CTSU capacitive touch systems. We recommend first time CTSU users to familiarize yourself with the CTSU and capacitive touch principles by studying the following related documents.

- Basic information regarding capacitive touch detection and CTSU
  Capacitive Touch User's Guide for Capacitive Sensor MCUs (R30AN0424)

- Information regarding hardware board design
  Capacitive Sensor Microcontrollers - CTSU Capacitive Touch Electrode Design Guide (R30AN0389)

- Information regarding CTSU driver (CTSU module) software
  RA Family Renesas Flexible Software Package (FSP) User's Manual (Web Version - HTML)
  API Reference > Modules > CapTouch > CTSU (r_ctsu)
  RL78 Family CTSU Module Software Integration System (R11AN0484)
  RX Family QE CTSU Module Firmware Integration Technology (R01AN4469)

- Information regarding touch middleware (TOUCH module) Software
  RA Family Renesas Flexible Software Package (FSP) User's Manual (Web Version - HTML)
  API Reference > Modules > CapTouch > Touch (rm_touch)
  RL78 Family TOUCH Module Software Integration System (R11AN0485)
  RX Family QE Touch Module Firmware Integration Technology (R01AN4470)

- Information regarding QE for Capacitive Touch (capacitive touch application development support tool)
  Using QE and FSP to Develop Capacitive Touch Applications (R01AN4934)
  Using QE and FIT to Develop Capacitive Touch Applications (R01AN4516)
  RL78 Family Using QE and SIS to Develop Capacitive Touch Applications (R01AN5512)
  RL78 Family Using the Standalone Version of QE to Develop Capacitive Touch Applications (R01AN6574)

2. Noise Types and Countermeasures

2.1 EMC Standards

Table 2-1 provides a list of EMC standards. Noise can influence operations by infiltrating the system through air gaps and connection cables. This list introduces IEC 61000 standards as examples to describe the types of noise developers must be aware to ensure proper operations for systems using the CTSU. Please refer to the latest version of IEC 61000 for further details.

Table 2-1 EMC Testing Standards (IEC 61000)

Test Description	Overview	Standard
Radiated Immunity Test	Test for immunity to relatively high-frequency RF noise	IEC61000-4-3
Conducted Immunity Test	Test for immunity to relatively low-frequency RF noise	IEC61000-4-6
Electrostatic Discharge Test (ESD)	Test for immunity to electrostatic discharge	IEC61000-4-2
Electrical Fast Transient/Burst Test (EFT/B)	Test for immunity to continuous pulsed transient response introduced into power supply lines, etc.	IEC61000-4-4

Table 2-2 lists the performance criterion for immunity testing. Performance criteria are specified for EMC immunity tests, and results are judged based on the operation of the equipment during the test (EUT). Performance criteria are the same for each standard.

Table 2-2 Performance Criteria for Immunity Testing

Performance Criterion	Description
A	The equipment shall continue to operate as intended during and after the test. No degradation of performance or loss of function is allowed below a performance level specified by the manufacturer when the equipment is used as intended.
B	The equipment shall continue to operate as intended during and after the test. No degradation of performance or loss of function is allowed below the performance level specified by the manufacturer when the equipment is used as intended. During the test, degradation of performance is however allowed. No change of actual operating state or stored data is allowed.
C	Temporary loss of function is allowed, provided the function is self-recoverable or can be restored by the operation of the controls.

2.2 RF Noise Countermeasures

RF noise indicates electromagnetic waves of radio frequencies used by television and radio broadcasting, mobile devices, and other electrical equipment. RF noise may directly seep into a PCB or it may enter through the power supply line and other connected cables. Noise countermeasures must be implemented on the board for the former and at the system level for the latter, such as via the power supply line. The CTSU measures capacitance by converting it into an electrical signal. Change in capacitance due to touch is extremely small, so to ensure normal touch detection, the sensor pin and the power supply of the sensor itself must be protected from RF noise.

Two tests with differing test frequencies are available to test for RF noise immunity: IEC 61000-4-3 and IEC 61000-4-6.

IEC61000-4-3 is a radiated immunity test and is used to evaluate noise immunity by directly applying a signal from the radio-frequency electromagnetic field to the EUT. The RF electromagnetic field ranges from 80MHz to 1GHz or higher, which converts to wave lengths of approximately 3.7m to 30cm. As this wavelength and the length of the PCB are similar, the pattern may act as an antenna, adversely affecting the CTSU measurement results. In addition, if the wiring length or parasitic capacitance differs for each touch electrode, the affected frequency may differ for each terminal. Refer to Table 2-3 for details regarding the radiated immunity test.

Table 2-3 Radiated Immunity Test

Frequency Range	Test Level	Test Field Strength
80MHz-1GHz Up to 2.7GHz or up to 6.0GHz, depending on test version	1	1 V/m
	2	3 V/m
	3	10 V/m
	4	30 V/m
	X	Specified individually

IEC 61000-4-6 is a conducted immunity test and is used to evaluate frequencies between 150kHz and 80MHz, a range lower than that of the radiated immunity test. This frequency band has a wavelength of several meters or more, and the wavelength of 150 kHz reaches about 2 km. Because it is difficult to directly apply an RF electromagnetic field of this length on the EUT, a test signal is applied to a cable directly connected to the EUT to evaluate the effect of low-frequency waves. Shorter wavelengths mainly affect power supply and signal cables. For example, if a frequency band causes noise that affects the power cable and the power supply voltage destabilizes, the CTSU measurement results may be affected by noise across all pins. Table 2-4 provides details of the conducted immunity test.

Table 2-4 Conducted Immunity Test

Frequency Range	Test Level	Test Field Strength
150kHz-80MHz	1	1 V rms
	2	3 V rms
	3	10 V rms
	X	Specified individually

In an AC power supply design where the system GND or MCU VSS terminal is not connected to a commercial power supply ground terminal, conducted noise may directly enter the board as common mode noise, which can cause noise in the CTSU measurement results when a button is touched.

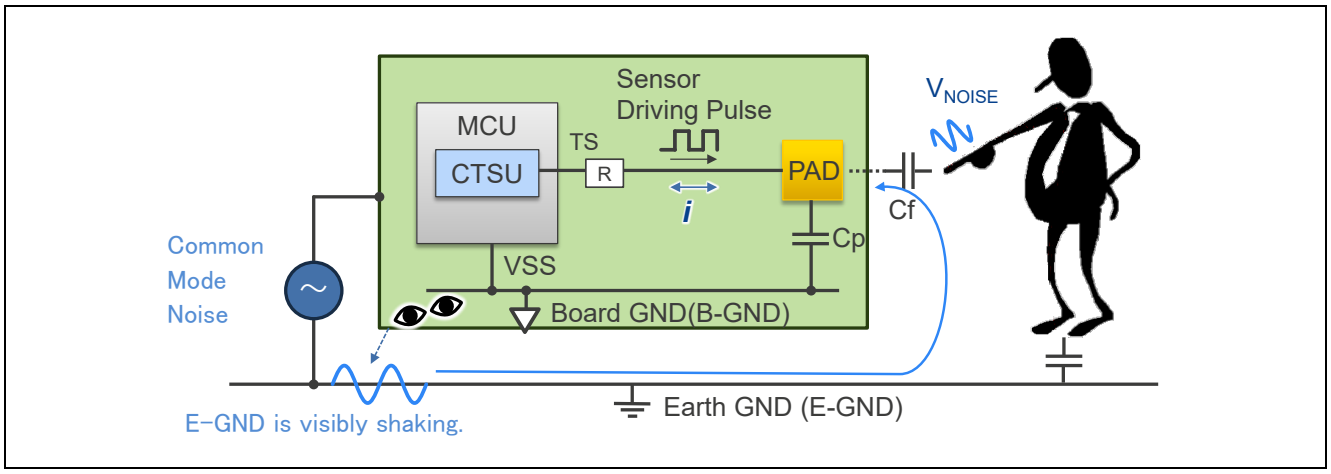


Figure 2-1 Common Mode Noise Entrance Path

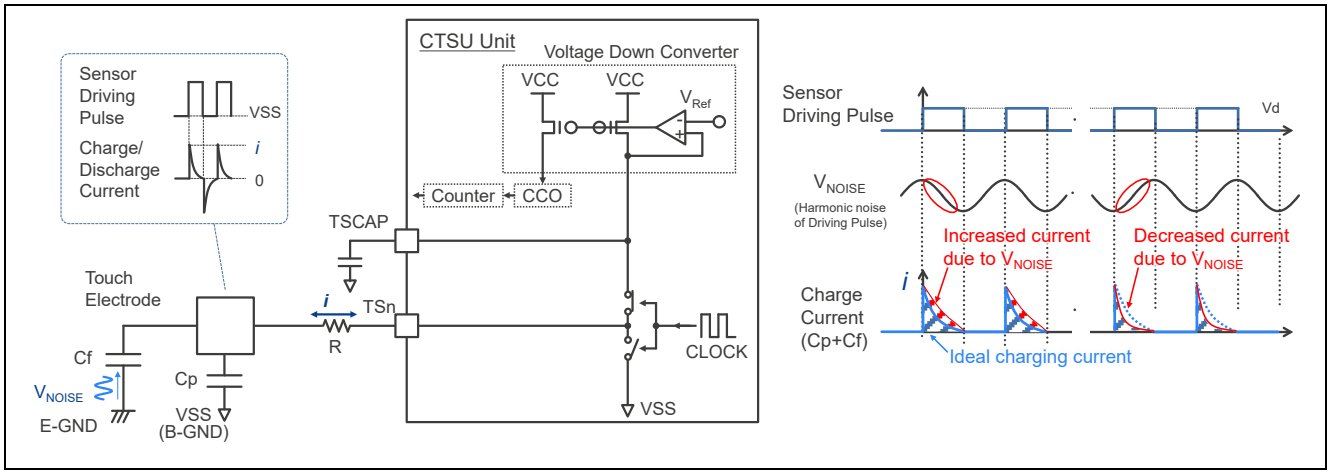


Figure 2-2 Relationship Between Common Mode Noise and Measurement Current

Figure 2-1 shows the Common Mode Noise Entrance Path and Figure 2-2 shows the Relationship Between Common Mode Noise and Measurement Current. From the board GND (B-GND) perspective, common mode noise appears to fluctuate as noise is superimposed on the earth GND (E-GND). In addition, because the finger (human body) that touches the touch electrode (PAD) is coupled to E-GND due to stray capacitance, common mode noise is transmitted and appears to fluctuate in the same way as E-GND.

If the PAD is touched at this point, the noise (V_{NOISE}) generated by common mode noise is applied to the capacitance Cf formed by the finger and the PAD, causing the charging current measured by the CTSU to fluctuate. Changes in the charging current appear as digital values with superimposed noise. If the common mode noise includes frequency components that match the drive pulse frequency of the CTSU and its harmonics, the measurement results may fluctuate significantly.

Table 2-5 provides a list of countermeasures required for improving RF noise immunity. Most countermeasures are common to the improvement of both radiated immunity and conducted immunity. Please refer to the section of each corresponding chapter as listed for each development step.

Table 2-5 List of Countermeasures Required for RF Noise Immunity Improvements

Development Step	Countermeasures Required at Time of Design	Corresponding Sections
MCU selection (CTSU function selection)	Using an MCU embedded with CTSU2 is recommended when noise immunity is priority. • Enable CTSU2 anti-noise countermeasure functions: — Multi-frequency measurement — Active shield — Set to non-measurement channel output when using active shield Or • Enable CTSU anti-noise countermeasure functions: — Random phase shift function — High frequency noise reduction function	 3.3.1 Multi-frequency Measurement 3.3.2 Active Shield 3.3.3 Non-measurement Channel Output Selection 3.2.1 Random Phase Shift Function 3.2.2 High-frequency Noise Reduction Function (spread spectrum function)
Hardware design	• Board design using recommended electrode pattern • Use power supply source for low-noise output • GND pattern design recommendation: in a grounded system use parts for a common mode noise countermeasure • Reduce noise infiltration level at the sensor pin by adjusting the damping resistor value. • Place damping resistor on communication line • Design and place appropriate capacitator on MCU power supply line	4.1.1 Touch Electrode Pattern Designs 4.1.2.1 Voltage Supply Design 4.1.2.2 GND Pattern Design 4.3.1 Common Mode Filter 4.3.4 Considerations for GND Shield and Electrode Distance 4.2.1 TS Pin Damping Resistance 4.2.2 Digital Signal Noise 4.3.4 Considerations for GND Shield and Electrode Distance
Software implementation	Adjust the software filter to reduce the effect of noise on measured values • IIR moving average (effective for most random noise cases) • FIR moving average (for specified periodic noise)	 5.1 IIR Filter 5.2 FIR Filter

2.3 ESD Noise (electrostatic discharge)

Electrostatic discharge (ESD) is generated when two charged objects are in contact or located in proximity. Static electricity accumulated within the human body can reach electrodes on a device even through an overlay. Depending on the amount of electrostatic energy applied to the electrode, the CTSU measurement results may be affected, causing damage to the device itself. Therefore, countermeasures must be introduced at the system level, such as protection devices on the board circuit, board overlays, and protective housing for the device.

The IEC 61000-4-2 standard is used to test ESD immunity. Table 2-6 provides ESD test details. The target application and properties of the product will determine the required test level. For further details, refer to the IEC 61000-4-2 standard. When ESD reaches the touch electrode, it instantaneously generates a potential difference of several kV. This may cause pulse noise to occur in the CTSU measured value, reducing measurement accuracy, or may stop the measurement due to detection of overvoltage or overcurrent. Note that semiconductor devices are not designed to withstand direct application of ESD. Therefore, the ESD test should be conducted on the finished product with the board protected by the device case. Countermeasures introduced on the board itself are failsafe measures to protect the circuit in the rare case that ESD does, for some reason, enter the board.

Table 2-6 ESD Test

Test Level	Test Voltage	
	Contact Discharge	Air Discharge
1	2 kV	2 kV
2	4 kV	4 kV
3	6 kV	8 kV
4	8 kV	15 kV
X	Specified individually	Specified individually

Table 2-7 lists countermeasures required for improving ESD noise immunity. For details regarding each item, refer to the section listed in the table.

Table 2-7 List of Countermeasures Required for Improving ESD Noise Immunity

Development Step	Countermeasure Required at Design Stage	Corresponding Section
Hardware design	• Board design based on recommended electrode patterns • Considerations for GND pattern design • Addition of electrostatic breakdown protection circuit to TS terminal	4.1.1 Touch Electrode Pattern Designs 4.5.1.2 GND Pattern Design 4.5.2 TS Pin Protection Circuit
Software implementation	Reduce noise affecting measurement values with software adjustments • Median filter	5.4 Median Filter

2.4 EFT Noise (Electrical Fast Transients)

Electrical products generate a phenomenon called Electrical Fast Transients (EFT), such as a back electromotive force when the power is switched on due to the internal configuration of the power supply or chattering noise on relay switches. In environments where multiple electrical products are connected in some way, such as on power strips, this noise may travel through power supply lines and affect the operation of other equipment. Even power lines and signal lines of electrical products that are not plugged into a shared power strip may be affected via the air simply by being near power lines or signal lines of the noise source.

The IEC 61000-4-4 standard is used to test EFT immunity. IEC 61000-4-4 evaluates immunity by injecting periodic EFT signals into the EUT power and signal lines. EFT noise generates a periodic pulse in the CTSU measurement results, which may lower the accuracy of the results or cause false touch detection. Table 2-8 provides EFT/B (Electrical Fast Transient Burst) test details.

Table 2-8 EFT/B Test

Test Level	**Open Circuit Test Voltage (peak)**		Pulse repetition frequency (PRF)
	Power Supply Line/Ground Wire	**Signal/Control Line**	
1	0.5 kV	0.25 kV	5kHz or 100kHz
2	1 kV	0.5 kV	
3	2 kV	1 kV	
4	4 kV	2 kV	
X	Specified individually		Specified individually

Table 2-9 shows the list of measures required to improve EFT noise immunity. For details on each item, refer to the links provided in the table.

Table 2-9 List of Countermeasures Required for EFT Noise Immunity Improvements

Development Step	**Countermeasures Required at Time of Design Period**	**Corresponding Sections**
MCU selection (CTSU function selection)	Using an MCU embedded with CTSU2 is recommended when noise immunity is priority. • Enable CTSU2 anti-noise countermeasure function: — Multi-frequency measurement	3.3.1 Multi-frequency Measurement
Hardware design	• Board design using recommended electrode pattern • Use power supply source for low-noise output • Apply countermeasures when designing GND pattern design • Use parts for common mode noise countermeasure to reduce EFT noise infiltration from the AC line in common mode. • Use appropriate capacitor design and placement for MCU power lines • Place TVS diodes on supply and TS pins	4.1.1 Touch Electrode Pattern Designs 4.1.2.1 Voltage Supply Design 4.1.2.2 GND Pattern Design 4.3.1 Common Mode Filter 4.3.2 Capacitor Layout 4.4.3 TVS Diode
Software implementation	Adjust the software filter to reduce the effect of noise on measured value • Median filter	5.4 Median Filter

3. CTSU Noise Countermeasure Functions

CTSUs are equipped with noise countermeasure functions, but the availability of each function differs depending on the version of the MCU and CTSU you are using. Always confirm the MCU and CTSU versions before developing a new product. This chapter explains the differences in noise countermeasure functions between each CTSU version.

3.1 Measurement Principles and Effect of Noise

The CTSU repeats charging and discharging multiple times for each measurement cycle. The measurement results for each charge or discharge current are accumulated and the final measurement result is stored in the register. In this method, the number of measurements per unit time can be increased by increasing the drive pulse frequency, thus improving the dynamic range (DR) and realizing highly sensitive CTSU measurements. On the other hand, external noise causes changes in the charge or discharge current. In an environment where periodic noise is generated, the measurement result stored in the Sensor Counter Register is offset due to an increase or decrease in the amount of current in one direction. Such noise-related effects ultimately decrease measurement accuracy.

Figure 3-1 shows an image of charge current error due to periodic noise. The frequencies that pose as periodic noise are those that match the sensor drive pulse frequency and its harmonic noise. Measurement errors are greater when the rising or falling edge of the periodic noise is synchronized with the SW1 ON period. The CTSU is equipped with hardware-level noise countermeasure functions as protection against this periodic noise.

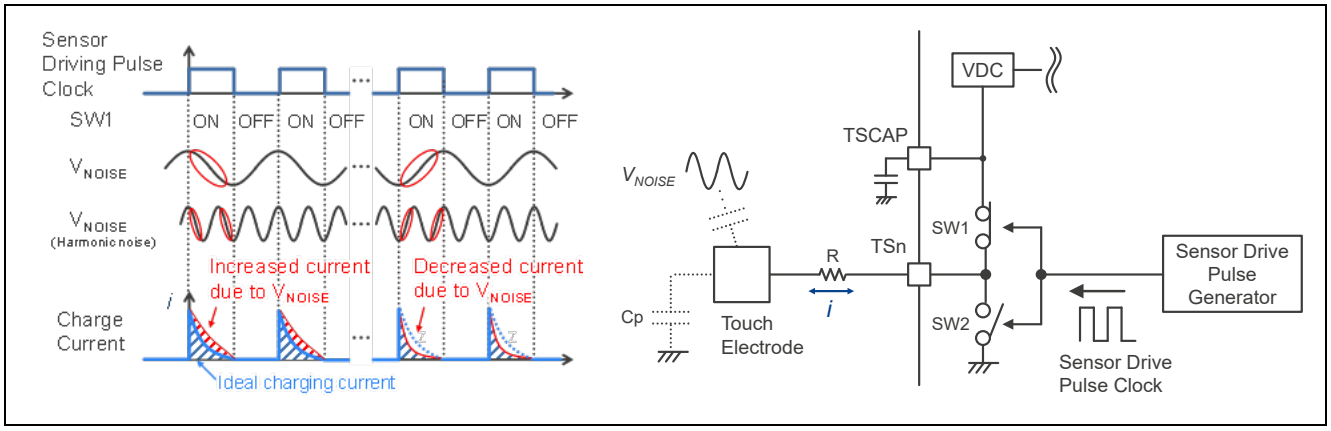


Figure 3-1 Example of Charge Current Error Due to Periodic Noise

3.2 CTSU1

CTSU1 is equipped with a random phase shift function and a high-frequency noise reduction function (spread spectrum function). The effect on the measured value can be reduced when the fundamental harmonics of the sensor drive pulse frequency and the noise frequency match. The maximum setting value of the sensor drive pulse frequency is 4.0MHz.

3.2.1 Random Phase Shift Function

Figure 3-2 shows an image of noise desynchronization using the random phase shift function. By changing the phase of the sensor drive pulse by 180 degrees at random timing, the unidirectional increase/decrease in current due to periodic noise can be randomized and smoothed to improve measurement accuracy.

This function is always enabled in the CTSU module and TOUCH module.

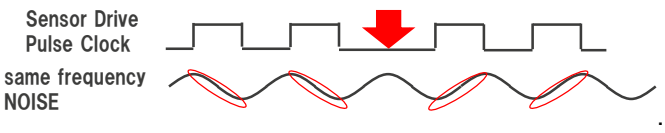


Figure 3-2 Periodic Noise Desynchronization by Random Phase Shift Function (image)

3.2.2 High-frequency Noise Reduction Function (spread spectrum function)

The high-frequency noise reduction function measures at the sensor drive pulse frequency with intentionally added chattering. It then randomizes the synchronization point with the synchronous noise to disperse the peak of the measurement error and improve measurement accuracy.

This function is always enabled in the CTSU module output and TOUCH module output by code generation.

3.3 CTSU2

3.3.1 Multi-frequency Measurement

Multi-frequency measurement uses multiple sensor drive pulse frequencies with differing frequencies. Spread spectrum is not used to avoid interference at each drive pulse frequency.

This function improves immunity against conducted and radiated RF noise because it is effective against synchronous noise on the sensor drive pulse frequency, as well as noise introduced through the touch electrode pattern.

Figure 3-3 shows an image of how measured values are selected in multi-frequency measurement, and Figure 3-4 shows an image of separating noise frequencies in the same measurement method. Multi-frequency measurement discards the measurement results affected by noise from the group of measurements taken at multiple frequencies to improve measurement accuracy.

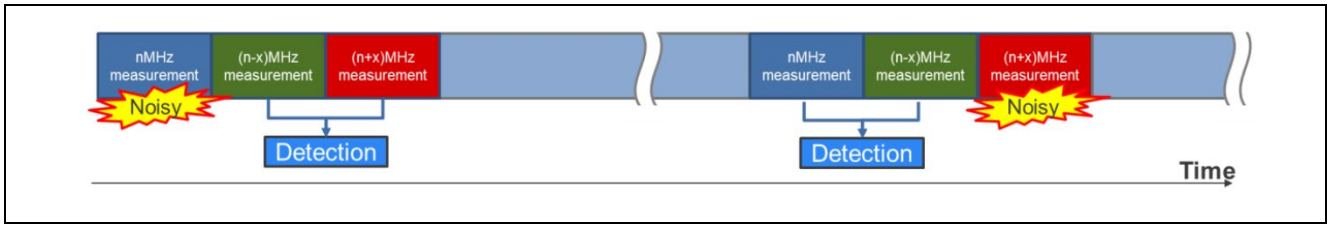


Figure 3-3 Measured Value Selection in Multi-Frequency Measurement (image)

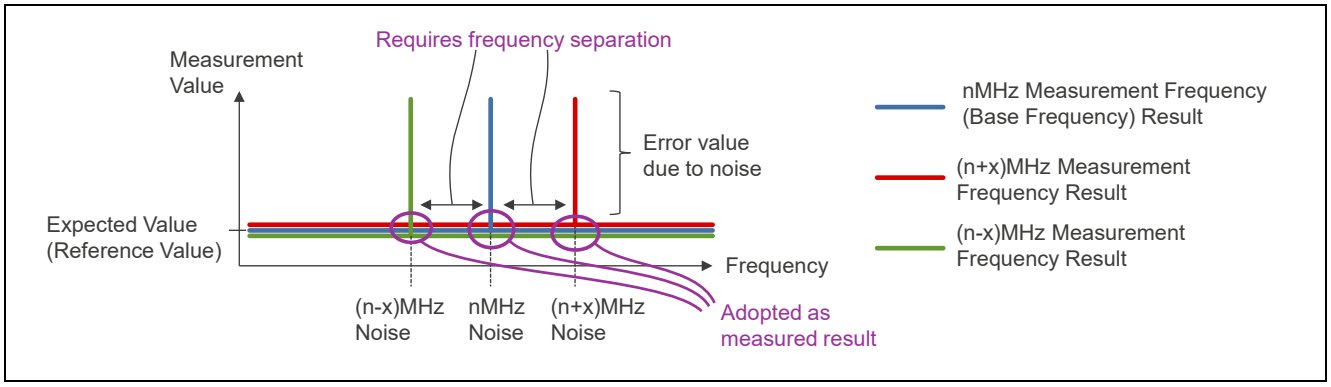


Figure 3-4 Noise Frequency Separation in Multi-Frequency Measurement (image)

In application projects that incorporate CTSU driver and TOUCH middleware modules (refer to the FSP, FIT or SIS documentation), when “QE for Capacitive Touch” tuning phase is executed the parameters of multi-frequency measurement are automatically generated and multi-frequency measurement can be used.

By enabling advanced settings in the tuning phase, the parameters can then be set manually. For details regarding advanced mode multi-clock measurement settings, refer to Capacitive Touch Advanced Mode Parameter Guide (R30AN0428EJ0100).

Figure 3-5 shows an Example of Interference Frequency on Multi-frequency Measurement. This example shows the interference frequency that appears when the measurement frequency is set to 1MHz and common mode conduction noise is applied to the board while the touch electrode is touched. Graph (a) shows the setting immediately after auto-tuning; the measurement frequency is set to +12.5% for the 2nd frequency and -12.5% for the 3rd frequency based on the 1st frequency of 1MHz. The graph confirms that each measurement frequency interferes as noise. Graph (b) shows an example in which the measurement frequency is manually tuned; measurement frequency is set to -20.3% for the 2nd frequency and +9.4% for the 3rd frequency based on the 1st frequency of 1MHz.

If a specific frequency noise appears in the measurement results and the noise frequency matches the measurement frequency, make sure you adjust the multi-frequency measurement while evaluating in the actual environment to avoid interference between the noise frequency and the measurement frequency.

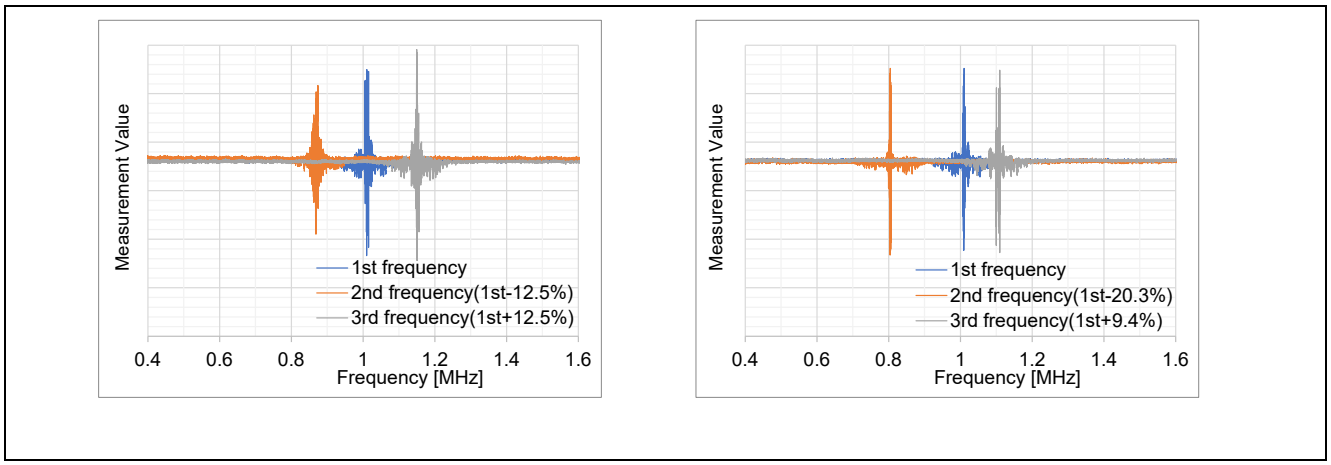


Figure 3-5 Example of Interference Frequency on Multi-frequency Measurements

3.3.2 Active Shield

In the CTSU2 self-capacitance method, an active shield can be used to drive the shield pattern in the same pulse phase as the sensor drive pulse. To enable the active shield, in the QE for Capacitive Touch interface configuration, set the pin that connects to the active shield pattern to “shield pin.” Active shield can be set to one pin per Touch interface configuration (method). For an explanation of the operation of Active Shield, refer to the ”Capacitive Touch User’s Guide for Capacitive Sensor MCUs (R30AN0424)”. For PCB design information, refer to the ”CTSU Capacitive Touch Electrode Design Guide (R30AN0389)“

3.3.3 Non-measurement Channel Output Selection

In the CTSU2 self-capacitance method, pulse output in the same phase as the sensor drive pulse can be set as the non-measurement channel output. In the QE for Capacitive Touch interface configuration (method), non-measurement channels (touch electrodes) are automatically set to the same pulse phase output for methods assigned with active shielding.

4. Hardware Noise Countermeasures

4.1 Board Design Countermeasures

4.1.1 Touch Electrode Pattern Designs

The touch electrode circuit is very susceptible to noise, requiring noise immunity to be considered at the hardware design stage. For detailed board design rules that tackle noise immunity, please refer to the latest version of the CTSU Capacitive Touch Electrode Design Guide (R30AN0389). Figure 4-1 provides an excerpt from the Guide showing an overview of self-capacitance method pattern design, and Figure 4-2 shows the same for mutual-capacitance method pattern design.

① Electrode shape: square or circle
② Electrode size: 10mm to 15mm
③ Electrode proximity: Electrodes should be placed with ample distance so that they do not react simultaneously to the target human interface, (referred to as “finger” in this document); suggested interval: button size x 0.8 or more
④ Wire width: approx. 0.15mm to 0.20mm for printed board
⑤ Wiring length: Make the wiring as short as possible. On corners, form a 45-degree angle, not a right angle.
⑥ Wiring spacing:
(A) Make spacing as wide as possible to prevent false detection by neighboring electrodes.
(B) 1.27mm pitch
⑦ Cross-hatched GND pattern width: 5mm
⑧ Cross-hatched GND pattern and button/wiring spacing
(A) area around electrodes: 5mm (B) area around wiring: 3mm or more
Cover the electrode area as well as the wiring and opposite surface with a cross-hatched pattern. Also place a cross-hatched pattern in the empty spaces, and connect the 2 surfaces of cross-hatched patterns through vias.
Refer to section “2.5 Anti-Noise Layout Pattern Designs” for cross-hatched pattern dimensions, active shield (CTSU2 only), and other anti-noise countermeasures.
⑨ Electrode + wiring capacitance: 50pF or less
⑩ Electrode + wiring resistance: 2kΩ or less (including damping resistor with reference value of 560Ω)

Figure 4-1 Pattern Design Recommendations for Self-capacitance Method (excerpt)

① Electrode shape: square (combined transmitter electrode TX and receiver electrode RX)
② Electrode size: 10mm or larger
③ Electrode proximity: Electrodes should be placed with ample distance so that they do not react simultaneously to the touch object (finger, etc.), (suggested interval: button size x 0.8 or more)
④ Wire width: The thinnest wire capable through mass production; approx. 0.15mm to 0.20mm for a printed board
⑤ Wiring length: Make the wiring as short as possible. On corners, form a 45-degree angle, not a right angle.
⑥ Wiring spacing:
(A) Make spacing as wide as possible to prevent false detection by neighboring electrodes.
(B) When electrodes are separated: 1.27mm pitch
(C) 20mm or more to prevent coupling capacitance generation between Tx and Rx.
⑦ Cross-hatched GND pattern (shield guard) proximity
Because the pin parasitic capacitance in the recommended button pattern is comparatively small, parasitic capacitance increases the closer the pins are to GND.
A: 4mm or more around electrodes
We also recommend approx. 2-mm wide cross-hatched GND plane pattern between electrodes.
B: 1.27mm or more around wiring
⑧ Tx, Rx parasitic capacitance: 20pF or less
⑨ Electrode + wiring resistance: 2kΩ or less (including damping resistor with reference value of 560Ω)
⑩ Do not place GND pattern directly under the electrodes or wiring.
The active shield function cannot be used for the mutual-capacitance method.

Figure 4-2 Pattern Design Recommendations for Mutual Capacitance Method (excerpt)

4.1.2 Power Supply Design

The CTSU is an analog peripheral module that handles minute electrical signals. When noise infiltrates the voltage supplied to the MCU or GND pattern, it causes potential fluctuation on the sensor drive pulse and decreases measurement accuracy. We strongly suggest adding a noise countermeasure device to the power supply line or onboard power supply circuit to safely supply power to the MCU.

4.1.2.1 Voltage Supply Design

Action should be taken when designing the power supply for the system or onboard device to prevent noise infiltration via the MCU power supply pin. The following design-related recommendations can help prevent noise infiltration.

- Keep the power supply cable to the system and internal wiring as short as possible to minimize impedance.
- Place and insert a noise filter (ferrite core, ferrite bead, etc.) to block high frequency noise.
- Minimize the ripple on the MCU power supply. We recommend using a linear regulator on the MCU's voltage supply. Select a linear regulator with low-noise output and high PSRR characteristics.
- When there are several devices with high current loads on the board, we recommend inserting a separate power supply for the MCU. If this is not possible, separate the pattern at the root of the power supply.
- When running a device with high current consumption on the MCU pin, use a transistor or FET.

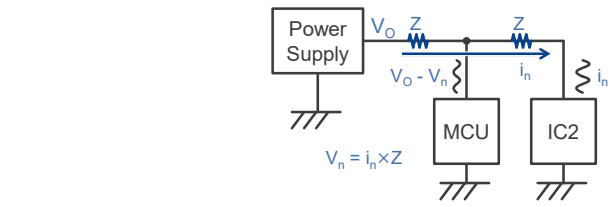
Figure 4-3 shows several layouts for the power supply line. IC2 indicates the devices on the board. V_o is the power supply voltage, i_n is the consumption current fluctuation resulting from IC2 operations, and Z is the power supply line impedance. V_n is the voltage generated by the power supply line and can be calculated as $V_n = i_n \times Z$. The GND pattern can be considered in the same way. For more details on the GND pattern, refer to 4.1.2.2 GND Pattern Design.

In configuration (a), the power supply line to the MCU is long and the IC2 supply lines branch near the MCU's power supply. This configuration is not recommended as the MCU's voltage supply is susceptible to V_n noise when the IC2 is in operation.

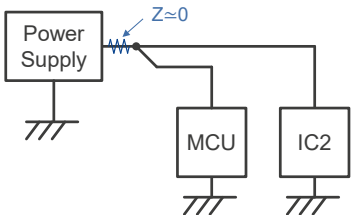
(b) and (c) circuit diagrams of (b) and (c) are the same as (a), but the pattern designs differ.

(b) branches the power supply line from the root of the power supply, and the effect of V_n noise is reduced by minimizing Z between the power supply and the MCU.

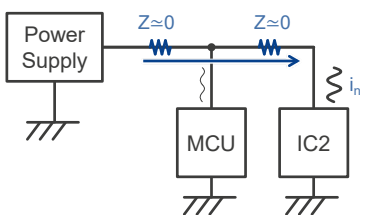
(c) also reduces the effect of V_n by increasing the surface area and line width of the power supply line to minimize Z.



(a) Undesirable power supply layout



(b) Ideal power supply layout (1)



(c) Ideal power supply layout (2)

Note: See 4.1.2.2 for details on GND pattern design.

Figure 4-3 Power Supply Line Layouts

4.1.2.2 GND Pattern Design

Depending on the pattern design, noise may cause the GND, which is the reference voltage for the MCU and on-board devices, to fluctuate in potential, decreasing CTSU measurement accuracy. The following hints for GND pattern design will help suppress potential fluctuation.

- Cover empty spaces with a solid GND pattern as much as possible to minimize impedance over a large surface area.
- Use a board layout that prevents noise from infiltrating the MCU via the GND line by increasing the distance between the MCU and devices with high current loads and separating the MCU from the GND pattern.

Figure 4-4 shows several layouts for the GND line. In this case, i_n is the consumption current fluctuation resulting from IC2 operations, and Z is the power supply line impedance. V_n is the voltage generated by the GND line and can be calculated as $V_n = i_n \times Z$.

In configuration (a), the GND line to the MCU is long and merges with the IC2 GND line near the MCU's GND pin. This configuration is not recommended as the MCU's GND potential is susceptible to V_n noise when the IC2 is in operation.

In configuration (b) the GND lines merge at the root of the power supply GND pin. Noise effects from Vn can be reduced by separating the GND lines of the MCU and the IC2 to minimize the space between the MCU and Z.

Although the circuit diagrams of (c) and (a) are the same, the pattern designs differ. Configuration (c) reduces the effect of V_n by increasing the surface area and line width of the GND line to minimize Z.

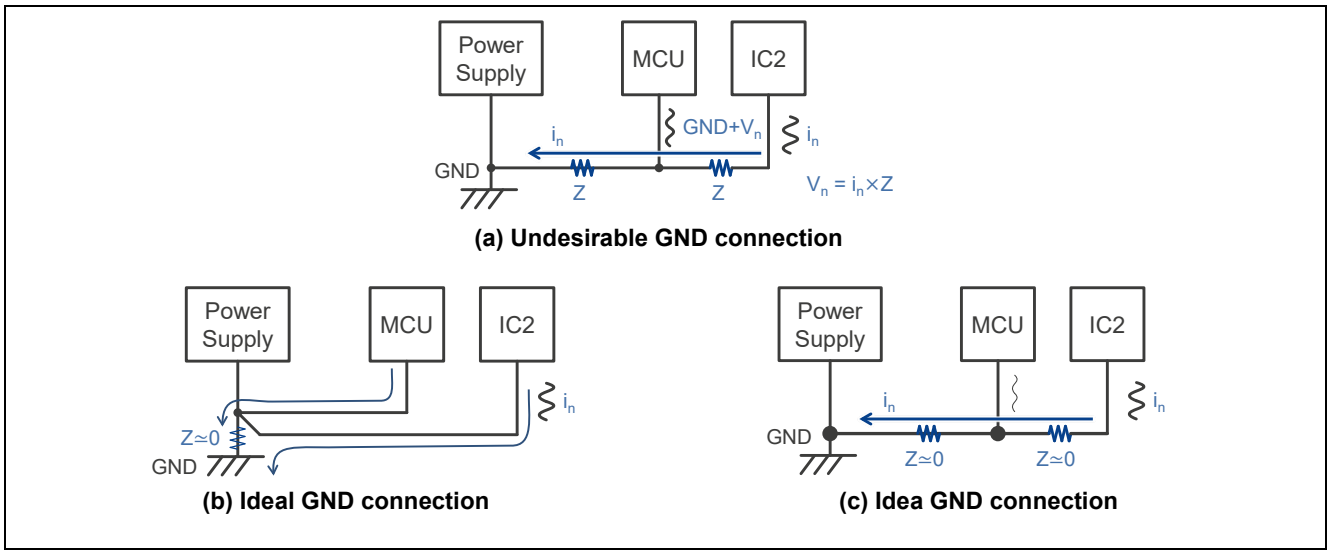


Figure 4-4 GND Line Layout

- Connect the TSCAP capacitor's GND to the GND solid pattern that is connected to the MCU's VSS terminal so that it has the same potential as the VSS terminal. Do not separate the TSCAP capacitor's GND from the MCU's GND. If the impedance between the TSCAP capacitor's GND and the MCU's GND is high, the high frequency noise rejection performance of the TSCAP capacitor will decrease, making it more susceptible to power supply noise and external noise.

4.1.3 Processing Unused Pins

Leaving unused pins in a high impedance state makes the device susceptible to the effects of external noise. Make sure you process all unused pins after referring to the corresponding MCU Faily hardware manual of each pin. If a pulldown resistor cannot be implemented due to lack of mounting area, fix the pin output setting to low output.

4.2 Radiated RF Noise Countermeasures

4.2.1 TS Pin Damping Resistance

The damping resistor connected to the TS pin and the electrode's parasitic capacitance component function as a low pass filter. Increasing the damping resistor lowers the cut off frequency, thus lowering the level of radiated noise infiltrating the TS pin. However, when the capacitive measurement charge or discharge current period is lengthened, the sensor drive pulse frequency must be lowered, which also lowers the touch detection accuracy. For information regarding sensitivity when changing the damping resistor in the self-capacitance method, refer to "5. Self-capacitance Method Button Patterns and Characteristics Data" in the CTSU Capacitive Touch Electrode Design Guide (R30AN0389)

4.2.2 Digital Signal Noise

Digital signal wiring that handles communication, such as SPI and I2C, and PWM signals for LED and audio output is a source of radiated noise that affects the touch electrode circuit. When using digital signals, take the following suggestions into consideration during the design stage.

- When the wiring includes right-angle corners (90 degrees), noise radiation from the sharpest points will increase. Make sure the wiring corners are 45 degrees or less, or curved, to reduce noise radiation.
- When the digital signal level changes, the overshoot or undershoot is radiated as high-frequency noise. As a countermeasure, insert a damping resistor on the digital signal line to suppress the overshoot or undershoot. Another method is to insert a ferrite bead along the line.
- Layout the lines for digital signals and the touch electrode circuit so that they do not touch. If the configuration requires the lines to run in parallel, keep as much distance between them as possible and insert a GND shield along the digital line.
- When running a device with high current consumption on the MCU pin, use a transistor or FET.

4.2.3 Multi-frequency Measurement

When using an MCU embedded with CTSU2, make sure to use multi-frequency measurement. For details, see "3.3.1 Multi-frequency Measurement".

4.3 Conducted Noise Countermeasures

The design of the system's power supply unit is critical for achieving conducted noise immunity. Conducted noise infiltrates the system through the AC power line. Therefore, noise must be reduced via the power supply unit to prevent it from entering the MCU and peripheral circuits. The first requirement is to design a power supply unit that can supply a voltage with low noise. This chapter describes hardware noise countermeasures and CTSU functions that should be considered when designing an MCU board to improve conducted noise immunity.

4.3.1 Common Mode Filter

Place or mount a common mode filter (common mode choke, ferrite core) to reduce noise entering the board from the power cable. Inspect the system's interference frequency with a noise test and select a device with high impedance to reduce the targeted noise band. Refer to the respective items as the installation position differs depending on the type of filter. Note that each type of filter is placed differently on the board; refer to the corresponding explanation for details. Always consider the filter layout to avoid radiating noise within the board.

- Common Mode Choke

The common mode choke is used as a noise countermeasure implemented on the board, requiring it to be embedded during the board and system design phase. When using a common mode choke, make sure to use the shortest wiring possible immediately after the point where power supply is connected to the board. For example, when connecting the power cable and board with a connector, placing a filter immediately after the connector on the board side will prevent the noise entering via the cable from spreading across the board.

- Ferrite Core

The ferrite core is used to reduce noise conducted via the cable. When noise becomes an issue after system assembly, introducing a clamp-type ferrite core allows you to reduce noise without changing the board or system design. For example, when connecting the cable and board with a connector, placing a filter just before the connector on the board side will minimize the noise entering the board.

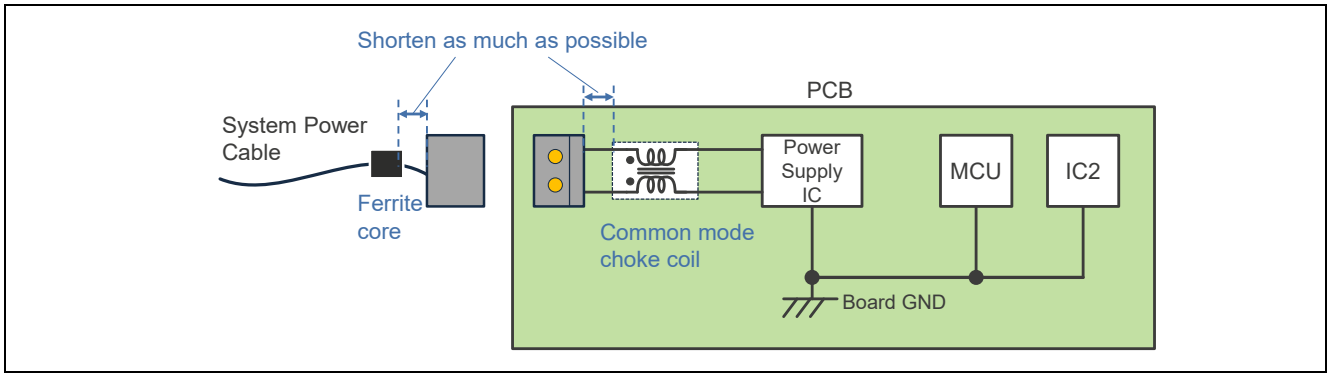


Figure 4-5 Common Mode Filter Layout Example

4.3.2 Capacitor Layout

Reduce power supply noise and ripple noise that enters the board from the power supply and signal cables by designing and placing decoupling capacitors and bulk capacitors near the MCU power line or terminals.

- Decoupling capacitor

A decoupling capacitor can reduce the voltage drop between the VCC or V_{DD} power supply pin and VSS due to the MCU's current consumption, stabilizing CTSU measurements. Use the recommended capacitance listed in the MCU User's Manual, placing the capacitor near the power supply pin and VSS pin. Another option is to design the pattern by following the hardware design guide for the target MCU family, if available.

- Bulk Capacitor

Bulk capacitors will smooth ripples in the MCU's voltage supply source, stabilizing the voltage between the MCU's power pin and VSS, and thus stabilizing CTSU measurements. The capacitance of capacitors will vary depending on the power supply design; make sure you use an appropriate value to avoid generating oscillation or voltage drop.

4.3.3 Multi-frequency Measurement

Multi-frequency measurement, a function of CTSU2, is effective in improving conducted noise immunity. If conducted noise immunity is a concern in your development, select an MCU equipped with CTSU2 to make use of the multi-frequency measurement function. For details, refer to 3.3.1 Multi-frequency Measurement.

4.3.4 Considerations for GND Shield and Electrode Distance

Figure 1 shows an image of noise suppression using the conduction noise addition path of the electrode shield. Placing a GND shield around the electrode and bringing the shield surrounding the electrode closer to the electrode strengthens the capacitive coupling between the finger and the shield. The noise component (V_{NOISE}) escapes to B-GND, reducing fluctuations in the CTSU measurement current. Note that the closer the shield is to the electrode, the bigger the Cp, resulting in reduced touch sensitivity. After changing the distance between the shield and the electrode, confirm the sensitivity in section 5. Self-capacitance Method Button Patterns and Characteristics Data of CTSU Capacitive Touch Electrode Design Guide (R30AN0389).

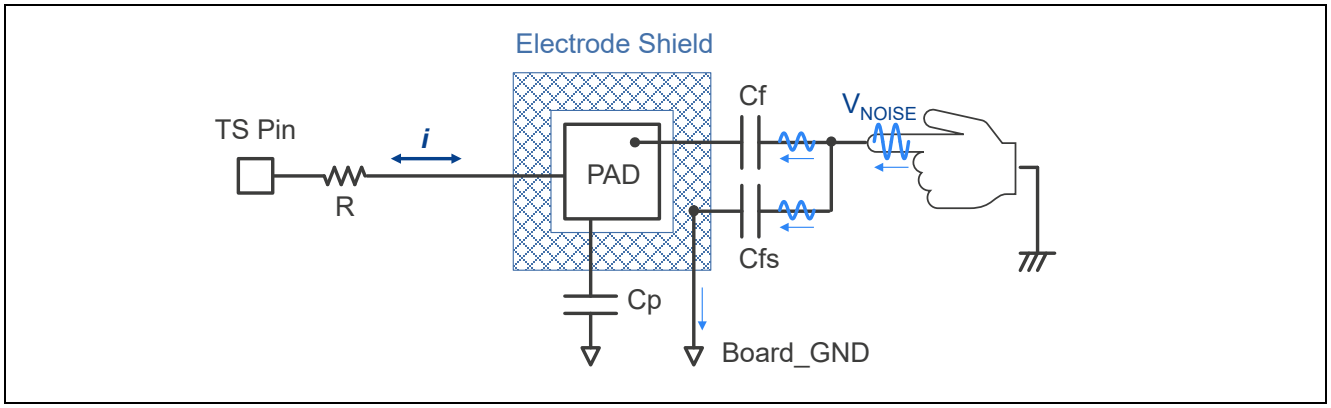


Figure 4-6 Noise Suppression Using Conduction Noise Addition Path of Electrode Shield

4.4 EFT Noise Countermeasures

The design of the system's power supply unit is critical for achieving EFT noise immunity. EFT noise is a continuous pulse noise of several kV that infiltrates the system through the AC power line. Therefore, noise must be reduced via the power supply unit to prevent it from entering the MCU and peripheral circuits. The first requirement is to design a power supply unit that can supply a voltage with low noise. This chapter describes hardware noise countermeasures and CTSU functions that should be considered when designing an MCU board to improve EFT noise immunity.

4.4.1 Power Supply Design

This section describes the effect of filters placed on the board's power supply line. For usage notes regarding power supply patterns for the MCU and peripheral circuits, refer to 4.1.2 Power Supply Design.

4.4.2 Common Mode Filter

Place or mount a common mode filter (common mode choke or ferrite core) to reduce noise infiltration to the board from the power supply cable. The common mode filter will reduce EFT noise that was not eliminated by the power supply unit as well as remove noise that appears in the CTSU measured values. When designing, keep in mind that the insertion location of a filter depends on the filter type, and use a layout that does not spread the noise across the board. For more details on filter layouts, refer to 4.3.1 Common Mode Filter.

4.4.3 TVS Diode

Using a TVS diode reduces the peak voltage of EFT noise superimposed on the power supply and CTSU drive pulse voltage and helps reduce noise that appears in CTSU measured values. Appropriate design and placement of TVS diodes is essential to fully benefit from their effect.

- Board power supply

When using a TVS diode for overvoltage protection, place it immediately after the power input pin. To mount the diode, connect it to the power line and board GND with wiring as short and as thick as possible to minimize impedance. If you are using a common mode filter, place the diode before the filter.

Consider the following recommendations when selecting a TVS diode.

- Electrostatic immunity (or ESD withstand voltage, etc.): equal to or greater than the expected EFT noise voltage
- Maximum reverse operating voltage (V_{RWM}) equal to or higher than the voltage of the power supply line where it is placed: As a guide, use a V_{RWM} approximately 10 to 20% higher than the supply voltage to allow for operating margin.
- Use breakdown voltage (V_{BR}) and clamping voltage (V_{CLAMP}) of only minimal difference with the V_{RWM}.

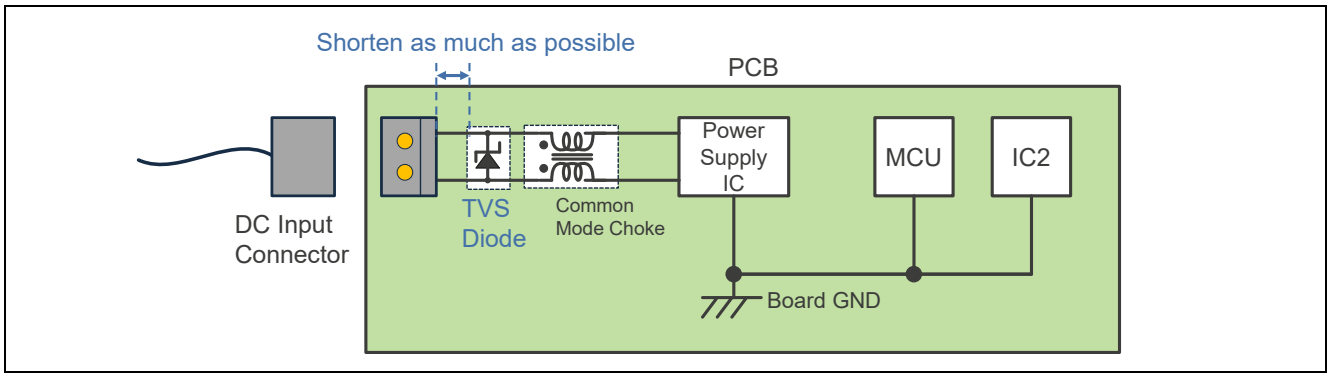


Figure 4-7 Example TVS Diode Layout

- TS pin (touch electrode)

When using a TVS diode, place it close to the touch electrode and connect it between the touch electrode and the board GND with wiring that is as short and as thick as possible to minimize impedance.

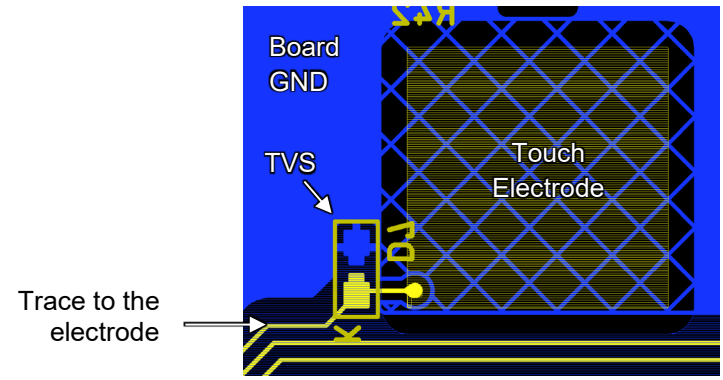


Figure 4-8 Recommended TVS Connection for TS Pin

Consider the following recommendations when selecting a TVS diode to connect to the TS pin.

- Low capacitance, low leakage current: Renesas has evaluated products with maximum values of 0.25 pF and 50 nA at 25°C.
- Electrostatic resistance greater than the expected EFT noise voltage
- Maximum reverse working voltage (V_{RWM}) must be equal to or higher than the MCU operating voltage, and breakdown voltage (V_{BR}) or clamp voltage (V_{CLAMP}) must be equal to or lower than the MCU's absolute rated voltage.
- Minimal difference between V_{BR} or V_{CLAMP} and V_{RWM}
- When selection is limited and the absolute rated voltage will be exceeded, use two unidirectional devices to configure a clamp circuit. In this case, select a product with a V_F (forward voltage) that ensures the sum of the TVS V_F and the MCU supply voltage is equal to or less than the absolute rated voltage.

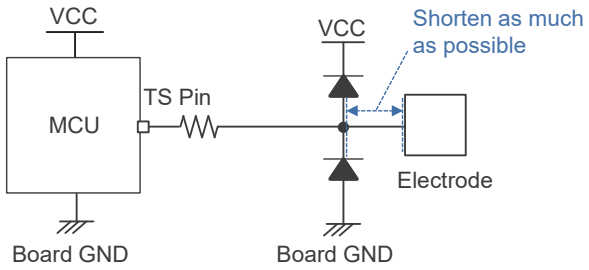


Figure 4-9 Clamp Circuit Configuration Example

The capacitance of the TVS diode is added to the capacitance of the TS pin. When the drive pulse frequency of the RA2L1's built-in CTSU2 is 1 MHz, from the CTSU2 perspective, the leakage current of the TVS diode appears to increase capacitance by approximately 0.67 pF/uA. Note that this increase in capacitance is inversely proportional to the drive pulse frequency. For example, when drive pulse frequency is 0.5 MHz, capacitance is approximately 1.33pF/uA; when 2 MHz, approximately 0.33pF/uA. The CTSU selects the drive pulse frequency in stages, according to the total capacitance connected to the TS pin. The higher the drive pulse frequency, the higher the signal value (the difference between touch ON/OFF) and the better the SNR. If the total capacitance connected to the TS pin is too large, the drive pulse frequency must be reduced, which in turn lowers the SNR. Therefore, when adding an ESD protection device to the TS pin, select a device with low capacitance and low leakage current to avoid lowering the drive pulse frequency. For details regarding parasitic capacitance, damping resistance, and drive pulse frequency, see Capacitive Sensor MCU QE for Capacitive Touch Advanced Mode Parameter Guide. For information regarding the effect on measurement values or device conditions during evaluation when connecting a TVS diode to the TS pin, refer to Capacitive Sensor Microcontrollers CTSU Capacitive Touch Electrode Design Guide, 5.4.6.4 Sensitivity characteristics with ESD Protection Diode Connected.

4.4.4 Multi-frequency Measurement

When using the CTSU2 microcontroller's Multi-frequency measurement, the three different measurement drive pulse frequencies make EFT noise cycle synchronization difficult, effectively reducing synchronous noise. In addition, the multi-frequency measurement discards the measured values affected from the group of measurements taken at multiple frequencies through the majority decision process to improve measurement accuracy. For more details on multi-frequency measurements, refer to 3.3.1 Multi-frequency Measurement.

4.5 ESD Noise Countermeasures

Touch electrode circuitry is susceptible to noise, so noise immunity must be taken into consideration during the hardware design stage. Electrostatic discharge (ESD) can be released to the touch electrode through the overlay covering it. Static electricity can also enter the system through gaps in the housing or through panel joints and can even penetrate the circuit board inside the housing. If the touch electrode is affected by static electricity, pulse noise can appear in the CTSU measurement values, measurement values might be caused to overflow or underflow, and in some cases, the device may be damaged. This chapter describes hardware noise countermeasures and CTSU functions that should be taken into consideration when designing your MCU board to improve ESD noise immunity.

4.5.1 Board Pattern Design

4.5.1.1 Touch Electrode

For details regarding design rules that take board noise into consideration, refer to the latest Capacitive Sensor Microcontrollers CTSU Capacitive Touch Electrode Design Guide.

4.5.1.2 GND Pattern Design

Place a GND pattern of 2mm or more around the board periphery and shield the touch electrode and wiring with the GND pattern. By inducing static electricity to a GND pattern with low and stable potential, you can reduce the direct penetration of static electricity into the touch electrode. In addition, place the touch electrode as far away from the edge of the board as possible.

4.5.2 TS Pin Protection Circuit

We recommend adding an ESD protection device such as a TVS diode to prevent damage to the TS pin. To ensure that the ESD protection device employed in your design operates effectively, follow the usage instructions for the specific device. Introducing additional protection circuitry can affect the CTSU measurement results, so we recommend selecting an ESD protection device that features low capacitance and low leakage current. The recommendations for selecting a TVS diode are listed in the subsection "TS pin (touch electrode)" in 4.4.3 TVS Diode. Since additional protection circuitry can affect the CTSU measurement results, low capacitance, low leakage current devices are recommended.

5. Software Filters

Touch detection uses capacitance measurement results to determine whether a sensor has been touched or not (ON or OFF) using both CTSU driver and TOUCH module software. The CTSU module performs noise reduction on the capacitance measurement results and passes the data to the TOUCH module which determines touch.

The CTSU driver includes the IIR moving average filter as the standard filter. In most cases, the standard filter can provide sufficient SNR and responsiveness. However, more powerful noise reduction processing may be required depending on the user system.

Figure 5-1 shows the Data Flow Through Touch Detection. User filters can be placed between the CTSU driver and TOUCH module for noise processing. Refer to the application note below for detailed instructions on how to incorporate filters into a project file as well as a software filter sample code and usage example project file.

RA Family Capacitive Touch Software Filter Sample Program (R30AN0427)

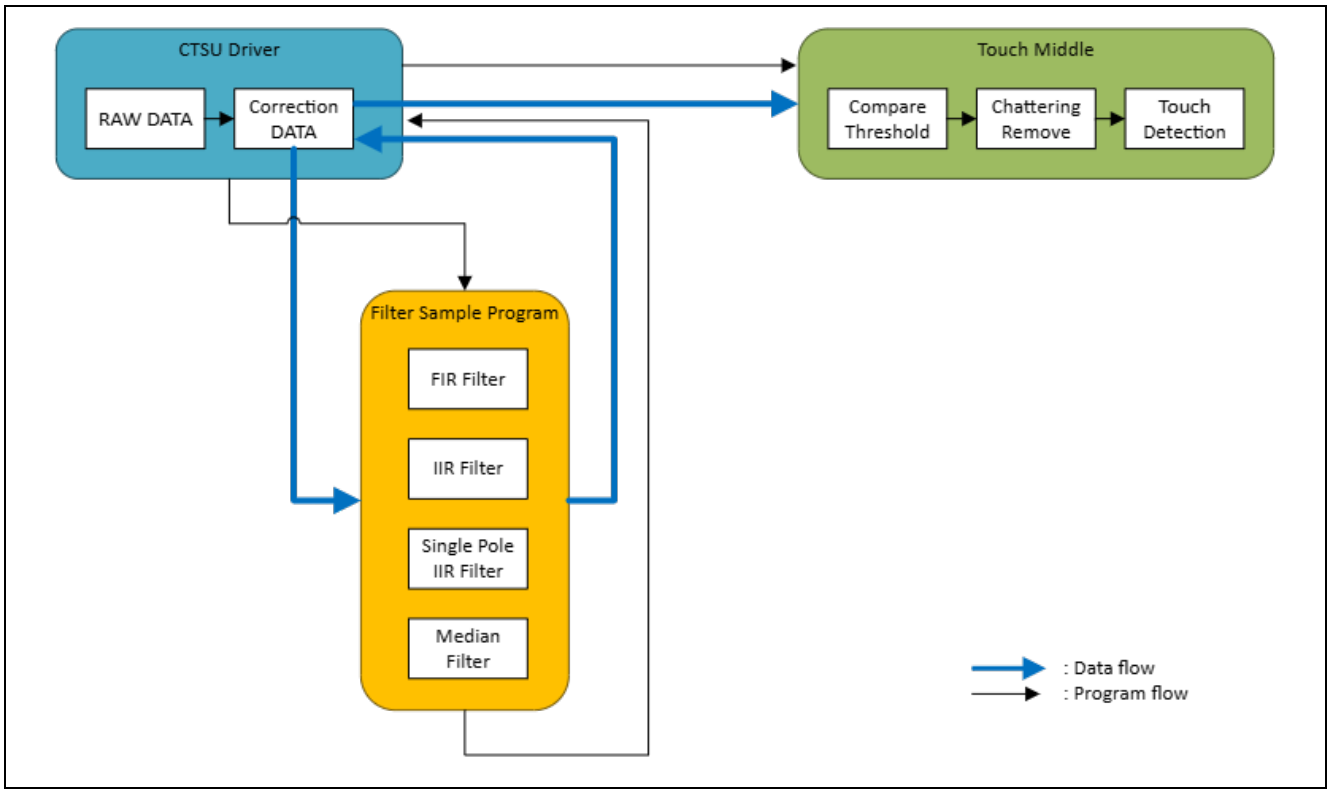


Figure 5-1 Data Flow Through Touch Detection

This section introduces effective filters for each EMC standard.

Table 5-1 EMC Standards and Corresponding Software Filters

EMC Standard	Expected Noise	Corresponding Software Filter
IEC61000-4-3 Radiated immunity, IEC61000-4-6 Conducted immunity	Random noise	IIR filter
	Periodic noise	FIR filter
IEC61000-4-4 EFT/B IEC61000-4-2 ESD	Pulse noise	Median filter

5.1 IIR Filter

The IIR filter (Infinite Impulse Response filter) requires less memory and boasts a small calculation load, making it ideal for low-power systems and applications with many buttons. Using this as a low pass filter helps reduce high frequency noise. However, care must be taken as the lower the cutoff frequency, the longer the settling time, which will delay the ON/OFF judgment process.

The single-pole first-order IIR filter is calculated using the following formula, where a and b are coefficients, x_n is the input value, y_n is the output value, and y_{n-1} is the immediately previous output value.

$$y_n = ax_n + by_{n-1}$$

When the IIR filter is used as a low-pass filter, coefficients a and b can be calculated using the following formula, where the sampling frequency is f_s and the cutoff frequency is f_c.

$$b = e^{-\frac{2\pi f_c}{f_s}}, \qquad a = 1 - b$$

5.2 FIR Filter

The FIR filter (Finite Impulse Response filter) is a highly stable filter that incurs minimal accuracy deterioration due to calculation errors. Depending on the coefficient, it can be used as a low-pass filter or band-pass filter, reducing both periodic noise and random noise, thus improving SNR. However, because samples from a certain previous period are stored and calculated, memory usage and calculation load will increase in proportion to the filter tap length.

The FIR filter is calculated using the following formula, where L and h_0 to h_{L-1} are coefficients, x_n is the input value, x_{n-I} is the input value pervious to sample i, and y_n is the output value.

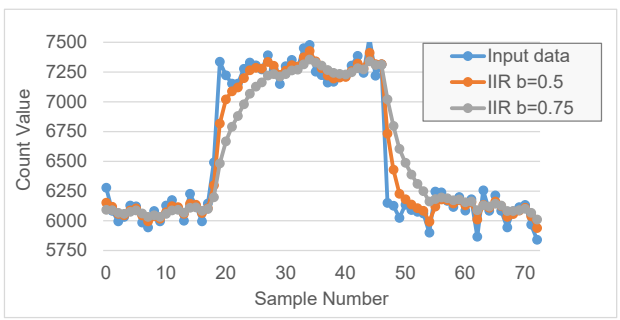
$$y_n = \sum_{i=0}^{L-1} h_i \cdot x_{n-i}$$

5.3 Usage Examples

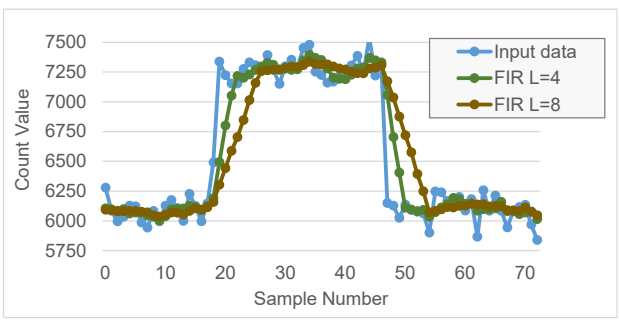
This section provides examples of noise removal using IIR and FIR filters. Table 5-2 shows filter conditions and Figure 5-2 shows an example of random noise removal.

Table 5-2 Filter Usage Examples

Filter Format	Condition 1	Condition 2	Remarks
Single-pole first-order IIR	b=0.5	b=0.75	
FIR	L=4 h_0~ h_{L-1}=0.25	L=8 h_0~ h_{L-1}=0.125	Use as simple moving average



(a) Single-pole first-order IIR Filter



(b) FIR Filter

Figure 5-2 Noise Removal Examples

5.4 Median Filter

A median filter is a filter that extracts the median value from an arbitrary number of sampling data and effectively removes pulsed noise that appears in measured values. The median filter sorts the input sampling data in order of size and then uses the median of the sorted results as the output value. This removes the pulsed noise input to the filter that is less than half the sampling data length.

5.4.1 Usage Example

The following shows an example of the removal of pulsed noise when using a median filter. Table 5-3 lists the filter usage conditions, Figure 5-3 and Figure 5-4 show the pulsed noise removal example.

Table 5-3 Filter Usage Conditions

Filter Type	Condition	Setting Value
Median	Sampling data length	3

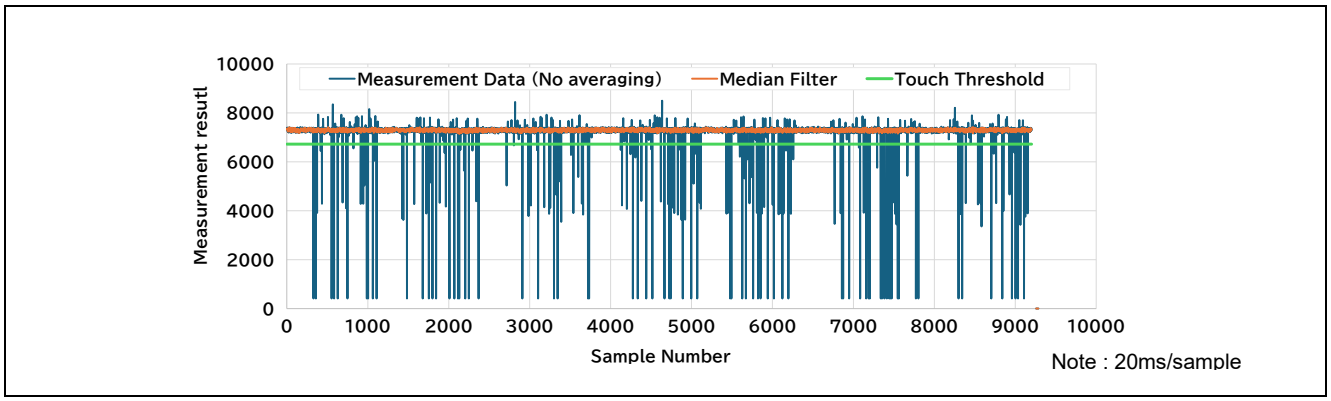


Figure 5-3 Pulsed Noise Removal Example

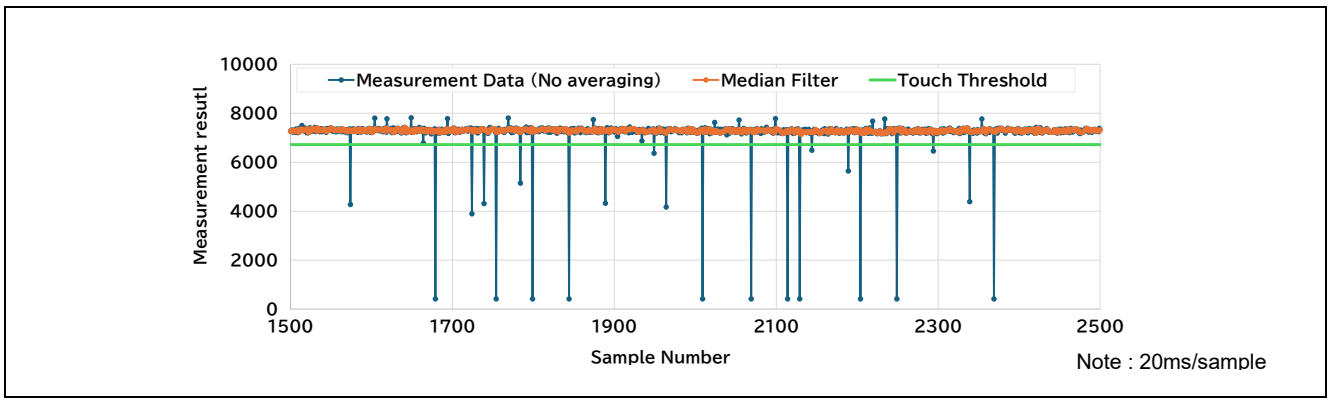


Figure 5-4 Pulsed Noise Removal Example (partially enlarged)

5.5 Usage Notes Regarding Measurement Cycle

The frequency characteristics of software filters change depending on the accuracy of the measurement cycle. In addition, you may not obtain expected filter characteristics due to deviations or variations in the measurement cycle. To focus priority on filter characteristics, use a high-speed on-chip oscillator (HOCO) or an external crystal oscillator as the main clock. We also recommend managing touch measurement execution cycles with a hardware timer.

6. Evaluation Results

The CTSU measured values obtained when using the noise suppression devices described in this guide are shown as reference data. The data shows the evaluation results (performance) when combining a Renesas capacitive touch evaluation board and a power supply IC evaluation board. The data provided here does not guarantee the electrical characteristics of each MCU. When designing your board, always create prototypes and perform sufficient evaluations to determine whether the devices are appropriate for your design.

6.1 Evaluation Conditions

Table 6-1 shows the hardware conditions.

Table 6-1 Hardware Conditions

Item	Specification
Evaluation board	RA2L1 Capacitive Touch Evaluation System (RTK0EG0022S01001BJ) • CPU board: RA2L1 Cap Touch CPU Board (RTK0EG0018C01001BJ v1.0) • Touch electrode board: Self-capacitance Touch Electrode Board (RTK0EG0019B01002BJ v1.1)
MCU	RA2L1 (R7FA2L1AB2DFP) On-board capacitive touch sensor: CTSU2
Operating frequency	48MHz（HOCO）
Power supply unit	5.0V (iW1810-00 For 5V600mA AC-DC SMPS Design P/N: EBC10013)

Figure 6-1 shows the evaluated touch electrode. The self-capacitive touch electrode board (RTK0EG0019B01002BJ v1.1) and touch button labeled TS-B1 were used for testing.

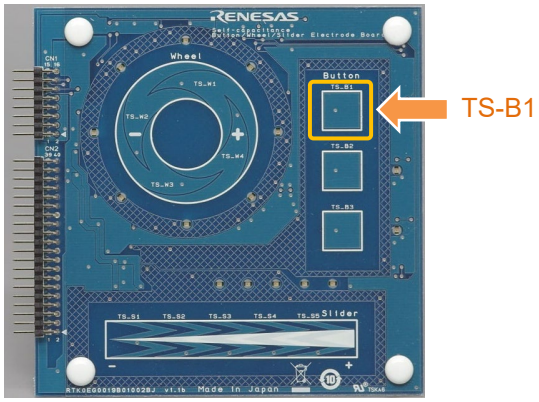


Figure 6-1 Tested Touch Electrode (TS-B1)

Table 6-2 shows the software development environment.

Table 6-2 Software Development Environment

Item	Specification
Integrated development environment (IDE)	Renesas e² studio Version: 2024-01
C Compiler	GCC ARM Embedded 10.3.1.20210824
RA FSP	Version 5.1.0
Development Assistance Tool for Capacitive Touch Sensors	QE for Capacitive Touch V3.3.0
Emulator	Renesas E2 emulator Lite

Table 6-3 shows the software conditions.

Table 6-3 Software Conditions

Item	Setting
Electrodes	TS-B1 of RTK0EG0019B01002BJ v1.1 (connected to TS11 of RA2L1) Active shield: enabled (connected to TS0 of RA2L1)
Touch sensor parameters	Uses auto-tuning process results of QE for Capacitive Touch unless otherwise noted • No. of multi-frequency measurements: 3 frequencies • No. of measurements/measurement period: 0.128ms • Drive pulse frequencies: f1 = 1MHz, f2 = 0.859MHz, f3 = 1.141MHz • Measurement current range: normal current (40 μA) • Non-measurement channel output: same pulse phase output
Cap Touch parameters	• Drift Correction Interval: 255 • Moving Average Filter Depth: 4 — The filters listed in 5 Software Filters are unused.
Measurement cycle	20ms (cycle is generated by hardware timer (AGT) and started by polling process)
Other	All LEDs on the touch electrode board are ON.

Figure 6-2 shows the auto-tuning results from QE for Capacitive Touch (RTK0EG0022S01001BJ).

Method	Kind	Name	Touch Sensor	Parasitic Capacitance[pF]	Sensor Drive Pulse Frequency[MHz]	Threshold	Scan Time[ms]	Overflow
config01	Button(self)	TS_B1	TS11	13.139	1.0	529	0.576	None
config01	Button(self)	TS_B2	TS10	14.924	1.0	553	0.576	None
config01	Button(self)	TS_B3	TS09	11.646	1.0	580	0.576	None
config01	Shield Electrode Pin	Shield00	TS00	49.062	-	-	-	-
config02	Shield Electrode Pin	Shield01	TS08	47.688	-	-	-	-
config02	Button(self)	TS_S1	TS04	11.583	1.0	405	0.576	None
config02	Button(self)	TS_S2	TS02	9.938	1.0	369	0.576	None
config02	Button(self)	TS_S3	TS05	10.938	1.0	397	0.576	None
config02	Button(self)	TS_S4	TS07	11.694	1.0	422	0.576	None
config02	Button(self)	TS_S5	TS06	11.833	1.0	453	0.576	None
config03	Button(self)	TS_W4	TS32	12.34	1.0	499	0.576	None
config03	Shield Electrode Pin	Shield02	TS14	45.694	-	-	-	-
config03	Button(self)	TS_W1	TS18	13.16	1.0	530	0.576	None
config03	Button(self)	TS_W2	TS21	13.056	1.0	553	0.576	None
config03	Button(self)	TS_W3	TS23	13.194	1.0	487	0.576	None

Figure 6-2 Auto-tuning Results from QE for Capacitive Touch (RTK0EG0022S01001BJ)

The evaluation results shown below are based on data obtained using multi-frequency measurements with CTSU2. For more details regarding the multi-frequency measurement function and measurement value selection process (majority decision), refer to 3.3.1 Multi-frequency Measurement.

Figure 6-3 shows how to read the evaluation results of this document.

(a) Shows the multi-frequency measurement results: 3 separate frequency measurements (measured values of f1, f2, and f3)
(b) Shows the majority decision results: majority decision obtained from the results of (a) after applying the moving average to the measured values.

In step (b), majority decision processing combines two of the three frequencies obtained in (a), which doubles the amount of data. Therefore, graph (b) has been adjusted to twice the scale of graph (a)

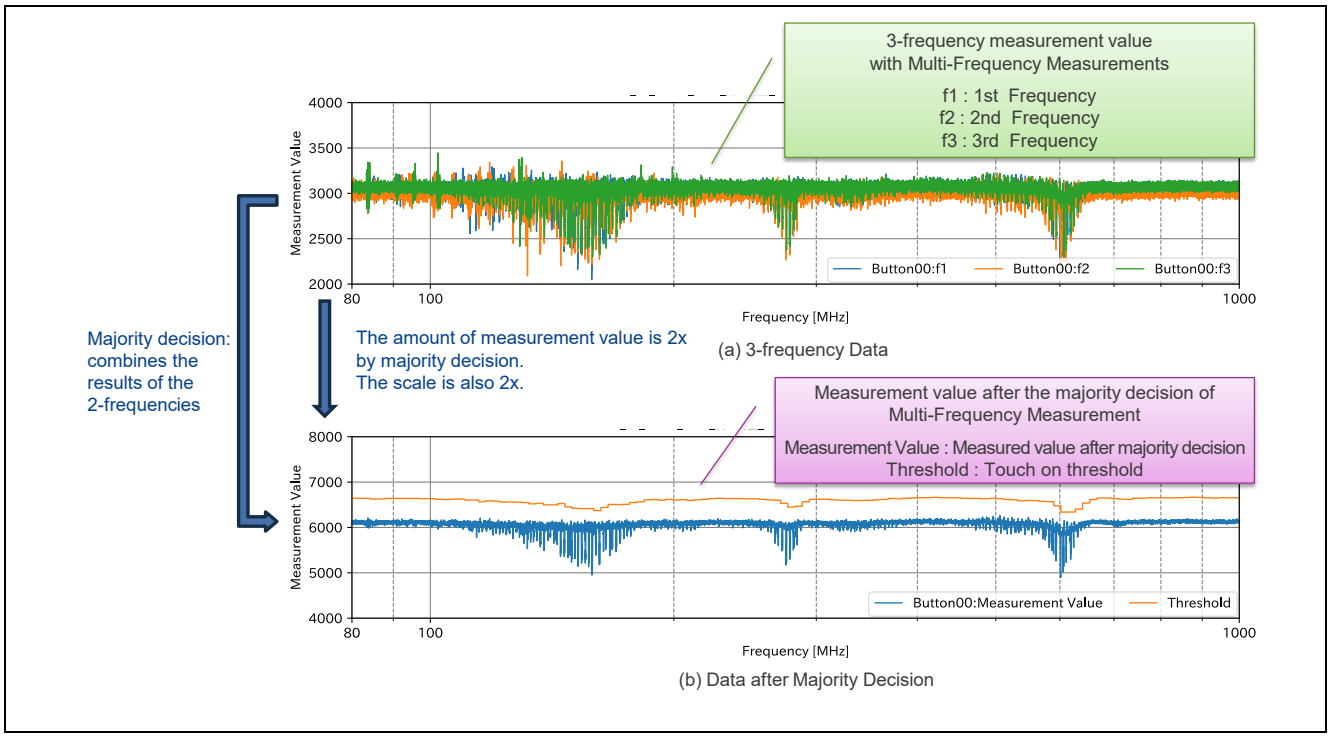


Figure 6-3 How to Read Evaluation Results

6.2 Radiated Immunity (IEC61000-4-3)

6.2.1 Test Conditions

Table 6-4 lists the radiated immunity test conditions, Figure 6-4 shows the test environment block diagram, and Figure 6-5 shows the text environment. The tests conducted for this guide were conducted in accordance with the IEC61000-4-3 standard.

Table 6-4 Radiation Immunity Test Conditions

Item	Setting	Notes
Test voltage	60V/m ±10%	
Test frequency	・80MHz to1GHz ・1GHz to 6GHz	
Frequency step	1.0%	
Modulation conditions	1kHz sine wave AM 80%	
Dwell time	1.0 second	
Electromagnetic field direction	Horizontal, vertical	Irradiation on the evaluation board and touch electrode surface

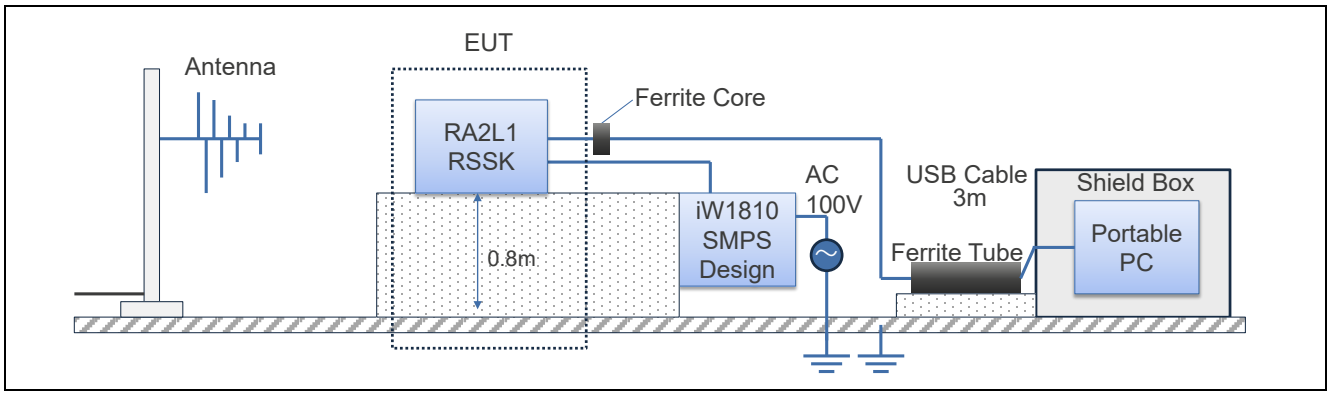


Figure 6-4 Test Environment Block Diagram

With this test, we wanted to evaluate the effect of only the patterns on the evaluation board as much as possible. The power cable (1.2m) and the communication cable for connecting to the PC (3m USB cable) were arranged to flow away from the connector to avoid influence from radio waves, and horizontally and vertically polarized waves were applied to the touch electrode surface of the evaluation board.

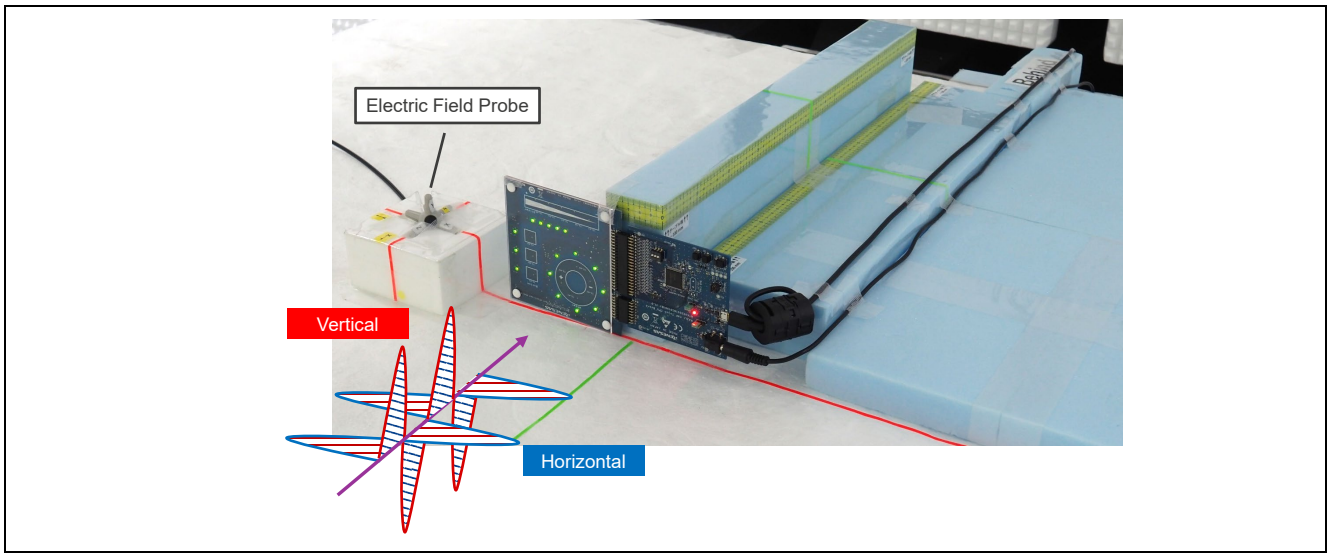


Figure 6-5 Test Environment

6.2.2 Common Mode Choke

Table 6-5 lists the parts used and Figure 6-6 shows the common mode choke placement. This evaluation shows the results when using a choke with an impedance of 100 Ω.

Table 6-5 Parts Used in Test

Part	Impedance Specification (100MHz)
Murata DLW5BTM101SQ2L	100Ω

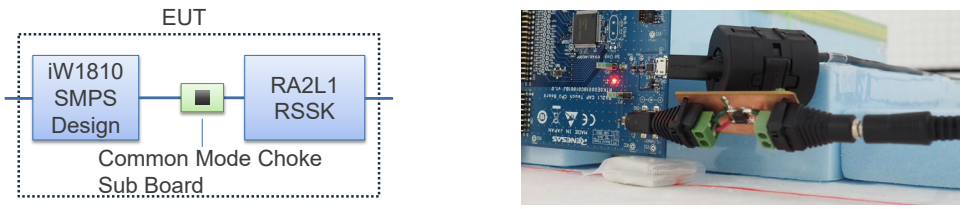
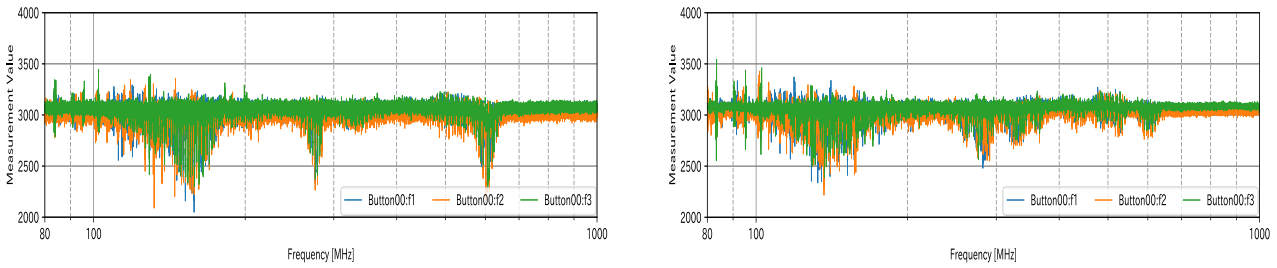


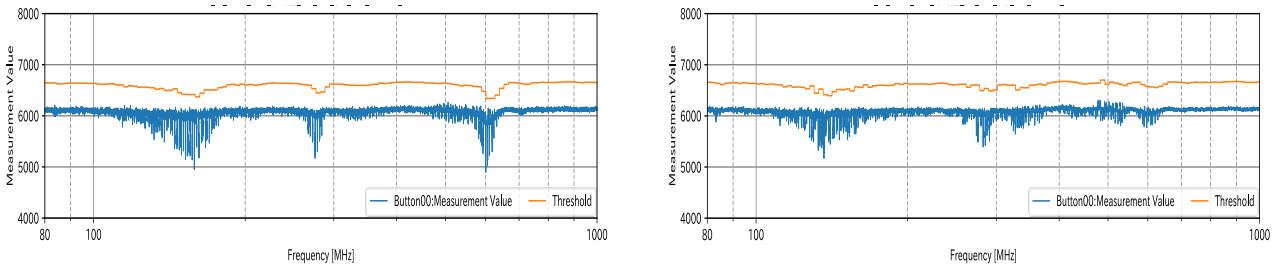
Figure 6-6 Common Mode Choke Placement

Figure 6-7 to Figure 6-10 show the evaluation results. Without the common mode choke, radiated noise affected results at 180MHz, 260MHz, and 600MHz, but noise was reduced when using the common mode choke.



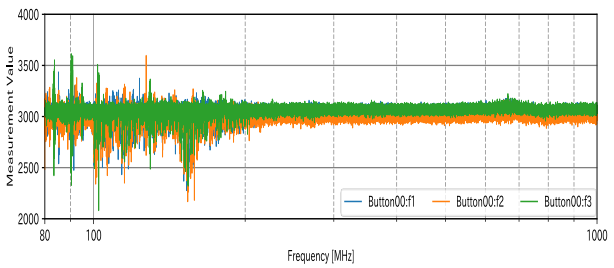
(a) Without common mode choke (b) With common mode choke

Figure 6-7 Common Mode Choke Data 3-frequency Data (horizontal polarization)

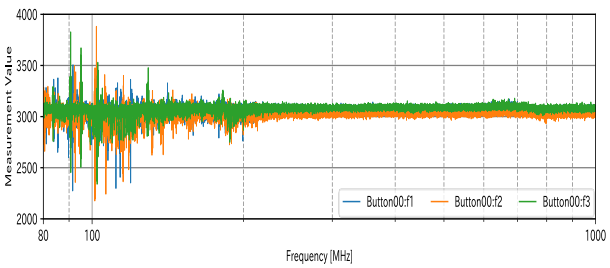


(a) Without common mode choke (b) With common mode choke

Figure 6-8 Common Mode Choke Data after Majority Decision (horizontal polarization)

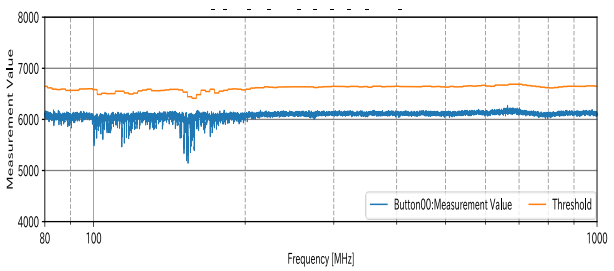


(a) Without common mode choke

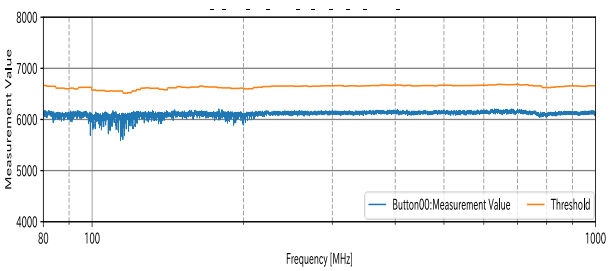


(b) With common mode choke

Figure 6-9 Common Mode Choke 3-frequency Measurement Data (vertical polarization)



(a) Without common mode choke



(b) With common mode choke

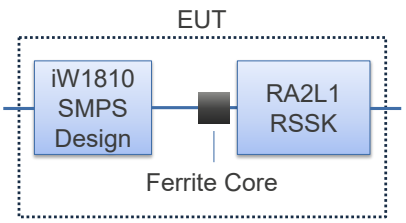
Figure 6-10 Common Mode Choke Data after Majority decision (vertical polarization)

6.2.3 Ferrite Core

Table 6-6 lists the parts used in the test, and Figure 6-11 shows the ferrite core placement. The results show the amount of noise reduction according to the number of turns.

Table 6-6 Parts Used in Test

Parts Used	Number of Turns
SEIWA E04SR200935A	1 turn
	2 turns



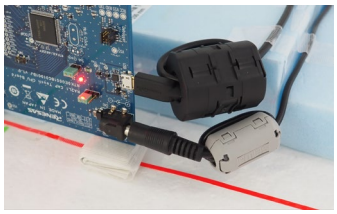
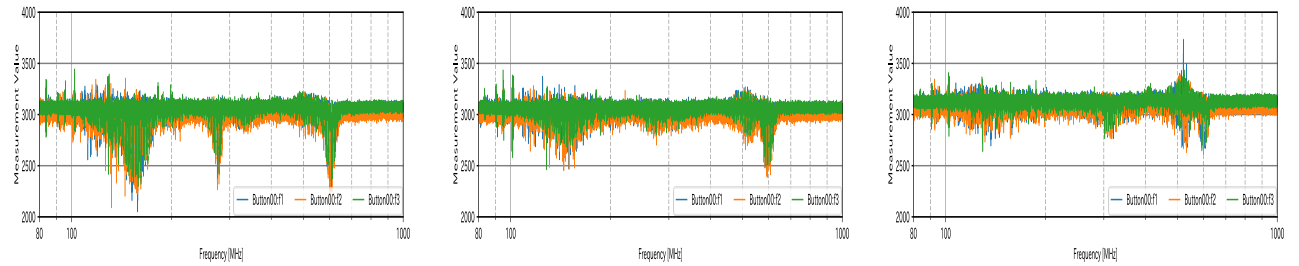


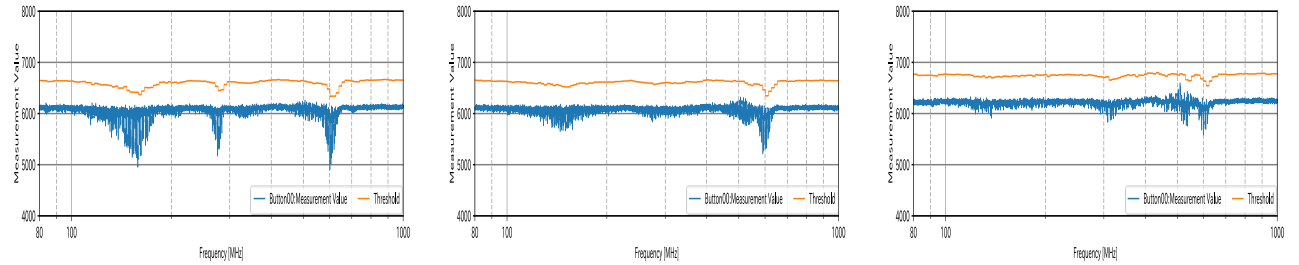
Figure 6-11 Ferrite Core Placement

Figure 6-12 to Figure 6-15 show the evaluation results. Without the ferrite core, radiated noise affected results at 180MHz, 260MHz, and 600MHz, but noise was reduced using the ferrite core. The greater the number of turns, the more noise was reduced.



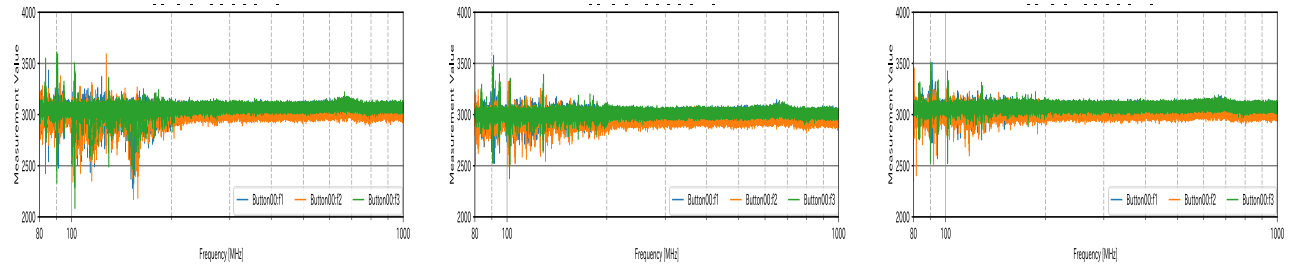
(a) Without ferrite core (b) Ferrite core (1 turn) (c) Ferrite core (2 turns)

Figure 6-12 Ferrite Core 3-frequency Data (horizontal polarization)



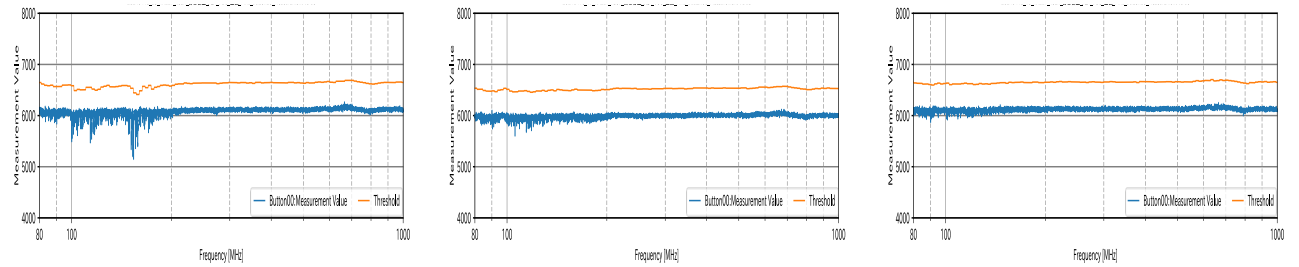
(a) Without ferrite core (b) Ferrite core (1 turn) (c) Ferrite core (2 turns)

Figure 6-13 Ferrite Core Data after Majority Decision (horizontal polarization)



(a) Without ferrite core (b) Ferrite core (1 turn) (c) Ferrite core (2 turns)

Figure 6-14 Ferrite Core 3-frequency Data (vertical polarization)



(a) Without ferrite core (b) Ferrite core (1 turn) (c) Ferrite core (2 turns)

Figure 6-15 Ferrite Core Data after Majority Decision (vertical polarization)

6.3 Conducted Immunity (IEC61000-4-6)

6.3.1 Test Conditions

Table 6-7 lists the conduction immunity test conditions, Figure 6-16 shows the test environment block diagram, and Figure 6-17 shows the test environment. These tests were conducted in accordance with the IEC61000-4-6 standard.

Table 6-7 Conducted Immunity Test Conditions

Item	Setting	Notes
Test level	10Vrms	
Test frequency	0.15MHz to 80MHz	
Frequency step	1.0%	
Modulation conditions	1kHz sine wave AM 80%	
Dwell Time	1.0 second	

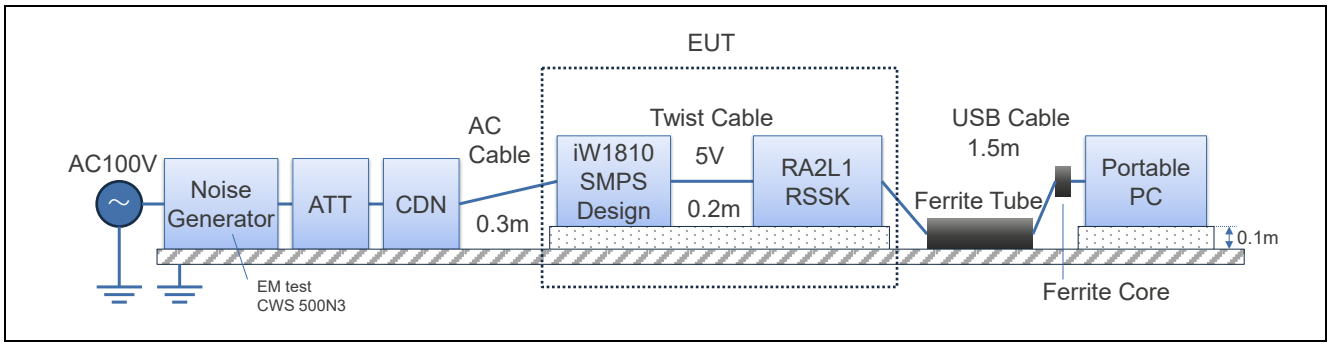


Figure 6-16 Test Environment Block Diagram

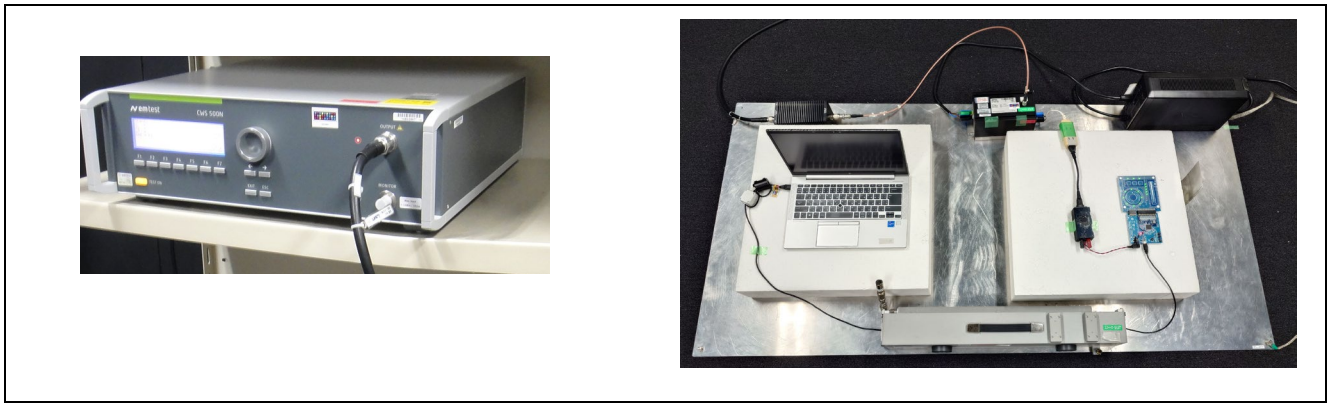


Figure 6-17 Test Environment

Table 6-8 lists the pseudo-finger specifications. As IEC 61000-4-6 refers to a test that simulates the effects human touch on a device during operations, we also conducted an evaluation of the touch condition using an artificial finger.

Table 6-8 Pseudo-finger Specifications

Item	Specification
Material	SUS304 stainless
Outer diameter	Φ10mm
Length	50mm
Grounding method	Connected with a 300mm wire through an RC network of 200pF and 510Ω
Touch ON capacitance increase	Approximately 0.95pF (TS-B1 touch electrode shown in Figure 6-1)

6.3.2 Common Mode Choke

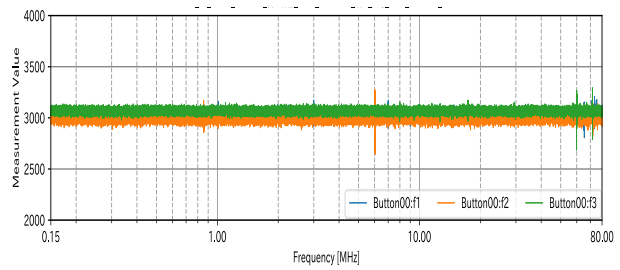
Table 6-9 lists the parts used and Figure 6-18 shows the common mode choke placement. This evaluation shows the results when using a choke with an impedance of 100Ω.

Table 6-9 Parts Used in Test

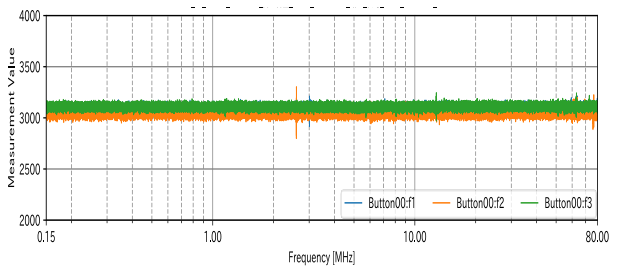
Part	Impedance Specification (100MHz)
Murata DLW5BTM101SQ2L	100Ω

Figure 6-18 Common Mode Choke Placement

Figure 6-19 and Figure 6-20 show the evaluation results. Some noise around 60MHz was evident in the 3-frequency data, but the noise was reduced with the common mode choke. In addition, the noise was further removed based on the majority decision of the multi-frequency measurement.

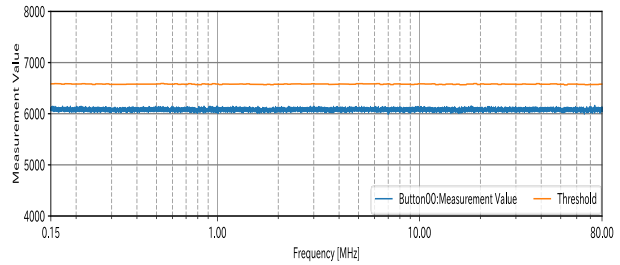


(a) Without common mode choke

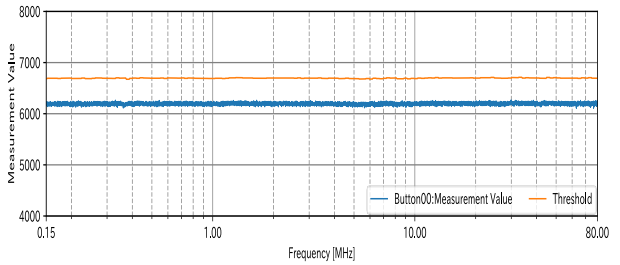


(b) With common mode choke

Figure 6-19 Common Mode Choke 3-frequency Data (touch OFF)



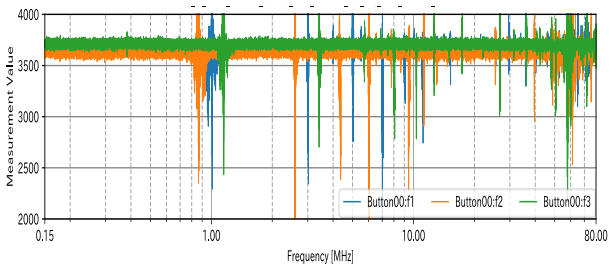
(a) Without common mode choke



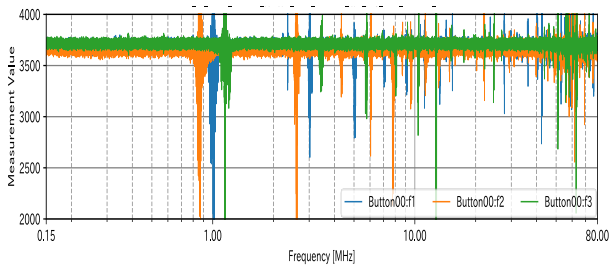
(b) With common mode choke

Figure 6-20 Common Mode Choke Data after Majority decision (touch OFF)

Figure 6-21 and Figure 6-22 show the evaluation results with touch ON. When touch is ON, conducted noise enters the board directly from the touch electrode through the artificial finger, so noise occurs at the CTSU drive pulse frequency (1.0 MHz) and its harmonics in the 3-frequency data. Noise also occurs around 60 MHz. The data after majority decision shows that most noise can be removed, indicating that majority decision in multi-frequency measurement is effective. According to the data after the majority decision, noise occurring around 1.0 MHz and 60 MHz was reduced using a common mode choke.

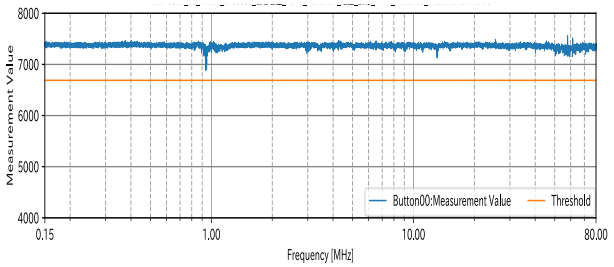


(a) Without common mode choke

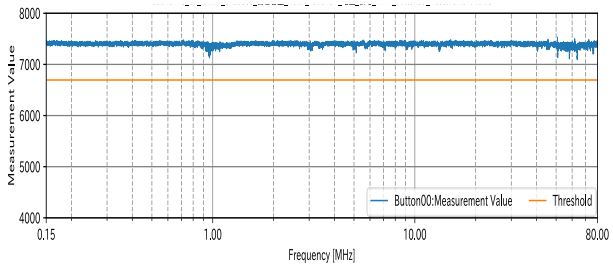


(b) With common mode choke

Figure 6-21 Common Mode Choke 3-frequency Data (touch ON)



(a) Without common mode choke



(b) With common mode choke

Figure 6-22 Common Mode Choke Data after Majority decision (touch OFF)

6.3.3 Ferrite Core

Table 6-10 lists the parts used in the test, and Figure 6-23 shows the ferrite core placement.

Table 6-10 Parts Used in Test

Part	Number of Turns
SEIWA E04SR200935A	1 turn
	2 turns

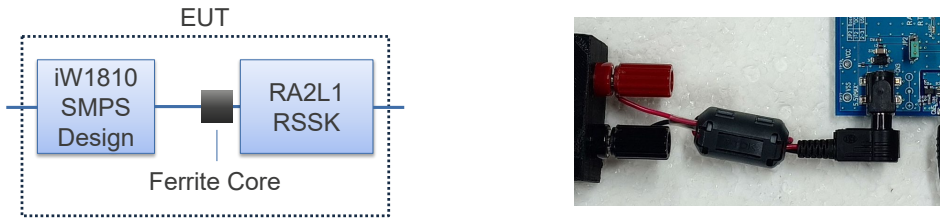
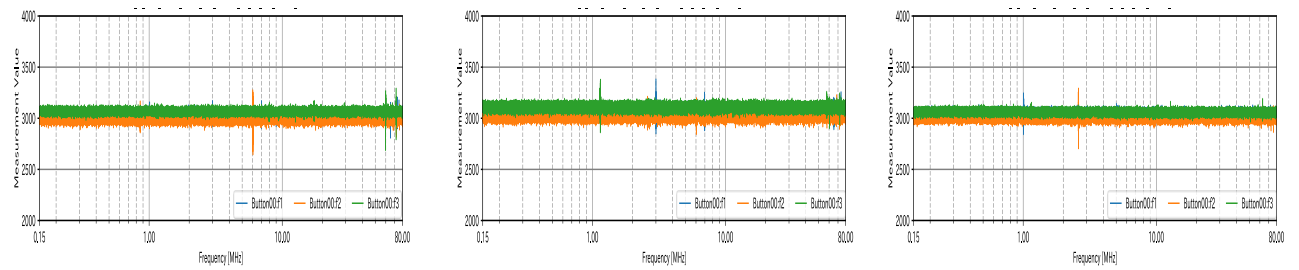


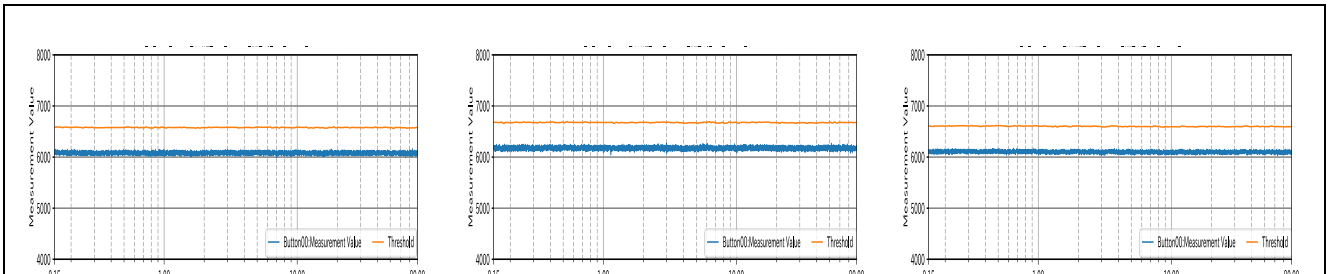
Figure 6-23 Ferrite Core Placement

Figure 6-24 and Figure 6-25 show the evaluation results with touch OFF. Some noise around 60MHz was evident in the 3-frequency data, but the noise was reduced with a ferrite core. In addition, the noise was further reduced based on the majority decision of the multi-frequency measurement.



(a) Without ferrite core (b) Ferrite core (1 turn) (c) Ferrite core (2 turns)

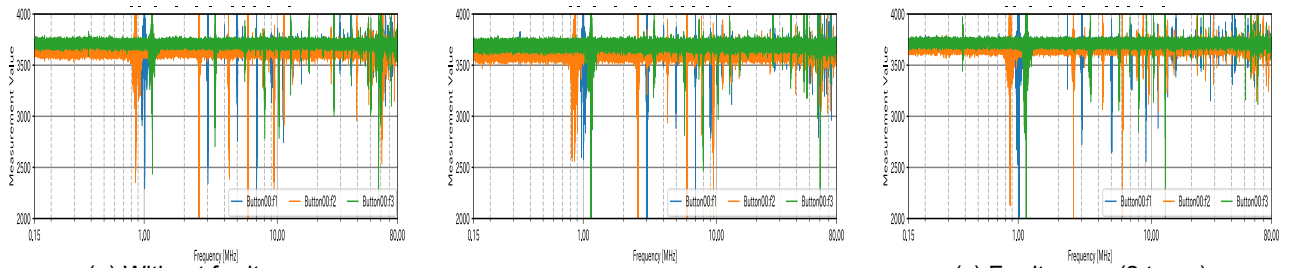
Figure 6-24 Ferrite Core 3-frequency Data (touch OFF)



(a) Without ferrite core (b) Ferrite core (1 turn) (c) Ferrite core (2 turns)

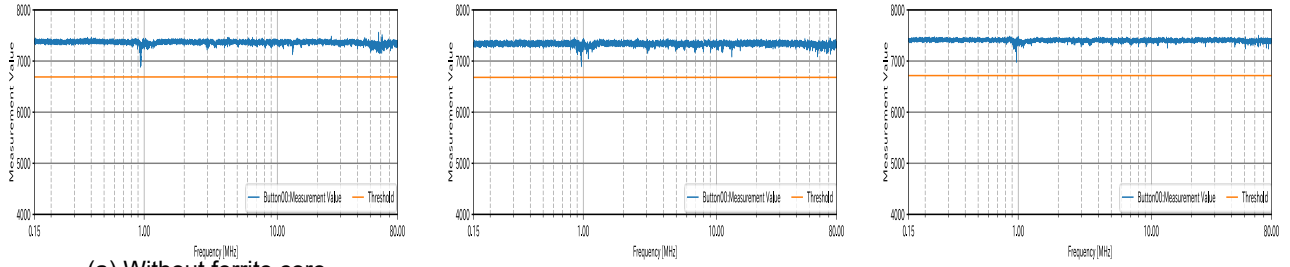
Figure 6-25 Ferrite Core Data after Majority Decision (touch OFF)

Figure 6-26 and Figure 6-27 shows the evaluation results with touch ON. The 3-frequency data is affected by noise from the CTSU drive pulse frequency (1.0 MHz) and its harmonics, as well as noise around 60 MHz. Noise around 60 MHz was reduced using the ferrite core. The data after the majority decision shows that most noise was removed by the process, indicating that majority decision of the multi-frequency measurement is effective. Additionally, noise occurring around 1.0 MHz and 60 MHz was reduced using a ferrite core.



(a) Without ferrite core (b) Ferrite core (1 turn) (c) Ferrite core (2 turns)

Figure 6-26 Ferrite Core 3-frequency Data (touch ON)



(a) Without ferrite core (b) Ferrite core (1 turn) (c) Ferrite core (2 turns)

Figure 6-27 Ferrite Core Data after Majority Decision (touch ON)

6.4 EFT/B (IEC61000-4-4)

6.4.1 Test Conditions

Table 6-11 lists the conduction immunity test conditions, Figure 6-28 shows the test environment block diagram, and Figure 6-29 shows the test environment. These tests were conducted in accordance with the IEC61000-4-4 standard.

Table 6-11 Test Conditions

Item	Setting	Notes
Test voltage	±2kV	
Pulse repetition frequency	5kHz, 100kHz	
Burst cycle	300ms	
Pulses	75	
Testing time	3 minutes	

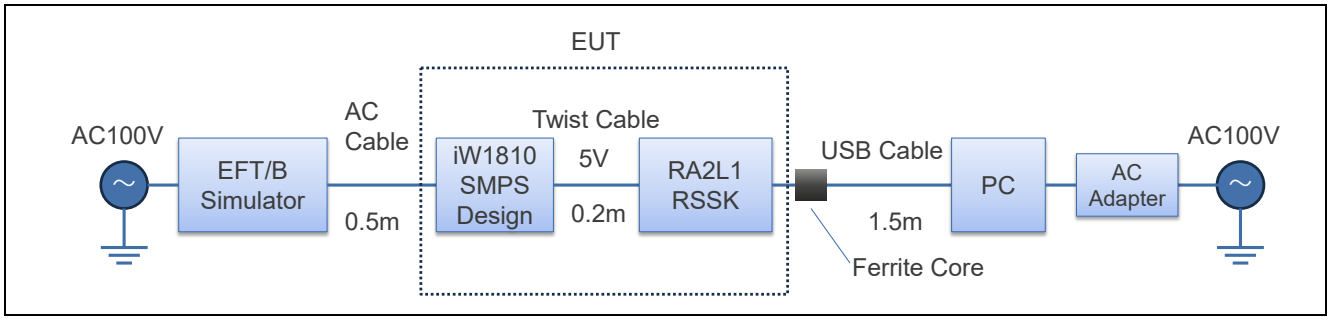


Figure 6-28 Test Environment Block Diagram

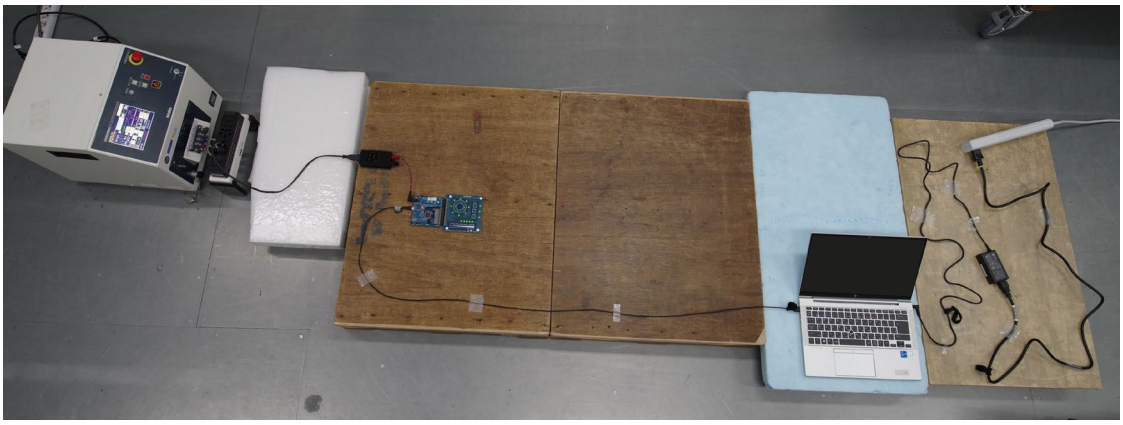


Figure 6-29 Test Environment

6.4.2 Common Mode Choke

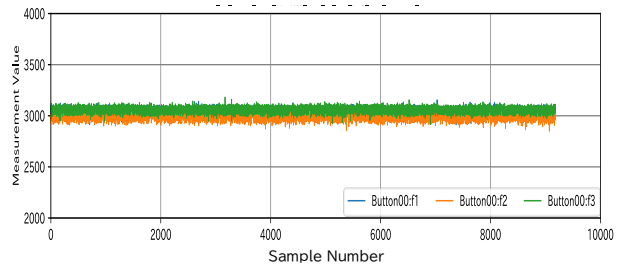
Table 6-12 lists the parts used and Figure 6-30 shows the common mode choke placement. This evaluation shows the results when using a choke with an impedance of 100 Ω.

Table 6-12 Parts Used in Test

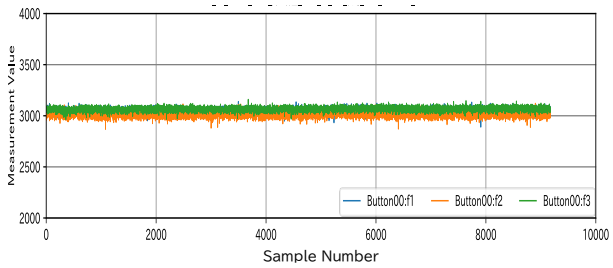
Part	Impedance Specification (100MHz)
Murata DLW5BTM101SQ2L	100Ω

Figure 6-30 Common Mode Choke Placement

Figure 6-31 to Figure 6-34 show the evaluation results with a repetition frequency of 5kHz. Some pulsed noise was evident in the 3-frequency data, it was further reduced based on the majority decision of the multi-frequency measurement.

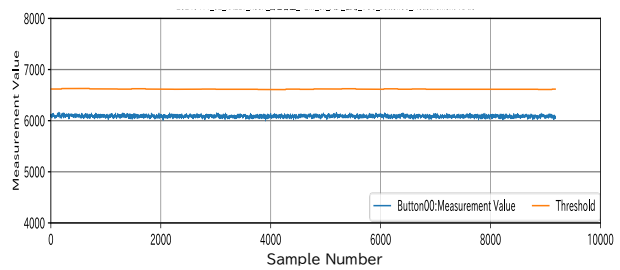


(a) Without common mode choke

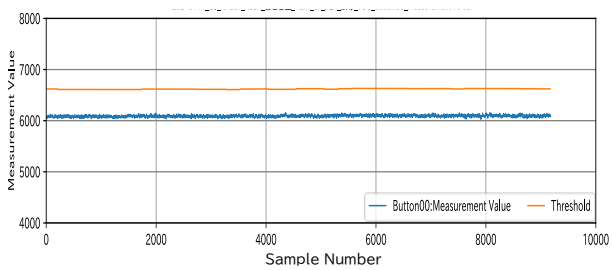


(b) With common mode choke

Figure 6-31 Common Mode Choke 3-frequency Data (+2kV, 5kHz)

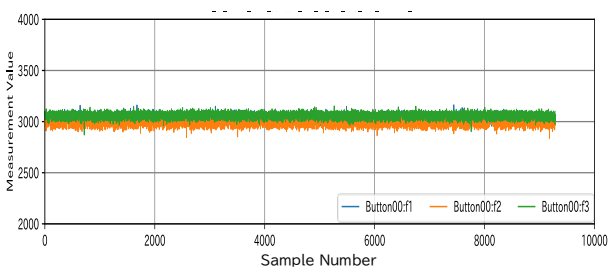


(a) Without common mode choke

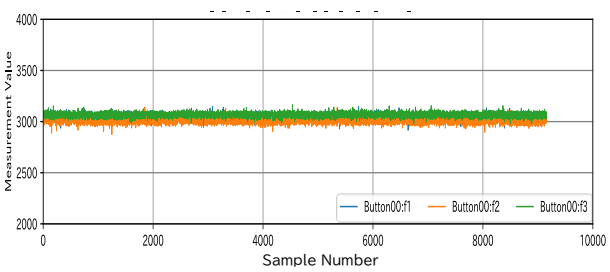


(b) With common mode choke

Figure 6-32 Common Mode Choke Data after Majority Decision (+2kV, 5kHz)

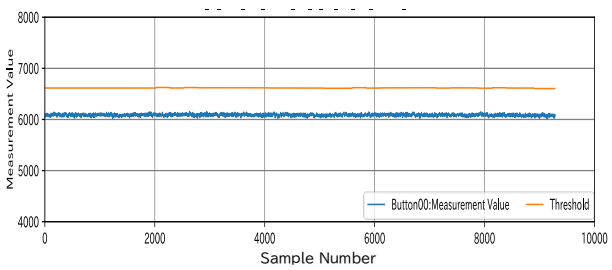


(a) Without common mode choke

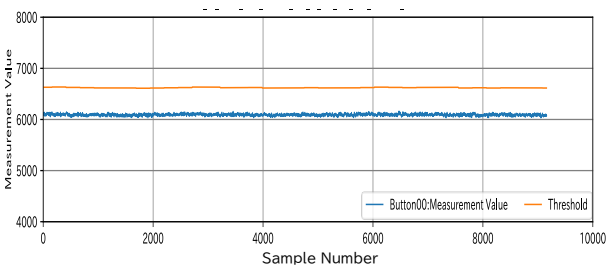


(b) With common mode choke

Figure 6-33 Common Mode Choke 3-frequency Data (-2kV, 5kHz)



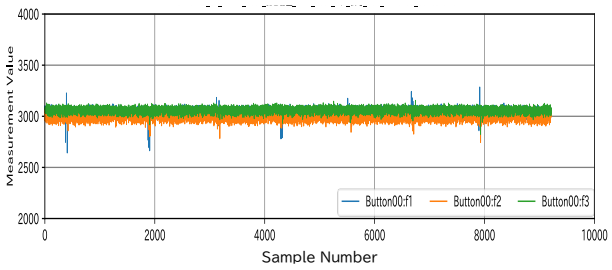
(a) Without common mode choke



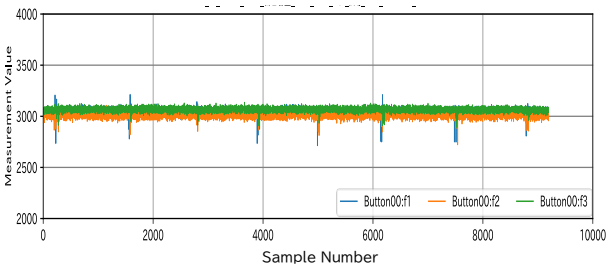
(b) With common mode choke

Figure 6-34 Common Mode Choke Data after Majority Decision (-2kV, 5kHz)

Figure 6-35 to Figure 6-38 show the evaluation results with a pulse repetition frequency of 100kHz. Although the pulsed noise in the 3-frequency data was larger than with a repetition frequency of 5 kHz, the noise in the measured values was reduced using a common mode choke and was further removed based on the majority decision of the multi-frequency measurement.

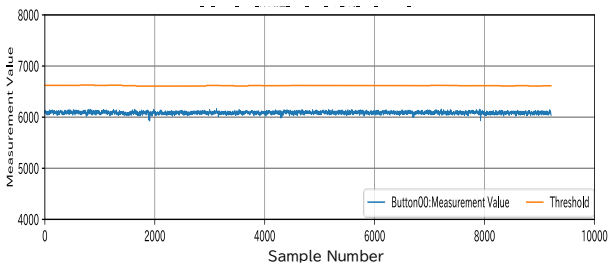


(a) Without common mode choke

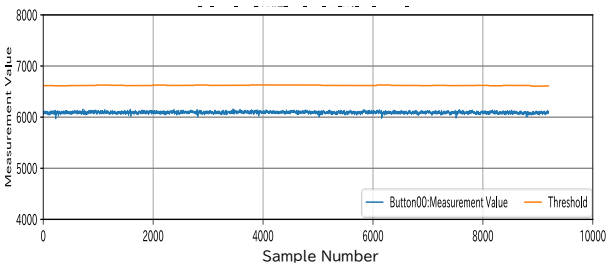


(b) With common mode choke

Figure 6-35 Common Mode Choke 3-frequency Data (+2kV, 100kHz)

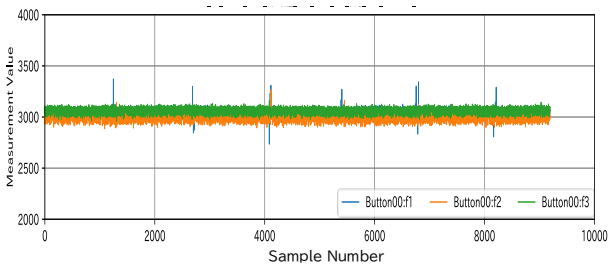


(a) Without common mode choke

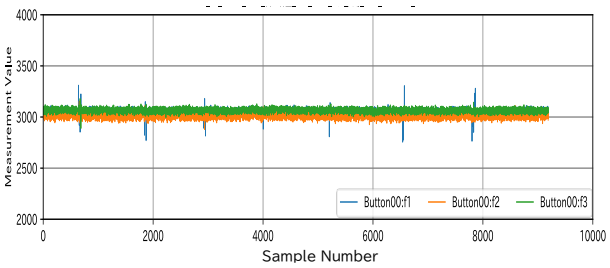


(b) With common mode choke

Figure 6-36 Common Mode Choke Data after Majority Decision (+2kV, 100kHz)

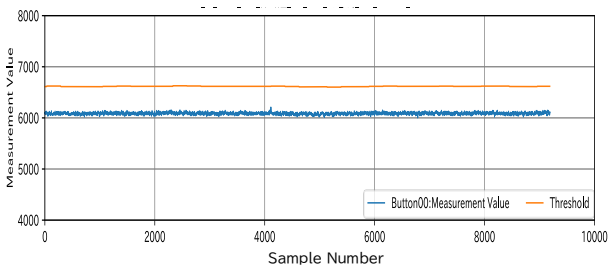


(a) Without common mode choke

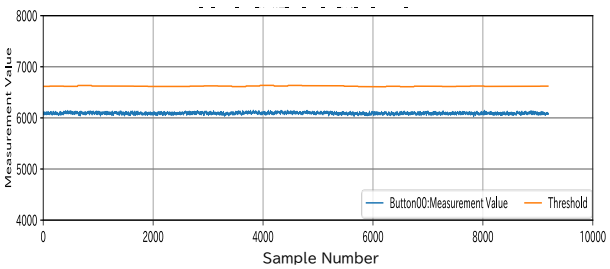


(b) With common mode choke

Figure 6-37 Common Mode Choke 3-frequency Data (-2kV, 100kHz)



(a) Without common mode choke



(b) With common mode choke

Figure 6-38 Common Mode Choke Data after Majority Decision (-2kV, 100kHz)

6.4.3 Ferrite Core

Table 6-13 lists the parts used in the test, and Figure 6-39 shows the ferrite core placement. This evaluation shows the noise reduction effect according to the number of turns.

Table 6-13 Parts Used in Test

Part	Number of Turns
SEIWA E04SR200935A	1 turn
	2 turns

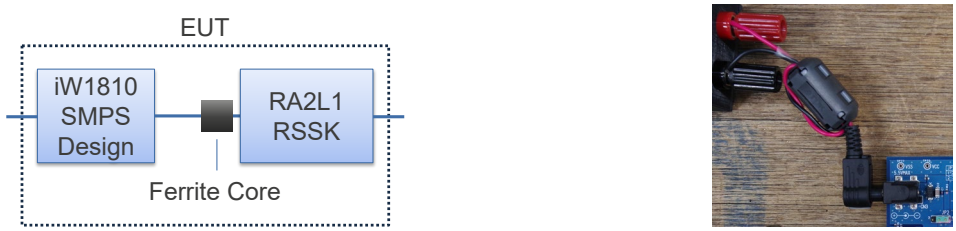
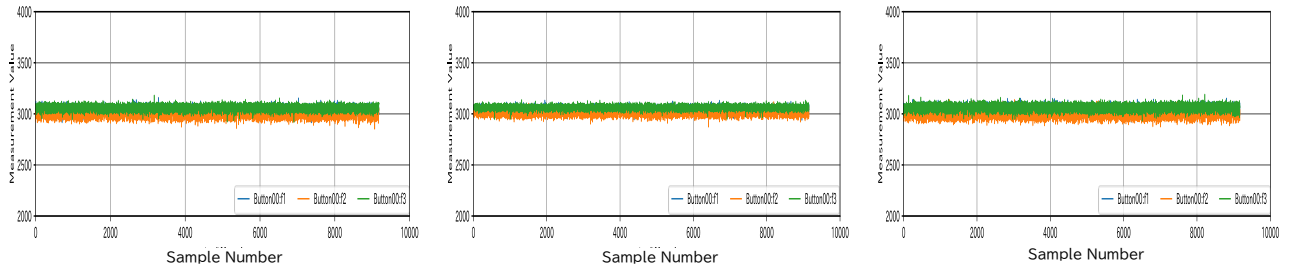


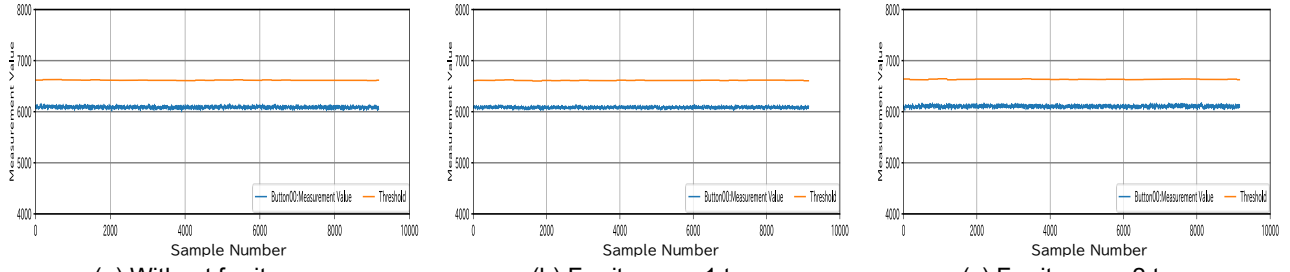
Figure 6-39 Ferrite Core Placement

Figure 6-40 to Figure 6-43 show the evaluation results with a pulse repetition frequency of 5kHz. Although the pulsed noise in the 3-frequency data was larger than with a repetition frequency of 5 kHz, it was further removed based on the majority decision of the multi-frequency measurement.



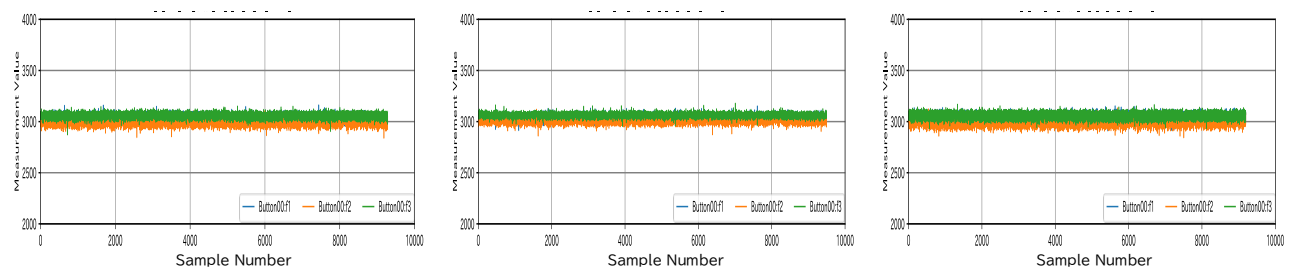
(a) Without ferrite core (b) Ferrite core, 1 turn (c) Ferrite core, 2 turns

Figure 6-40 Ferrite Core 3-frequency Data (+2kV, 5kHz)



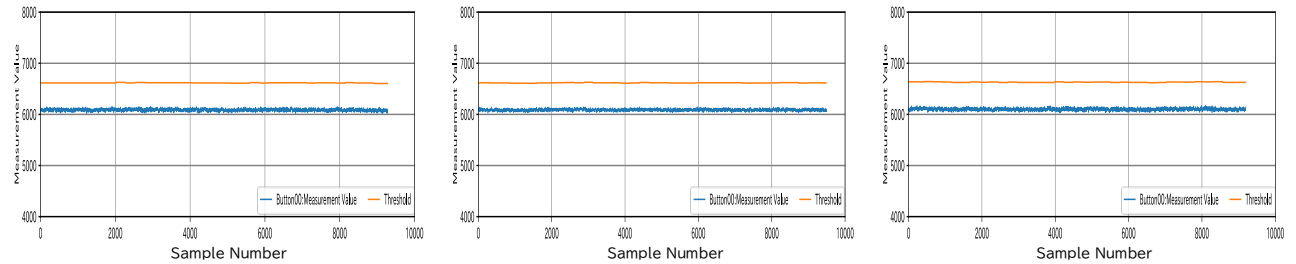
(a) Without ferrite core (b) Ferrite core, 1 turn (c) Ferrite core, 2 turns

Figure 6-41 Ferrite Core Data after Majority Decision (+2kV, 5kHz)



(a) Without ferrite core (b) Ferrite core, 1 turn (c) Ferrite core, 2 turns

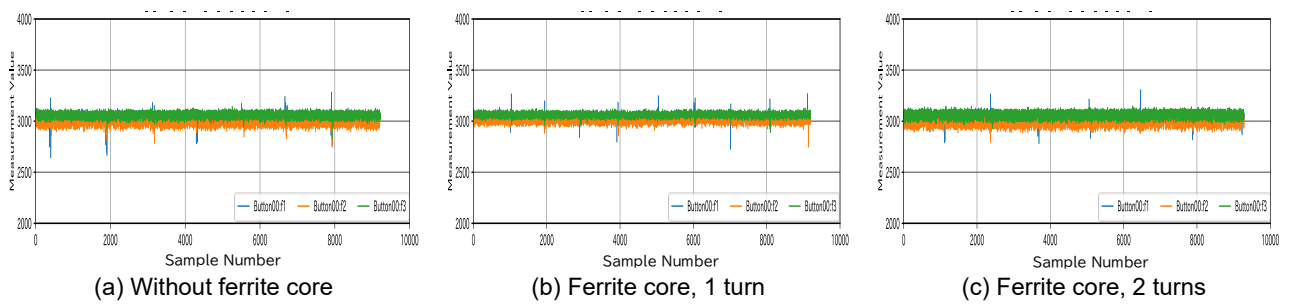
Figure 6-42 Ferrite Core 3-frequency Data (-2kV, 5kHz)



(a) Without ferrite core (b) Ferrite core, 1 turn (c) Ferrite core, 2 turns

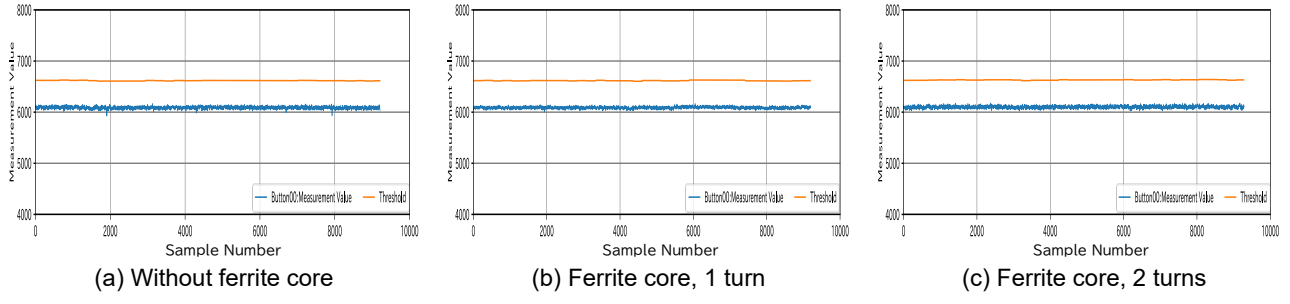
Figure 6-43 Ferrite Core Data after Majority Decision (-2kV, 5kHz)

Figure 6-44 to Figure 6-47 show the evaluation results with a pulse repetition frequency of 100kHz. Although the pulsed noise in the 3-frequency data was larger than with a repetition frequency of 5 kHz, the noise in the measured values was reduced using a ferrite core and was further reduced based on the majority decision of the multi-frequency measurement.



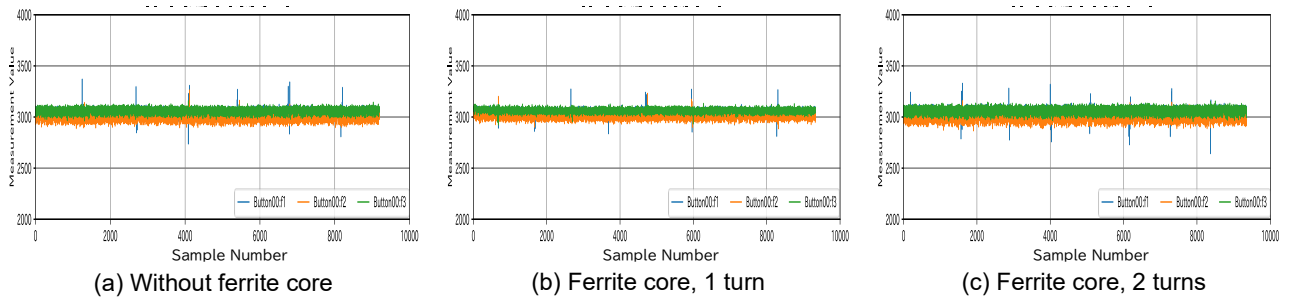
(a) Without ferrite core (b) Ferrite core, 1 turn (c) Ferrite core, 2 turns

Figure 6-44 Ferrite Core 3-frequency Data (+2kV, 100kHz)



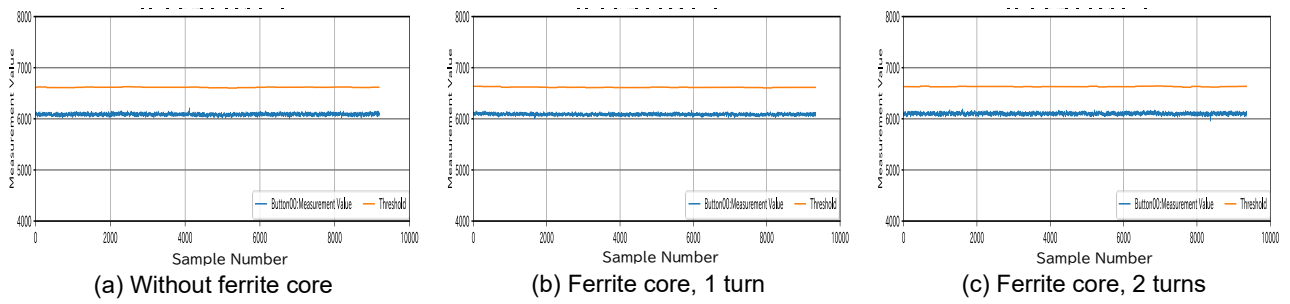
(a) Without ferrite core (b) Ferrite core, 1 turn (c) Ferrite core, 2 turns

Figure 6-45 Ferrite Core Data after Majority Decision (+2kV, 100kHz)



(a) Without ferrite core (b) Ferrite core, 1 turn (c) Ferrite core, 2 turns

Figure 6-46 Ferrite Core 3-frequency Data (-2kV, 100kHz)



(a) Without ferrite core (b) Ferrite core, 1 turn (c) Ferrite core, 2 turns

Figure 6-47 Ferrite Core Data after Majority Decision (-2kV, 100kHz)

Glossary

Term	Definition
CTSU	Capacitive Touch Sensing Unit. Also used in CTSU1 and CTSU2.
CTSU1	Second generation CTSU IP. “1” is added to differentiate from CTSU2.
CTSU2	Third generation CTSU IP.
CTSU driver	CTSU driver software bundled in Renesas Software packages.
CTSU module	A unit of CTSU driver software that can be embedded using the Smart Configurator.
TOUCH middleware	Middleware for touch detection processing when using CTSU bundled in Renesas software packages.
TOUCH module	A unit of TOUCH middleware that can be embedded using the Smart Configurator.
r_ctsu module	The CTSU driver displayed in the Smart Configurator.
rm_touch module	The TOUCH module displayed in the Smart Configurator
CCO	Current Control Oscillator. The current-controlled oscillator used in capacitive touch sensors. Also written as ICO in some documents.
ICO	Same as CCO.
TSCAP	A capacitor for stabilizing the CTSU internal voltage.
Damping resistor	A resistor used to reduce pin damage or effects due to external noise. For details, refer to Capacitive Touch Electrode Design Guide (R30AN0389).
VDC	Voltage Down Converter. Power supply circuit for capacitive sensor measurement built into the CTSU.
Multi-frequency measurement	A function that uses multiple sensor unit clocks with differing frequencies to measure touch; indicates the multi-clock measurement function.
Sensor drive pulse	Signal that drives the switched capacitor.
Synchronous noise	Noise at the frequency that matches the sensor drive pulse.
EUT	Equipment Under Test. Indicates the device to be tested.
LDO	Low Dropout Regulator
PSRR	Power Supply Rejection Ration
FSP	Flexible Software Package
FIT	Firmware Integration Technology。
SIS	Software Integration System

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May 31, 2023	-	Initial revision
2.00	Dec 25, 2023	-	For IEC61000-4-6
		6	Added common mode noise impact to 2.2
		7	Added items to Table 2-5
		9	Revised text in 3.1, corrected Figure 3-1
		10	In 3.3.1, revised text and added Figure 3-4. Deleted explanation of how to change settings for multi-frequency measurements and added explanation of multi-frequency measurement interference frequency and Figure3-5.
		11	Added reference documents to 3.2.2
		14	Added note concerning TSCAP capacitor GND connection to 4.1.2.2
		15	Added note concerning wiring corner design to 4.2.2
		16	Added 4.3 Conducted Noise Countermeasures
		18	Revised section 5.
3.00	Jun. 28, 2024	6	Corrected Figure 2-2
		9	Added text to 2.4 Added Table 2-8
		12	Corrected vertical axis name in Figure 3-5
		13	Corrected 4.1 heading
		14	Corrected text in 4.1.2.1
		17	Corrected text in 4.3
		19	Added 4.4 EFT Noise Countermeasures
		21	Added IEC61000-4-4 EFT/B to Table 5-1 Corrected Figure 5-1
		23	Renumbered Section 5.4 to Section 5.5 Added 5.4 Median Filter
		24	Added 6. Evaluation Results
4.00	Dec. 27. 2024	8	Corrected the corresponding section numbers in Table 2-5
		9	Added Table 2-8 ESD Countermeasures
		21	Corrected and added TVS diode selection recommendations
		22	Added 4.5 ESD Noise Countermeasures
		23	Corrected Figure 5-1 Added ESD to Table 5-1 EMC Standards and Corresponding Software Filters
		26	Added text to section 6.
		33	Added touch ON capacitance increase to Table 6-5 Pseudo-finger Specifications

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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