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H8SX Family

Buffered Operation of the TPU's Output–Compare Function

Introduction

Buffered operation of the TPU's output–compare function is used to drive toggling that produces an output pulse waveform with varying widths at the high and low levels.

Target Device

H8SX/1653

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3. Description of Modules Used 3
4. Principle of Operation 5
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1. Specification

Buffered operation of the TPU's output–compare function is used to drive output toggling.

- The output of the TIOCA3 pin goes to the "1" level after a power-on reset and produces an output pulse waveform with varying widths at the high and low levels.
- Buffered operation is selected for TGRA_3 and TGRC_3. In this case, the value in the buffer register (TGRC_3) is transferred to the timer general register (TGRA_3) at the same time as the output on the TIOCA3 pin is changed by compare-match A. This makes consecutive setting of TGRA_3 possible.

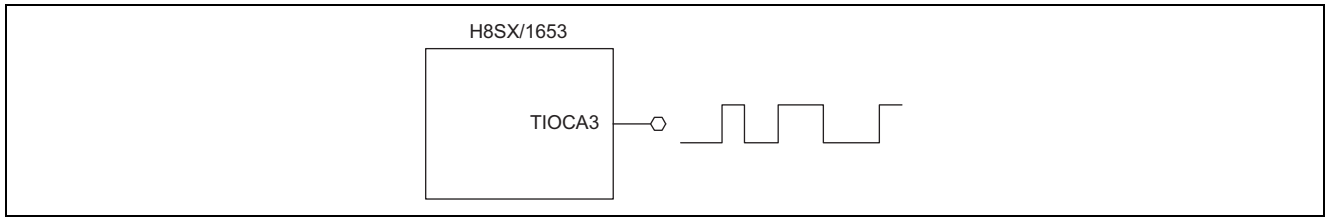


Figure 1 Pulse-Waveform Output through Buffered Operation of a TPU Output–Compare Function

2. Applicable conditions

Table 1 Applicable conditions

Item	Setting	
Operating frequency	Input clock	: 12 MHz
	System clock (Iϕ)	: 24 MHz (input clock frequency × 2)
	Peripheral module clock (Pϕ)	: 24 MHz (input clock frequency × 2)
	External bus clock (Bϕ)	: 24 MHz (input clock frequency × 2)
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, and MD0 = 0, MD_CLK = 0)	

3. Description of Modules Used

- Figure 2 is a block diagram of TPU.

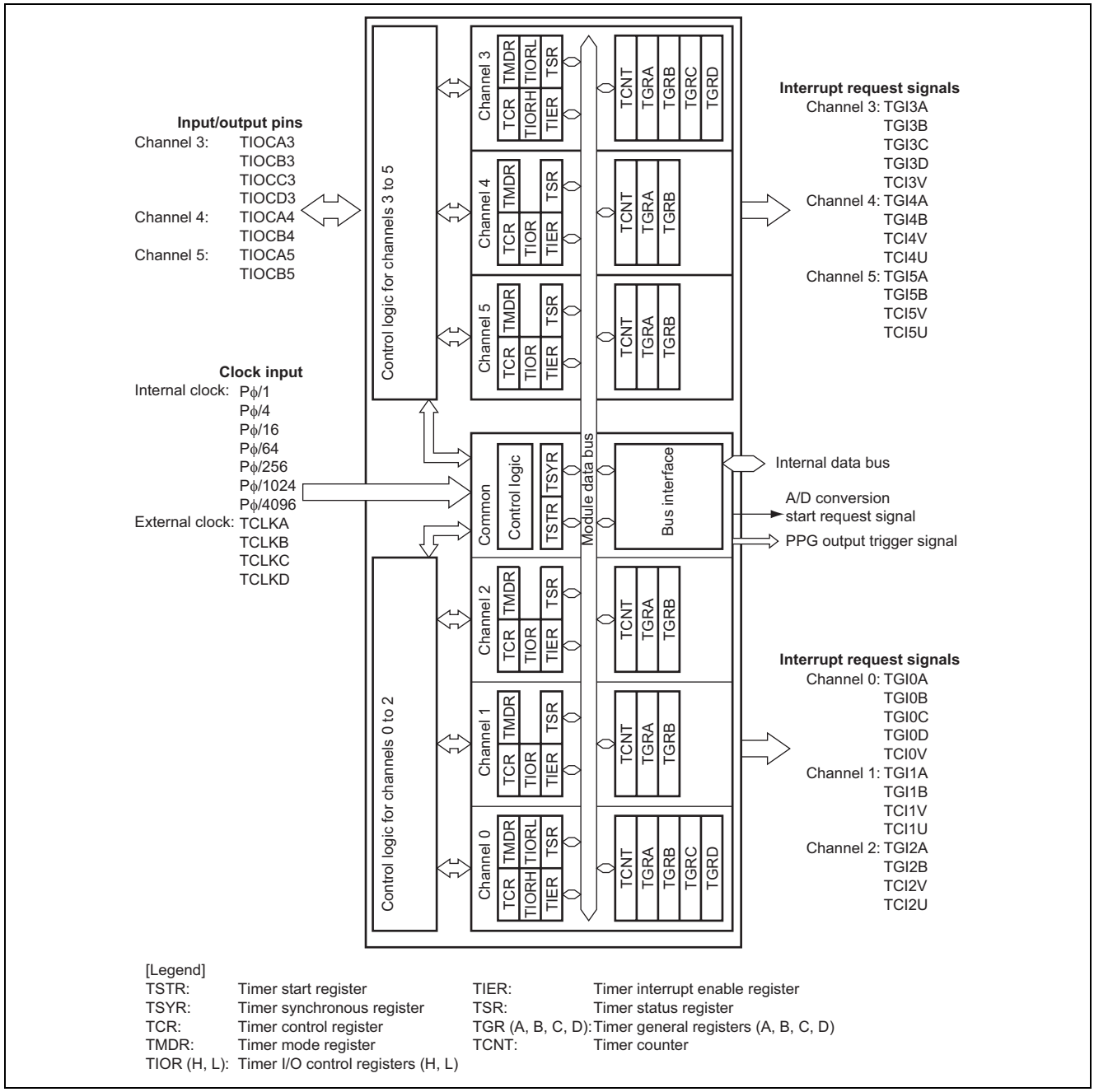


Figure 2 Block diagram of TPU

The following functions of the TPU are employed in this sample application.

- Automatic production of pulse waveforms without software intervention (output–compare)
- Clearing of the counter at the time of a match (counter clearing)
- Inversion of outputs by matches (output toggling)
- Transfer of value from a buffer register to the corresponding timer general register in synchronization with matches (buffered operation)

Explanations of the registers are given below.

- Timer Start Register (TSTR)
  TSTR starts or stops operation for channels 0 to 5. Stop the TCNT counter before setting the operating mode in TMDR or the clock for counting in TCR.

- Timer Control Register_3 (TCR_3)
  TCR controls the TCNT operation for each channel. The TPU has a total of six TCR registers, one for each channel. TCR register settings should only be made while TCNT operation is stopped.

- Timer I/O Control Register H_3 (TIORH_3)
  TIOR controls TGR. The TPU has eight TIOR registers, two each for channels 0 and 3, and one each for channels 1, 2, 4, and 5. Care is required since TIOR is affected by the TMDR setting.
  The initial output specification for TIOR becomes effective when the counter is stopped (the CST bit in TSTR is cleared to 0). Note also that, in PWM mode 2, the output at the point at which the counter is cleared to 0 is specified. When TGRC or TGRD is designated to operate as a buffer, the corresponding TIOR setting is invalid.
  To designate the input capture pin in TIOR, the DDR bit and ICR bit for the corresponding pin should be set to 0 and 1, respectively.

- Timer Counter_3 (TCNT_3)
  TCNT is a 16-bit readable/writable counter. The TPU has six TCNT counters, one for each channel. TCNT is initialized to H'0000 by a reset or in hardware standby mode. TCNT cannot be accessed in 8-bit units. TCNT must always be accessed in 16-bit units.

- Timer General Register A_3 (TGRA_3)
- Timer General Register C_3 (TGRC_3)
  TGR is a 16-bit readable/writable register and has a dual function as an output compare or input capture register. The TPU has 16 TGR registers, four each for channels 0 and 3 and two each for channels 1, 2, 4, and 5. TGRC and TGRD for channels 0 and 3 can also be designated for operation as buffer registers.
  The TGR registers cannot be accessed in 8-bit units; they must always be accessed in 16-bit units. Combinations of TGR and buffer for buffer operation are TGRA and TGRC, TGRB and TGRC.

- Timer Interrupt Enable Register_3 (TIER_3)
  Each TIER controls enabling and disabling of interrupts for the corresponding channel. Each channel has one TIER, so there are six in all.

4. Principle of Operation

Figure 3 illustrates how the TPU's output–compare function works with buffered operation of the general register. To explain the figure, detailed descriptions of processing at the numbered points are given in table 2.

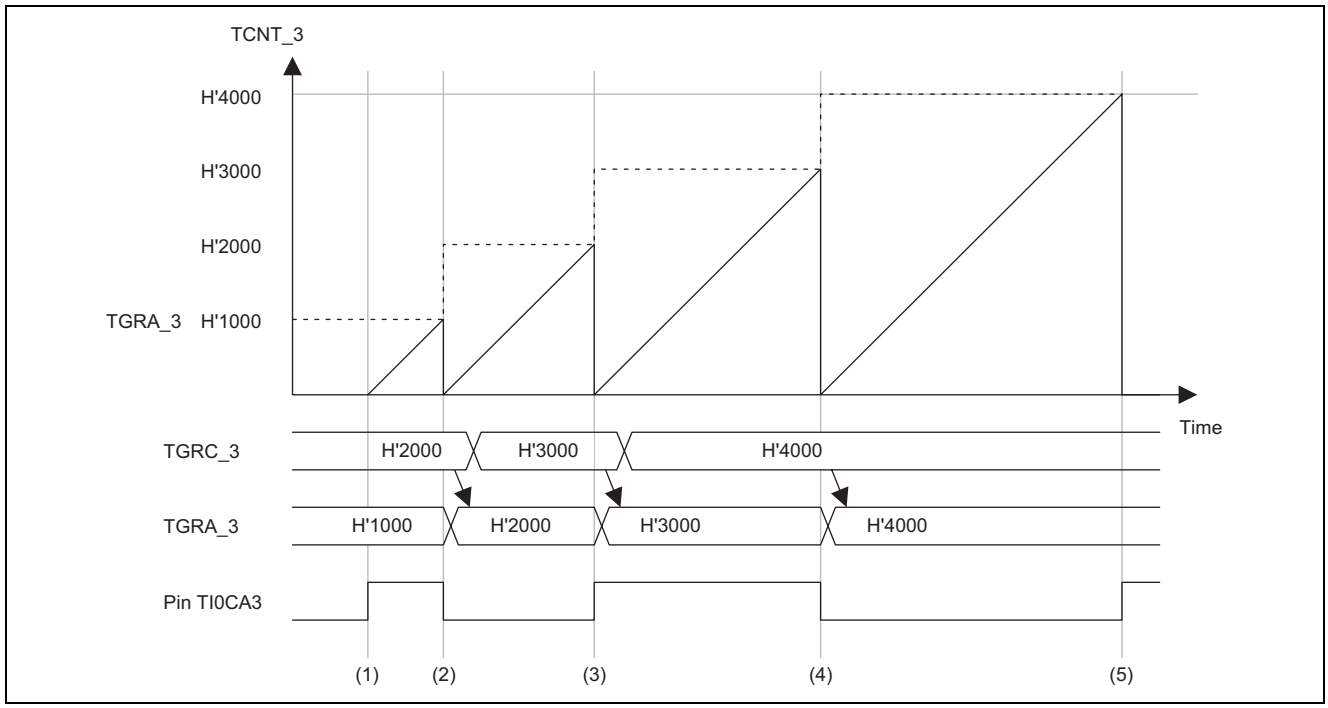


Figure 3 Illustration of Pulse-Output Operation in This Sample Task

Table 2 Description of Processing

	Hardware Processing	Software Processing
(1)	Power-on reset	Initial setting*
(2)	TGRA_3 compare-match generation a. TGFA = 1 in TSR_3. b. Toggle the compare-match output (to 0) for TGRA_3. c. Transfer the value in TGRC_3 (buffer register) to TGRA_3 (timer general register).	TGI3A interrupt a. Set the value in TGRC_3 (buffer register) for transfer to TGRA_3. b. Clear TGFA to 0 in TSR_3.
(3)	TGRA_3 compare-match generation a. TGFA = 1 in TSR_3. b. Toggle the compare-match output (to 1) for TGRA_3. c. Transfer the value in TGRC_3 (buffer register) to TGRA_3 (timer general register).	TGI3A interrupt a. Set the value in TGRC_3 (buffer register) for transfer to TGRA_3. b. Clear TGFA to 0 in TSR_3.
(4)	TGRA_3 compare-match generation a. TGFA = 1 in TSR_3. b. Toggle the compare-match output (to 0) for TGRA_3. c. Transfer the value in TGRC_3 (buffer register) to TGRA_3 (timer general register).	TGI3A interrupt a. Clear TGFA to 0 in TSR_3.
(5)	TGRA_3 compare-match generation a. TGFA = 1 in TSR_3. b. Toggle the compare-match output (to 1) for TGRA_3. c. Transfer the value in TGRC_3 (buffer register) to TGRA_3 (timer general register).	TGI3A interrupt a. Disable output on pin TIOCA3. b. Disable the TGI3A interrupt. c. Clear TGFA to 0 in TSR_3.

Notes *: Initial settings

a. Set the input clock for TCNT_3 to Pϕ.
b. Set compare match with TGRA_3 as the trigger for clearing of TCNT_3.
c. Set the initial output on pin TIOCA3 to 1, and select compare-match-driven toggling of the pin.
d. Enable the TGI3A interrupt.
e. Store the initial values in TGRA_3 and TGRC_3.
f. Start counter operation.

5. Description of Software

5.1 Operating Environment

Table 3 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.01.01
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler, Ver. 6.01.02 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	C	Area for constants
H'FF2000	B	Non-initialized data area (RAM area)

Table 5 Vector Table for Interrupt Exception Processing

Exception Processing Source		Vector No.	Vector address	Function to interrupt destination
Reset		0	H'000000	init
TPU_3	TGI3A	101	H'000194	tgi3a_int

5.2 List of Functions

Functions of this sample application are listed in table 6. The hierarchical structure of calls is shown in figure 4.

Table 6 List of Functions

Function Name	Function
init	Initialization routine Sets the CCR and configures the clocks, releases the required modules from the module stop mode, and calls the main function.
main	Main routine Makes settings for buffered operation of an output–compare function of the TPU to toggle the output on TIOCA3.
tgi3a_int	TGI3A interrupt-processing routine Sets values in TGRC_3 (buffer register) and clears the flag for the TGI3A interrupt.

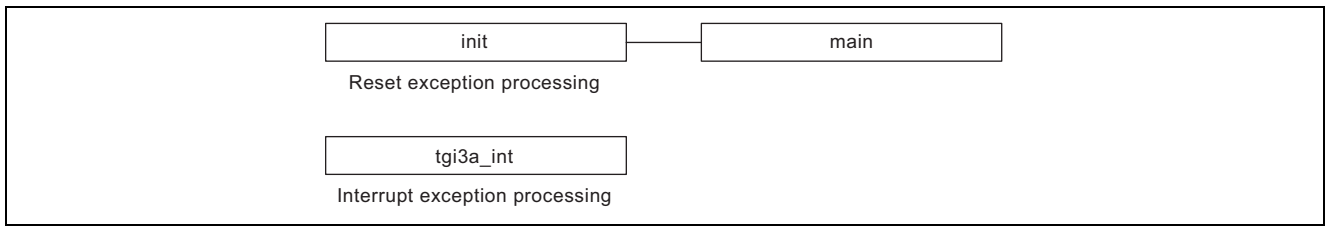


Figure 4 Hierarchical Structure

5.3 RAM Usage

Table 7 RAM Usage

Type	Variable Name	Description	Used in
unsigned char	cnt	Counter	main, tgi3a_int

5.4 Constant

Table 8 Constant

Type	Variable Name	Setting	Description	Used in
unsigned char	output[4]	H'1000, H'2000, H'3000, H'4000	Settings for TGRA_3	main, tgi3a_int

5.5 Description of Functions

5.5.1 init Function

1. Functional overview
   Initialization routine. (Releases the required modules from module stop mode, configures the clocks, and calls the main function.)
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   Usage of internal registers in this function of the sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. The latching is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0; see table 9). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latching is released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: Determined by the settings on pins MD3 to MD0.

Table 9 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System Clock Control Register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock
8	ICK0	1	R/W	provided to the CPU, DMAC, and DTC. 001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB and MSTPCRC control module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode, while clearing the bit to 0 releases the module from module stop mode.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current drawn by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: Disables all-module-clock-stop mode. 1: Enables all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

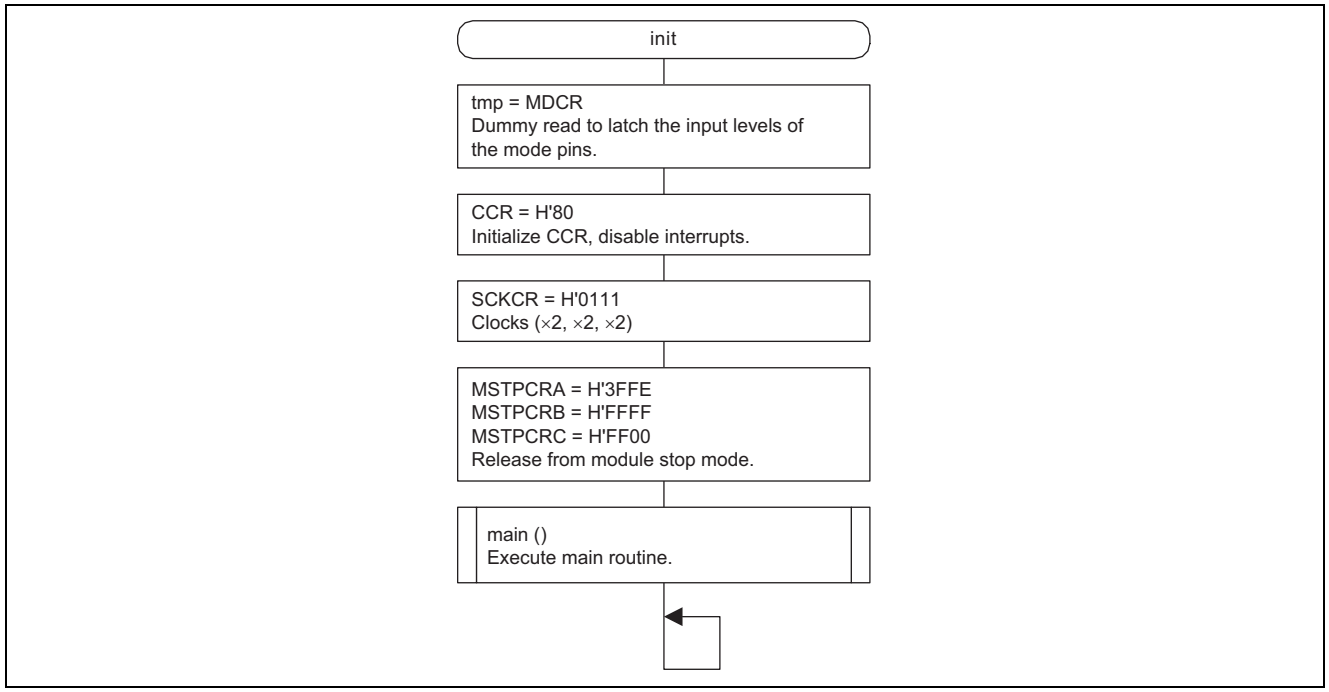
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus Interface 1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus Interface 0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timers (TMR_4 and TMR_5)
12	MSTPC12	1	R/W	8-bit timers (TMR_6 and TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy checker
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart



5.5.2 main Function

1. Functional overview
   For an output–compare function of the TPU, the main routine selects buffered operation and toggling of the TIOCA3 pin.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   Usage of internal registers in this function of the sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Description
5	CST5	0	R/W	Counter start 5 to 0
4	CST4	0	R/W	Selects operation or stopping of TCNT.
3	CST3	1	R/W	0: Stops counting by TCNT_5 to TCNT_0.
2	CST2	0	R/W	1: Counting by TCNT_5 to TCNT_0 proceeds.
1	CST1	0	R/W	
0	CST0	0	R/W	

- Timer control register_3 (TCR_3) Number of bits: 8 Address: H'FFFEC1

Bit	Bit Name	Setting	R/W	Description
7	CCLR2	0	R/W	Counter clear 2 to 0
6	CCLR1	0	R/W	Select the trigger for clearing of counter TCNT_3.
5	CCLR0	1	R/W	001: TCNT_3 cleared on compare match of/input capture in TGRA_3.
4	CKEG1	0	R/W	Clock edge 1 and 0
3	CKEG0	0	R/W	Select the input clock edge. 00: Counts on falling edges.
2	TPSC2	0	R/W	Timer prescaler 2 to 0
1	TPSC1	0	R/W	Select the counter clock for TCNT_3.
0	TPSC0	0	R/W	000: Counts on of the internal clock Pϕ/1.

- Timer mode register_3 (TMDR_3) Number of bits: 8 Address: H'FFFFF1

Bit	Bit Name	Setting	R/W	Description
4	BFA	1	R/W	Buffer Operation A 0: Normal operation of TGRA 1: Buffering operation of TGRA and TGRC
3	MD3	0	R/W	Mode 3 to 0
2	MD2	0	R/W	Set the timer operating mode.
1	MD1	0	R/W	0000: Normal operation
0	MD0	0	R/W	

- Timer I/O control register H_3 (TIORH_3) Number of bits: 8 Address: H'FFFFF2

Bit	Bit Name	Setting	R/W	Description
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	1	R/W	Specify the function of TGRA_3.
1	IOA1	1	R/W	0111: TGRA_3 functions as an output–compare register.
0	IOA0	1	R/W	The output on pin TIOCA3 is initially one, and is toggled on each instance of a compare-match.

- Timer interrupt enable register_3 (TIER_3) Number of bits: 8 Address: H'FFFFF4

Bit	Bit Name	Setting	R/W	Description
0	TGIEA	1	R/W	TGR Interrupt Enable A Enables or disables the generation of interrupt requests (TGIA) when the TGFA bit of TSR is set to 1. 0: Disables issuing of interrupt requests (TGIA) by the TGFA bit. 1: Enables issuing of interrupt requests (TGIA) by the TGFA bit.

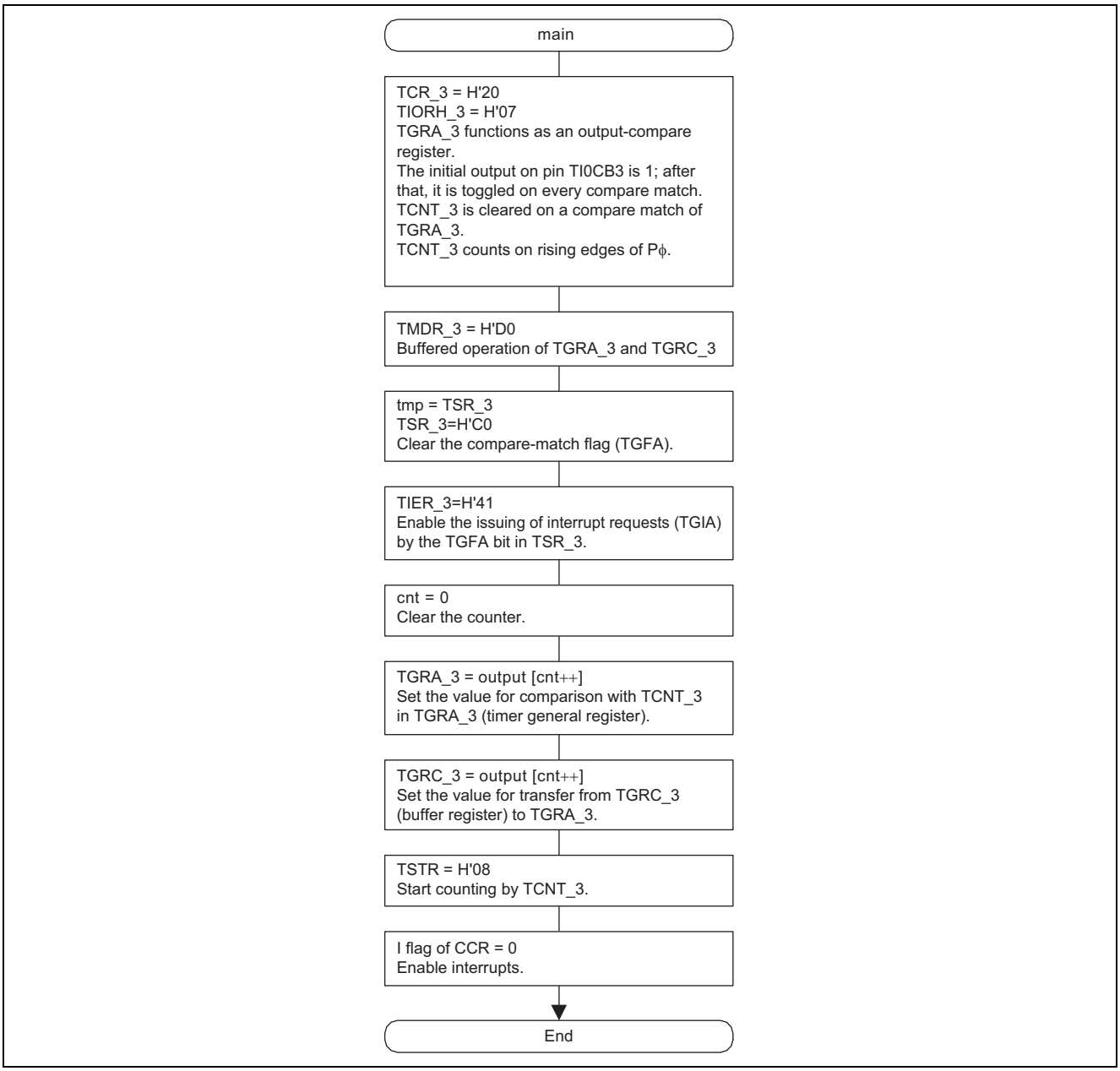
- Timer status register_3 (TSR_3) Number of bits: 8 Address: H'FFFFF5

Bit	Bit Name	Setting	R/W	Description
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A When TGRA_3 is functioning as an output-compare register, the following conditions apply. [Setting condition] When TCNT = TGRA [Clearing condition] Writing of 0 in TGFA after having read TGFA to 1

Note: * Only 0 can be written here, to clear the flag.

- Timer general register A_3 (TGRA_3) Number of bits: 16 Address: H'FFFFF8
  Function: TGRA_3 is used as an output–compare register in this application
  Setting value: output[cnt++]
- Timer general register C_3 (TGRC_3) Number of bits: 16 Address: H'FFFFFC
  Function: TGRC_3 is used as a buffer register for TGRA_3 in this application
  Setting value: output[cnt++]

5. Flowchart


main
TCR_3 = H'20
TIORH_3 = H'07
TGRA_3 functions as an output-compare register.
The initial output on pin TI0CB3 is 1; after that, it is toggled on every compare match.
TCNT_3 is cleared on a compare match of TGRA_3.
TCNT_3 counts on rising edges of Pϕ.
TMDR_3 = H'D0
Buffered operation of TGRA_3 and TGRC_3
tmp = TSR_3
TSR_3=H'C0
Clear the compare-match flag (TGFA).
TIER_3=H'41
Enable the issuing of interrupt requests (TGIA) by the TGFA bit in TSR_3.
cnt = 0
Clear the counter.
TGRA_3 = output [cnt++]
Set the value for comparison with TCNT_3 in TGRA_3 (timer general register).
TGRC_3 = output [cnt++]
Set the value for transfer from TGRC_3 (buffer register) to TGRA_3.
TSTR = H'08
Start counting by TCNT_3.
I flag of CCR = 0
Enable interrupts.
End

5.5.3 tgi3a_int Function

1. Functional overview
   Interrupt processing for TGI3A. (Sets values in TGRC_3 (the buffer register) and clears the flag for the TGI3A interrupt.)
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   Usage of internal registers in this function of the sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Timer I/O control register H_3 (TIORH_3) Number of bits: 8 Address: H'FFFFF2

Bit	Bit Name	Setting	R/W	Description
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	Specify the function of TGRA_3.
1	IOA1	0	R/W	0000: TGRA_3 functions as an output–compare register.
0	IOA0	0	R/W	Output on pin TIOCA3 is disabled.

- Timer interrupt enable register_3 (TIER_3) Number of bits: 8 Address: H'FFFFF4

Bit	Bit Name	Setting	R/W	Description
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables or disables the generation of interrupt requests (TGIA) when the TGFA bit of TSR is set to 1. 0: Disables issuing of interrupt requests (TGIA) by the TGFA bit. 1: Enables issuing of interrupt requests (TGIA) by the TGFA bit.

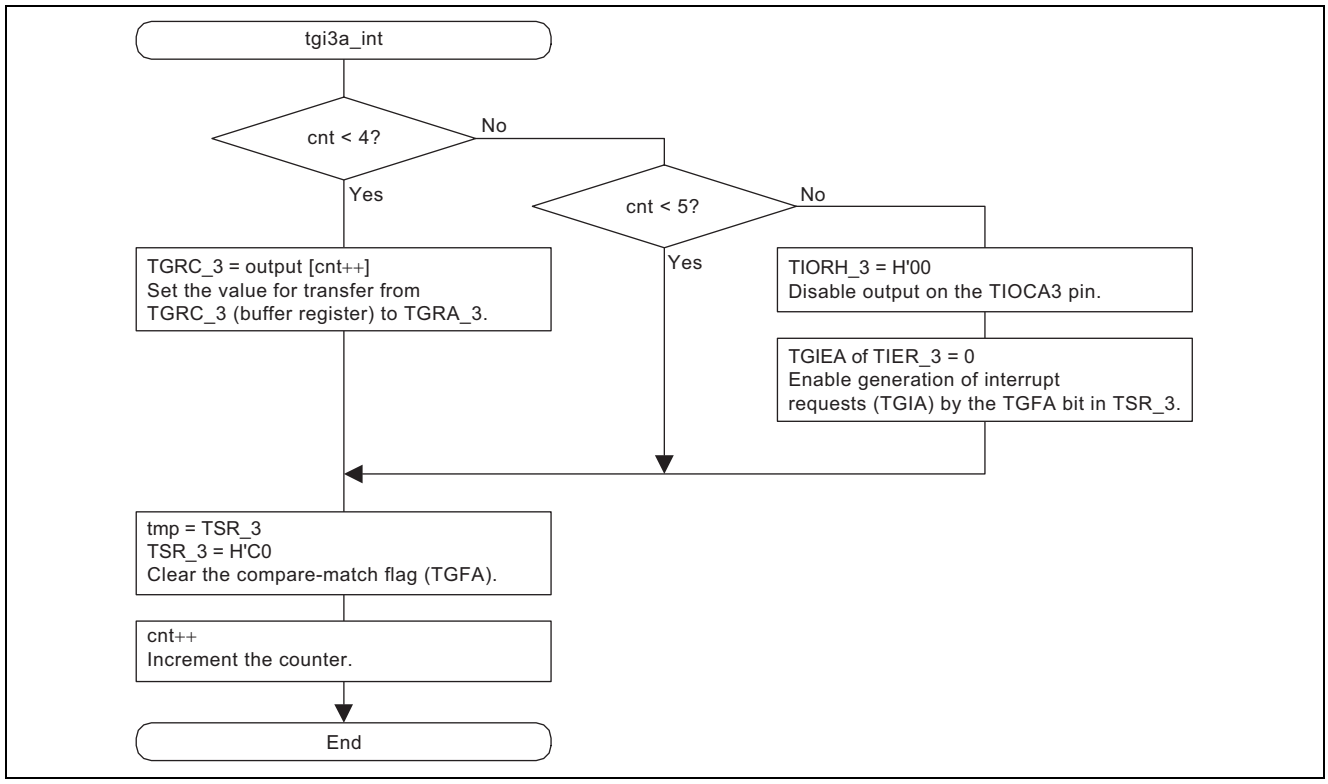
- Timer status register_3 (TSR_3) Number of bits: 8 Address: H'FFFFF5

Bit	Bit Name	Setting	R/W	Description
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A When TGRA_3 is functioning as an output-compare register, the following conditions apply. [Setting condition] When TCNT = TGRA [Clearing condition] Writing of 0 in TGFA after having read TGFA to 1

Note: * Only 0 can be written here, to clear the flag.

- Timer general register C_3 (TGRC_3) Number of bits: 16 Address: H'FFFFFC
  Function: TGRC_3 is used as a buffer register for TGRA_3 in this application
  Setting value: output[cnt++]

5. Flowchart


tgi3a_int
cnt < 4?
No
Yes
cnt < 5?
No
Yes
TGRC_3 = output [cnt++]
Set the value for transfer from
TGRC_3 (buffer register) to TGRA_3.
TIORH_3 = H'00
Disable output on the TIOCA3 pin.
TGIEA of TIER_3 = 0
Enable generation of interrupt
requests (TGIA) by the TGFA bit in TSR_3.
tmp = TSR_3
TSR_3 = H'C0
Clear the compare-match flag (TGFA).
cnt++
Increment the counter.
End

6. Documents for Reference (Note)

- Hardware manual
  H8SX/1653 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Technical News/Technical Update
  The most up-to-date information is available on the Renesas Technology Website.

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
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