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Renesas Electronics Corporation

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H8/300H Tiny Series

Buffer Operation of Input Capture Function

Introduction

The buffer operation of timer W's input capture function is used to measure the high-level width and low-level width of a pulse.

Target Device

H8/3664

Contents

1. Specifications

1. The buffer function of timer W's input capture function is used to measure the high-level width and low-level width of the pulses input to the input capture A pin (FTIOA).
2. The timer counter (TCNT) measures the time from the rising edge to falling edge of the pulse to measure the high-level width of the pulse.
3. The timer counter (TCNT) measures the time from the falling edge to rising edge of the pulse to measure the low-level width of the pulse.
4. The maximum width of a pulse that can be measured is 32.768 ms with the accuracy is ±0.5 µs.

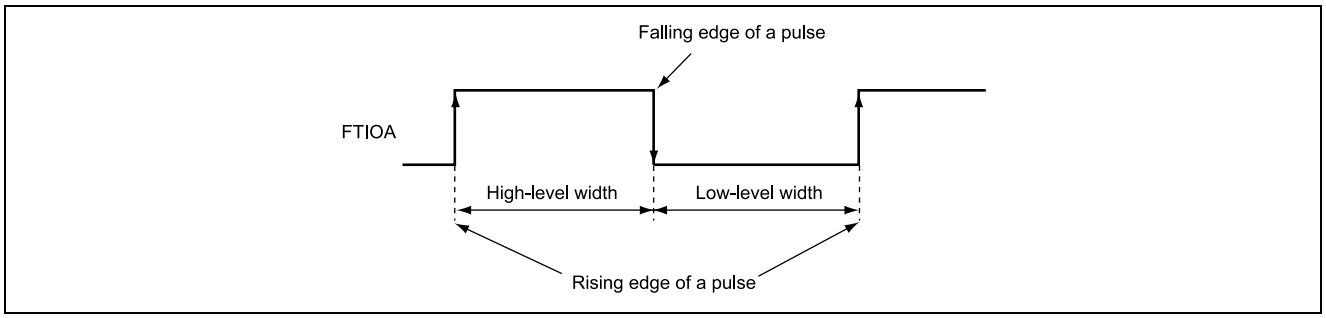


Figure 1.1 Measurement of Input Pulse Width

2. Description of Functions

1. In this sample task, the high-level width and low-level width of the pulse input to the input capture input pin A (FTIOA) is measured by using the buffer operation of timer W input capture function.
   Figure 2.1 is a block diagram of the input capture function of timer W. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer mode register W (TMRW) controls starting and stopping of the TCNT.
- Timer control register W (TCRW) specifies the TCNT clearing method and a TCNT input clock. In this sample task, input clock is specified as ϕ/8.
- Timer interrupt enable register W (TIERW) enables or disables various interrupt requests. In this sample task, interrupts generated by the OVF and IMFA flags are enabled and other interrupts are disabled.
- Timer status register W (TSRW) indicates the timer W statuses. In this task example, the overflow flag (OVF) is set to 1 when the TCNT overflows and the input-capture/compare-match flag A (IMFA) is set to 1 when the GRA input capture occurs.
- Timer I/O control register 0 (TIOR0) controls the GRA and GRB. In this sample task, the GRA is used as an input capture register and the TCNT value is transferred to the GRA at the rising and falling edges on the FTIOA pin.
- Timer I/O control register 1 (TIOR1) controls the GRC and GRD. In this sample task, the GRC is used as an input capture register and the TCNT value is transferred to the GRC at the rising and falling edges on the FTIOA pin.
- The timer counter (TCNT) is a 16-bit readable/writable up-counter that is incremented by internal or external clock input. In this sample task, the TCNT is incremented on the rising edge of ϕ/8.
- General register A (GRA) is a 16-bit readable/writable register. In this sample task, the GRA is used as an input capture register and the TCNT value is transferred to the GRA at the rising and falling edges on the FTIOA pin.
- General register C (GRC) is a 16-bit readable/writable register. In this sample task, the GRC is used as a buffer register for GRA and the GRA value is transferred to the GRC at the rising and falling edges on the FTIOA pin.
- The input-capture/output-compare A pin (FTIOA) is specified as an input capture input pin. The TCNT value is transferred to the GRA at the rising and falling edges on the FTIOA pin.

Input pulse's cycle
= (TCNT value stored in plhigh or pllow) × (TCNT input clock cycle)
= (TCNT value stored in plhigh or pllow) × (1/ (ϕ/PSS))
= (TCNT value stored in plhigh or pllow) × (1/ (16 MHz/8))
= (TCNT value stored in plhigh or pllow) × 0.5 μs

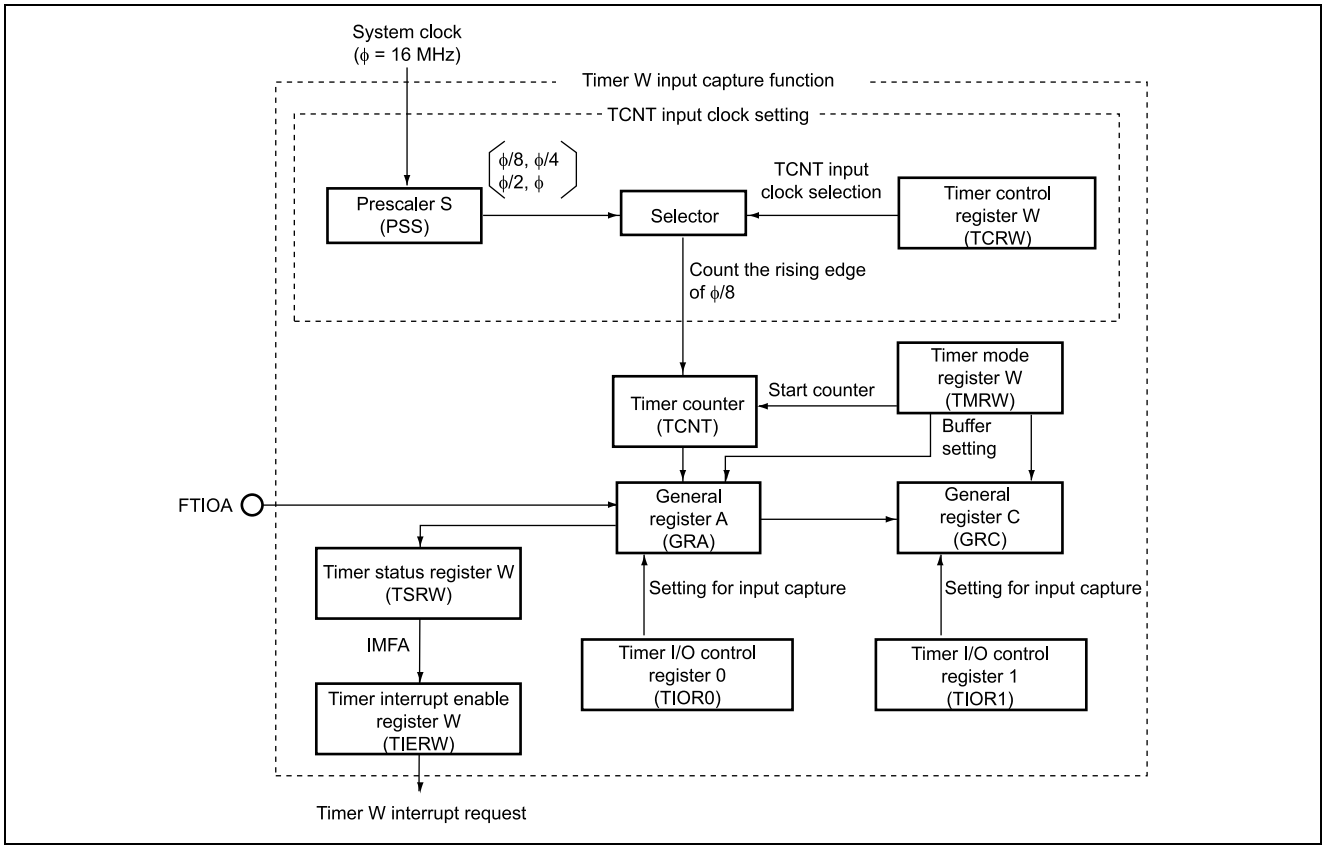


Figure 2.1 Timer W Block Diagram

Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so that the high-level and low-level widths of the pulse can be measured.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TMRW	Controls the TCNT start and stop and sets the GRC as the buffer register for GRA.
TCRW	Sets the input clock of TCNT.
TIERW	Enables the TCNT overflow and GRA input capture interrupt requests.
TSRW	Controls the flags for TNCT overflow and GRA input capture.
TIOR0	Specifies the GRA as an input capture register.
TIOR1	Specifies the GRC as an input capture register.
TCNT	16-bit up-counter incremented on the rising edge of ϕ/8
GRA	Stores the TCNT value on detecting the rising and falling edges on the FTIOA pin.
GRC	Stores the GRA value on detecting the rising and falling edges on the FTIOA pin.
FTIOA pin	Pulse input pin

3. Description of Operation

Figure 3.1 illustrates the operation of this sample task. The hardware and software processing are applied as shown in figure 3.1 to measure the high-level and low-level widths of the input pulse.

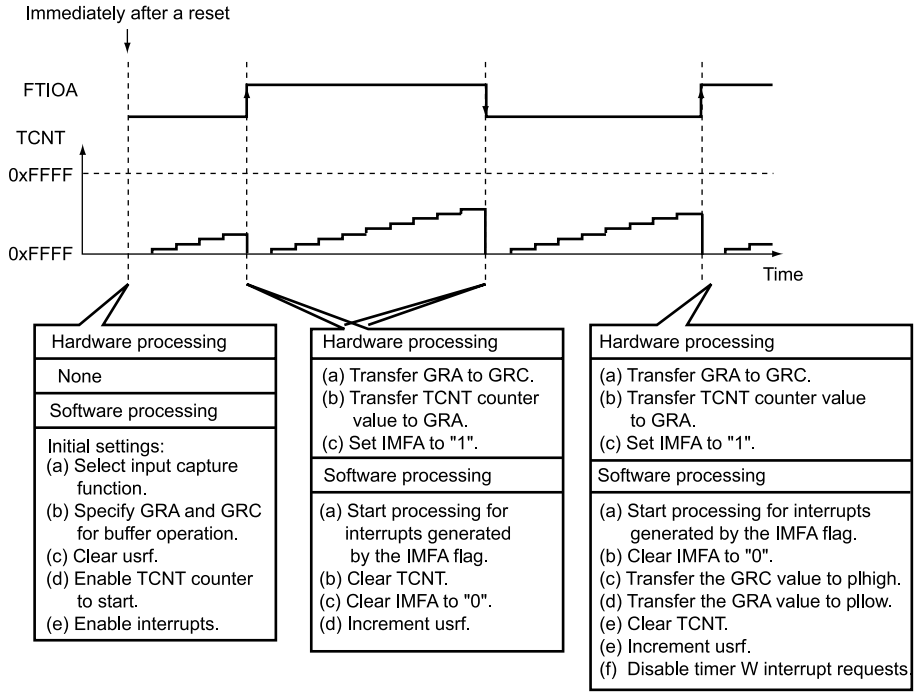


Figure 3.1 Description of Operation

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the module used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Specifies the timer W input capture function and buffer operation, starts the counter, and specifies interrupts.
Pulse width measurement end	twint	Performs timer W interrupt processing, clears the OVF and IMFA flags, and stores high-level and low-level widths of the pulse in RAM.

4.2 Description of Arguments

This sample task uses no arguments.

4.3 Description of Internal Registers

The internal registers used in this sample task are described below.

- TMRW Timer mode register W Address: 0xFF80

Bit	Bit Name	Setting	Function
7	CTS	0	Counter start CTS = 0: TCNT counter operation is stopped. CTS = 1: TCNT counter operation has been started.
4	BUFEA	1	Buffer operation A BUFEA = 0: GRC functions as an input-capture/output-compare register. BUFEA = 1: GRC functions as a buffer register for GRA.

- TCRW Timer control register W Address: 0xFF81

Bit	Bit Name	Setting	Function
6	CKS2	CKS2 = 0	Clock select 2 to 0
5	CKS1	CKS1 = 1	CKS2 = 0, CKS1 = 1, CKS0 = 1: TCNT is incremented by ϕ/8
4	CKS0	CKS0 = 1	

- TIERW Timer interrupt enable register W Address: 0xFF82

Bit	Bit Name	Setting	Function
7	OVIE	1	Timer overflow interrupt enable OVIE = 0: Disables interrupt requests generated by the OVF flag of TSRW. OVIE = 1: Enables interrupt requests generated by the OVF flag of TSRW.
0	IMIEA	1	Output compare interrupt A enable IMIEA = 0: Disables IMFA interrupt requests. IMIEA = 1: Enables IMFA interrupt requests.

- TSRW Timer status register W Address: 0xFF83

Bit	Bit Name	Setting	Function
7	OVF	0	Timer overflow OVF = 0: Indicates that TCNT overflow has not occurred. OVF = 1: Indicates that TCNT overflow has occurred.
0	IMFA	1	Output compare flag A When the GRA functions as an input capture register, IMFA indicates that the TCNT value has been transferred to the GRA based on an input capture signal. IMFA = 0: Indicates that the TCNT value has not been transferred to GRA. IMFA = 1: Indicates that the TCNT value has been transferred to GRA.

- TIOR0 Timer I/O control register 0 Address: 0xFF84

Bit	Bit Name	Setting	Function
2	IOA2	IOA2 = 1	IO control A 2 to 0
1	IOA1	IOA1 = 1	IOA2 = 1, IOA1 = 1, IOA0 = X:
0	IOA0	IOA0 = X	The GRA is used as an input capture register and the TCNT value is transferred to the GRA at the rising and falling edges on the FTIOA pin. (X: don't care)

- TIOR1 Timer I/O control register 1 Address: 0xFF85

Bit	Bit Name	Setting	Function
2	IOC2	IOC2 = 1	IO control C 2 to 0
1	IOC1	IOC1 = 1	IOC2 = 1, IOC1 = 1, IOC0 = X:
0	IOC0	IOC0 =	The GRC is used as an input capture register and the TCNT value is transferred to the GRC at the rising and falling edges on the FTIOA pin. (X: don't care)

- TCNT Timer counter Address: 0xFF86
  Function: 16-bit up-counter incremented at the rising edge of $\phi/8$.
  Setting: 0x0000

- GRA General register A Address: 0xFF88
  Function: During input capture operation, the TCNT value is transferred to the GRA at the rising and falling edges on the FTIOA pin.
  Setting: —

- GRC General register C Address: 0xFF8C
  Function: When the GRC functions as the buffer register for the GRA in input capture operation, the GRA value is transferred to the GRC at the rising and falling edges on the FTIOA pin.
  Setting —

4.4 Description of RAM

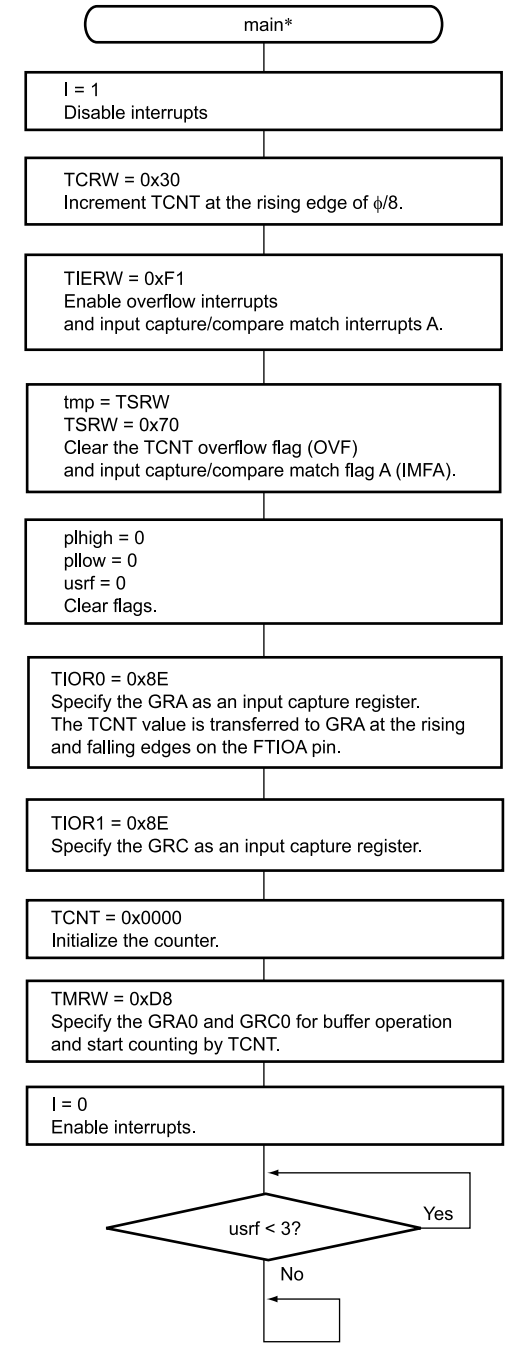
Table 4.2 describes the RAM used in this sample task.

Table 4.2 Description of RAM

Label Name	Function	Size	Used in
plhigh	Pulse high-level width measurement result	2 bytes	Main routine Pulse width measurement end
pllow	Pulse low-level width measurement result	2 bytes	Main routine Pulse width measurement end
usrf	Timer W interrupt status indicator usfr = 0: No interrupt has occurred. usfr = 1: Pulse width measurement has started. usfr = 2: Pulse high-level width measurement has completed. usfr = 3: Pulse low-level width measurement has completed/ Pulse width measurement has completed normally.	1 byte	Main routine Pulse width measurement end

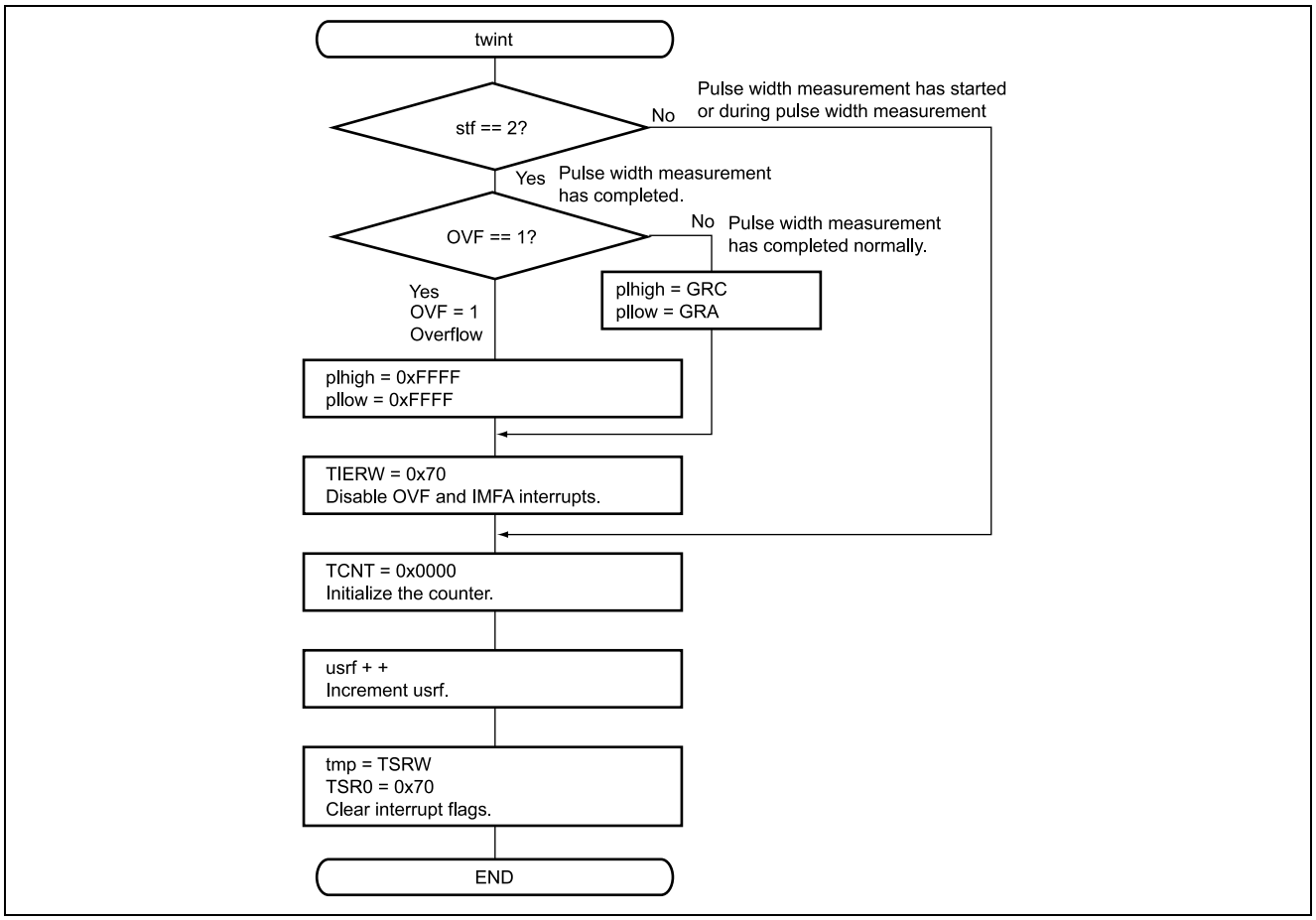
5. Flowchart

1. Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

2. Pulse width measurement end



6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3664-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'Pulse Period Measurement by Input Caputure Function'                                                              */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer W Input Caputure                                                                                           */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TMRW           *(volatile unsigned char *)0xFF80                  /* Timer mode register W                */
#define        TCRW           *(volatile unsigned char *)0xFF81                  /* Timer control register W             */
#define        TIERW          *(volatile unsigned char *)0xFF82                  /* Timer interrupt enable register W    */
#define        TIERW_BIT      (*(struct BIT *)0xFF82)                            /* Timer interrupt enable register W    */
#define        OVIE           TIERW_BIT.b7                                       /* Timer Overflow Interrupt Enable      */
#define        IMIEA          TIERW_BIT.b0                                       /* Input Capture/Compare Match          */
                                                                                 /* Interrupt Enable A                   */
#define        TSRW           *(volatile unsigned char *)0xFF83                  /* Timer Status Register W              */
#define        TSRW_BIT       (*(struct BIT *)0xFF83)                            /* Timer Status Register W              */
#define        OVF            TSRW_BIT.b7                                        /* Timer Over flow                      */
#define        IMFA           TSRW_BIT.b0                                        /* Input Capture/Compare Match FlagA    */
#define        TIOR0          *(volatile unsigned char *)0xFF84                  /* Timer I/O control register 0         */
#define        TIOR1          *(volatile unsigned char *)0xFF85                  /* Timer I/O control register 1         */
#define        TCNT           *(volatile unsigned short *)0xFF86                 /* Timer counter                        */
#define        GRA            *(volatile unsigned short *)0xFF88                 /* General register A                   */
#define        GRC            *(volatile unsigned short *)0xFF8C                 /* General register C                   */

#pragma interrupt   (twint)
```

```
/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                          /* SP Set                                           */
void main ( void );
void twint ( void );

/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
volatile unsigned short plhigh;                                     /* Pulse time data                                  */
volatile unsigned short pllow;                                      /* Pulse time data                                  */
volatile unsigned char  usrf;                                       /* User flag                                        */

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                              /* VECTOR SECTOIN SET                               */
void (*const VEC_TBL1[])(void) = {                                  /* 0x00 - 0x0f                                      */
     INIT                                                           /* 00 Reset                                         */
};
#pragma section     V2                                              /* VECTOR SECTOIN SET                               */
void (*const VEC_TBL2[])(void) = {
     twint                                                          /* 2A Timer W Interrupt                             */
};

#pragma section                                                     /* P                                                */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     unsigned char tmp;

     set_imask_ccr(1);                                              /* Interrupt Disable                                */

     TCRW = 0x30;                                                   /* phi/8 Clock count                                */
     TIERW = 0xF1;                                                  /* OVF,IMFA Interrupt Enable                        */
     tmp = TSRW;
     TSRW = 0x70;                                                   /* Interrupt Flag Clear                             */
     plhigh = 0;                                                    /* Ram clear                                        */
     pllow = 0;                                                     /* Ram clear                                        */
     usrf = 0;                                                      /* Flag clear                                       */
     TIOR0 = 0x8E;                                                  /* Input capture to GRA at both                     */
                                                                    /* rising and falling edges                         */
     TIOR1 = 0x8E;                                                  /* Input capture to GRC                             */
     TCNT = 0x0000;                                                 /* Clear TCNT                                       */
     TMRW = 0xD8;                                                   /* TCNT count start                                 */

     set_imask_ccr(0);                                              /* Interrupt Enable                                 */

     while(usrf < 3);

     while(1);
}
```

```
/************************************************************************************************************************/
/*   Timer W Interrupt                                                                                                  */
/************************************************************************************************************************/
void twint ( void )
{
     unsigned char tmp;

     if(usrf == 2){
          if(OVF == 1){
               plhigh = 0xFFFF;                                   /* Overflow                          */
               pllow = 0xFFFF;
          }
          else{
               plhigh = GRC;                                      /* Ram copy to GRC0                  */
               pllow = GRA;                                       /* Ram copy to GRA0                  */
          }
          TIERW = 0x70;                                           /* OVF,IMFA Interrupt Disable        */
     }

     TCNT = 0x0000;                                               /* Set TCNT                          */
     usrf++;                                                      /* User flag increment               */
     tmp = TSRW;
     TSRW = 0x70;                                                 /* Interrupt Flag Clear              */
}
```

Link address specifications

Section Name	Address
CV1	0x0000
CV2	0x002A
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.24.03	—	First edition issued

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