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R8C/2L Group

Brushless DC Motor Control

1. Abstract

This application note describes how the R8C/2L is used to control a brushless DC (BLDC) motor.

2. Introduction

The application example described in this document is applied to the following:

MCU: R8C/2L Group

This program can be used with other R8C Family MCUs which have the same special function registers (SFR) as the R8C/2L Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

3. BLDC Motor Control Overview

BLDC motors are used today in many applications. A BLDC motor has two main components: a rotor made up of permanent magnets, and a stator with coils connected to the control electronics.

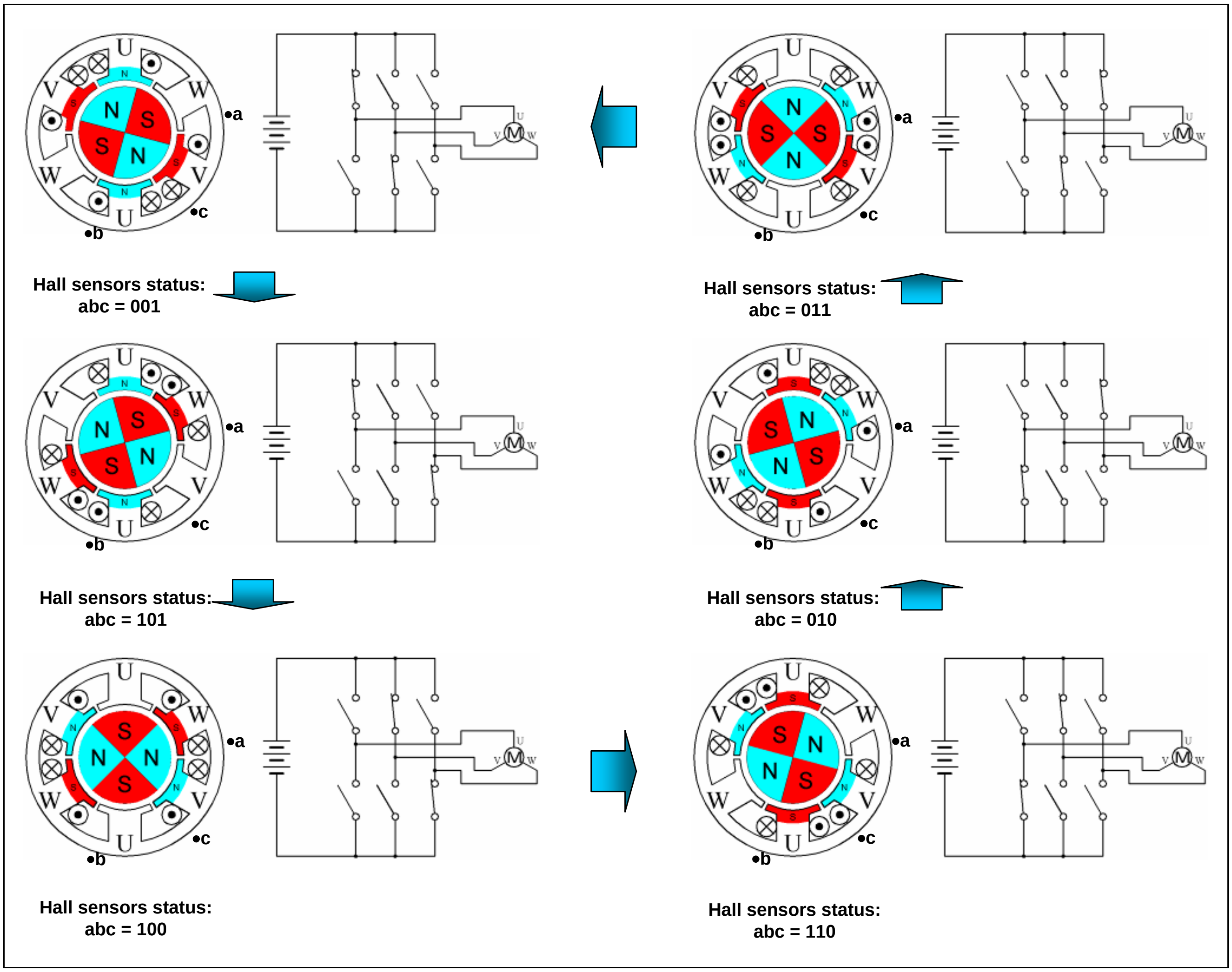


Figure 1. Six Step Commutation

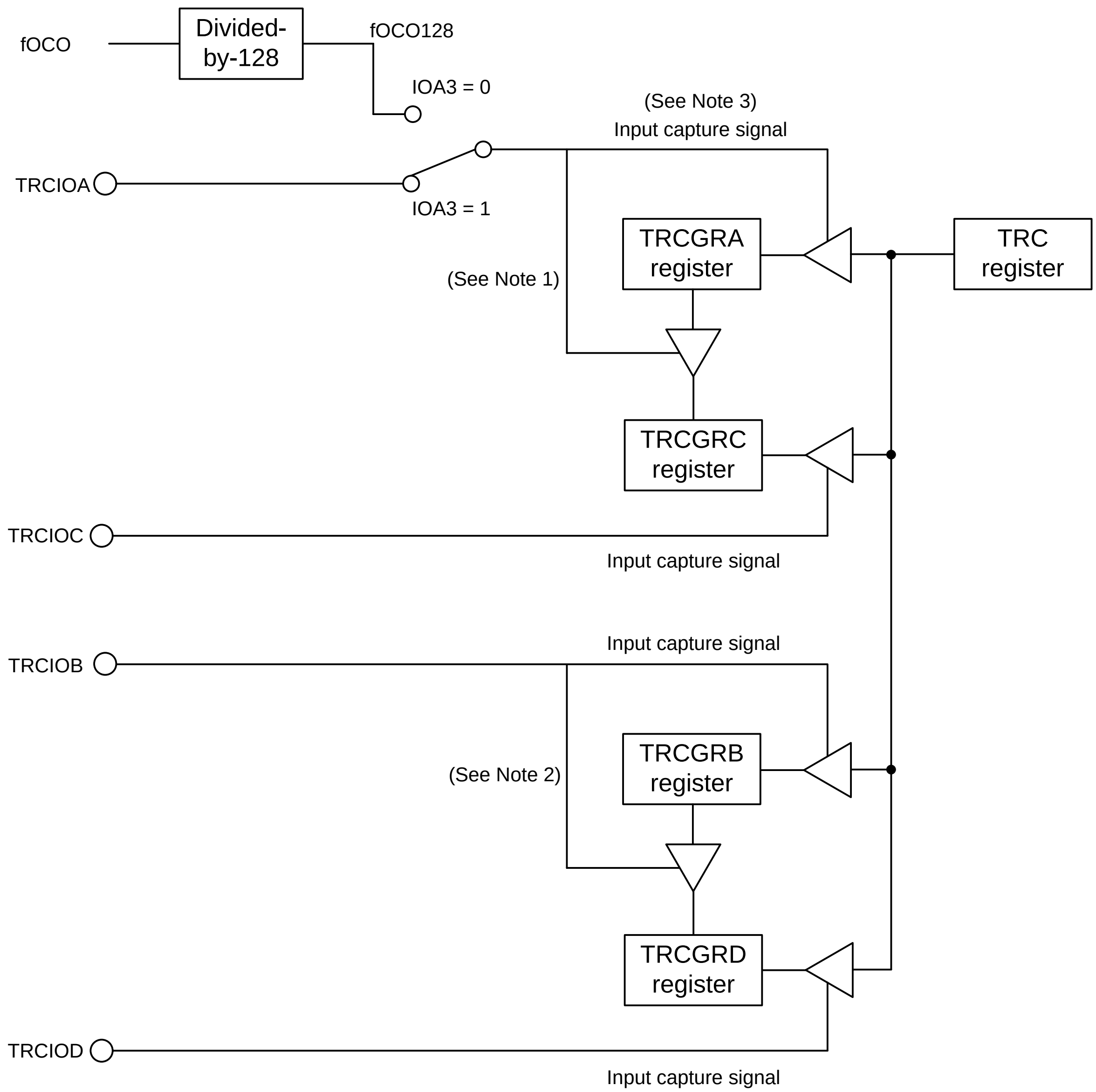
In this implementation, a six step commutation method which is illustrated in the figure above is used to steer a three-phase BLDC motor. The motor has two pole pairs and can rotate up to 8000 rpm at rated voltage of 15 V. Three Hall sensors (which are shown as ‘a’, ‘b’ and ‘c’ in Figure 1) located 60 degrees apart around the stator are used to obtain the rotor’s position. Depending on which magnetic field passes over each sensor, the output may be high or low. When the N pole passes over a sensor, its output is high. When the S pole passes over a sensor, its output is low.

The MCU plays an important role in this operation. The MCU should have three input ports, one for each Hall sensor, and six output pins, one for each switch driver. The MCU performs its task by executing interrupt based code and changing the state of the output pin. Hall sensor signals are fed into the MCU as external interrupts. With every interrupt signal, the MCU performs a state change: it turns off one switch and turns on another.

4. BLDC Motor Control Using R8C/2L

4.1 Timer RC Operation

In this implementation, the Timer RC's input capture function is used to monitor the state of the three Hall sensors. Three $\overline{INT}$ interrupts from the R8C/2L MCU can also be used to detect a change on these Hall sensors, but using the Timer RC's input capture function gives it a benefit when calculating the motor rotation speed.



IOA3: Bit in the TRCIOR0 register

NOTES:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)
3. The trigger input of the TRCGRA register can select the TRCIOA pin input or fOCO128 signal.

Figure 2. Input Capture Function Block Diagram

There are four I/O pins (TRCIOj (j = A, B, C, or D)) (depicted in Figure 2) that can be configured as the timer RC's input capture inputs, three of which are used in this application. Each rising or falling edge of the Hall sensor signal fed into the TRCIOj pin acts as a trigger for transferring the contents of the TRC register (counter) to the TRCGRj register, and also causes timer RC to generate an interrupt. In the interrupt service routine, a 3-bit Hall sensor value is read to determine the rotor's state on which a correct commutation sequence is generated to drive the windings of the BLDC motor. The value in the TRCGRj register is used for computing the motor rotation speed.

In this application, the timer RC digital filter function is used. When the digital filter is enabled, input to TRCIOj is sampled based on a rate specified by the user and only the signal qualified the filter condition can trigger an input capture. The digital filter can eliminate unwanted noise and spikes which can cause abnormal input capture triggering.

4.2 Timer RD Operation

In this implementation, timer RD is used to generate the required PWM waveform. Timer RD is a multi-purpose timer with dedicated PWM functions tailored for three-phase BLDC motor control. In this application, timer RD works in complementary PWM mode.

The table below lists the specification for timer RD in Complementary PWM Mode.

Table 1. Complementary PWM Mode Specification of Timer RD (1/2)

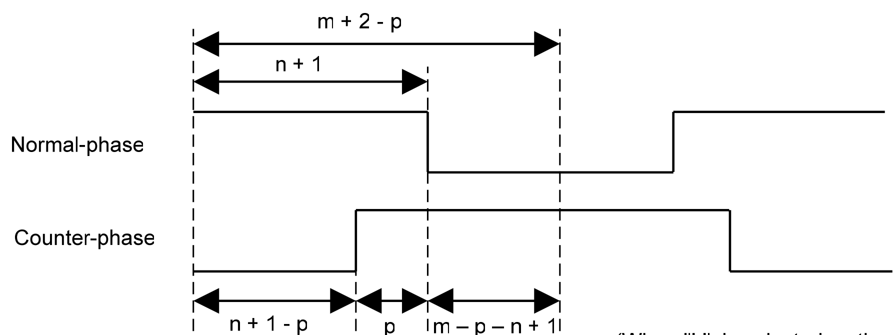
Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program) Set bits TCK2 to TCK0 in the TRDCR1 register to the same value (same count source) as bits TCK2 to TCK0 in the TRDCR0 register
Count operations	Increment or decrement Registers TRD0 and TRD1 are decremented with the compare match in registers TRD0 and TRDGRA0 during increment operation. The TRD1 register value is changed from 0000h to FFFFh during decrement operation, and registers TRD0 and TRD1 are incremented
PWM operations	PWM period: 1 / fk × (m + 2 - p) × 2 (Note) Dead time: p Active level width of normal-phase: 1 / fk × (m – n – p + 1) × 2 Active level width of counter-phase: 1 / fk × (n + 1 - p) × 2 fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output) p: Value set in the TRD0 register  (When "L" is selected as the active level)

Table 1. Complementary PWM mode specification of Timer RD (2/2)

Count start condition	1 (count starts) is written to bits TSTART0 and TSTART1 in the TRDSTR register
Count stop conditions	0 (count stops) is written to bits TSTART0 and TSTART1 in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1 (The PWM output pin holds output level before the count stops)
Interrupt request generation timing	• Compare match (content of the TRDi register matches content of the TRDGRji register) • The TRD1 register underflows
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every PWM period
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.
Select functions	• Pulse output forced cutoff signal input • The active level of normal-phase and counter-phase and initial output level selected individually • Transfer timing from the buffer register selected • A/D trigger generated

i = 0 or 1, j = either A, B, C, or D

Note: After a count starts, the PWM period is fixed.

Refer to Figure 3 and Figure 4 about complementary PWM mode. TRD0 and TRD1 are two dedicated 16-bit timers in timer RD. These two timers are incremented or decremented by a user defined clock (count) source which could be internal (f1, f2, f4, f8, f32, fOCO40M) or external (by inputting an external clock signal to the TRDCLK pin). The user decides the period (carrier frequency) required for the PWM by selecting a value and loading it in the TRDGRA0 register. The TRD0 value is compared to the TRDGRA0 value at each timer operation clock cycle. When there is a match, a new period is started.

The duty cycle is similarly controlled, by loading a value in the three duty cycle registers TRDGRB0, TRDGRA1, and TRDGRB1. The TRDi value is compared to the value in TRDGRB0, TRDGRA1 and TRDGRB1. If there is a match between the TRDi value and the value in one of the duty cycle registers, the corresponding duty cycle output is driven low or high as dictated by the selected PWM mode. The six outputs from the duty cycle compare compose three complementary output pairs where one output is high while the other is low, and vice versa. When driven as complementary outputs, dead time can be inserted between these two complementary waveforms. This dead time is hardware configured by loading a value in the TRD0 register.

As shown in Figure 5, each PWM output pin corresponds to a bit in the TRDOER1 register. These bits determine if the corresponding output pin is driven by a PWM signal (when set to “0”) or driven by the general purpose programmable I/O port (when set to “1”). This feature allows the user to have PWM signals available, but not driving, at all output stages of the pins. Depending on the value in the TRDOER1 register, the user can select which pin receives the PWM signal and which pin is driven active or inactive by programmable I/O ports. When controlling the BLDC motor sensored motor, it is necessary to excite two winding pairs depending on where the rotor is located and dictated by the value of the Hall sensors. In the timer RC input capture interrupt service routine, the Hall sensors are read and then the value of the sensors is used as an offset in a lookup table which corresponds to the value to be loaded in the P2 and TRDOER1 registers. Figure 7 shows how different values are loaded in the P2 and TRDOER1 registers depending on which state the rotor is in and thereby which windings need to be excited.

Another important feature of timer RD is the Pulse Output Forced Cutoff (depicted in Figure 5). The pulse output forced cutoff function has been designed specifically for overcurrent protection. If enabled, the TRDIOji output pins are set to the programmable I/O port after a low signal is applied to the $\overline{\text{INT0}}$ pin and waiting for 1 to 2 cycles of the timer RD operation clock. Set the pin status (high impedance, “L” or “H” output) to pulse output forced cutoff by registers P2 and PD2. In this implementation, PD2 is set to 0xFF and P2 is set to 0x00 in order to protect the motor.

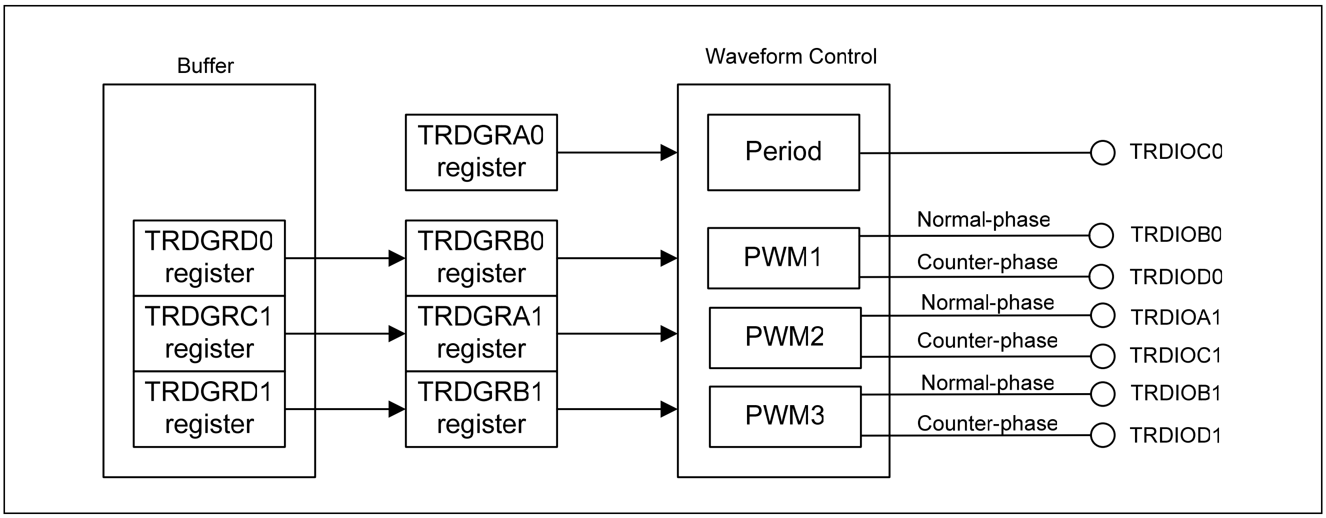


Figure 3. Complementary PWM Mode Block Diagram

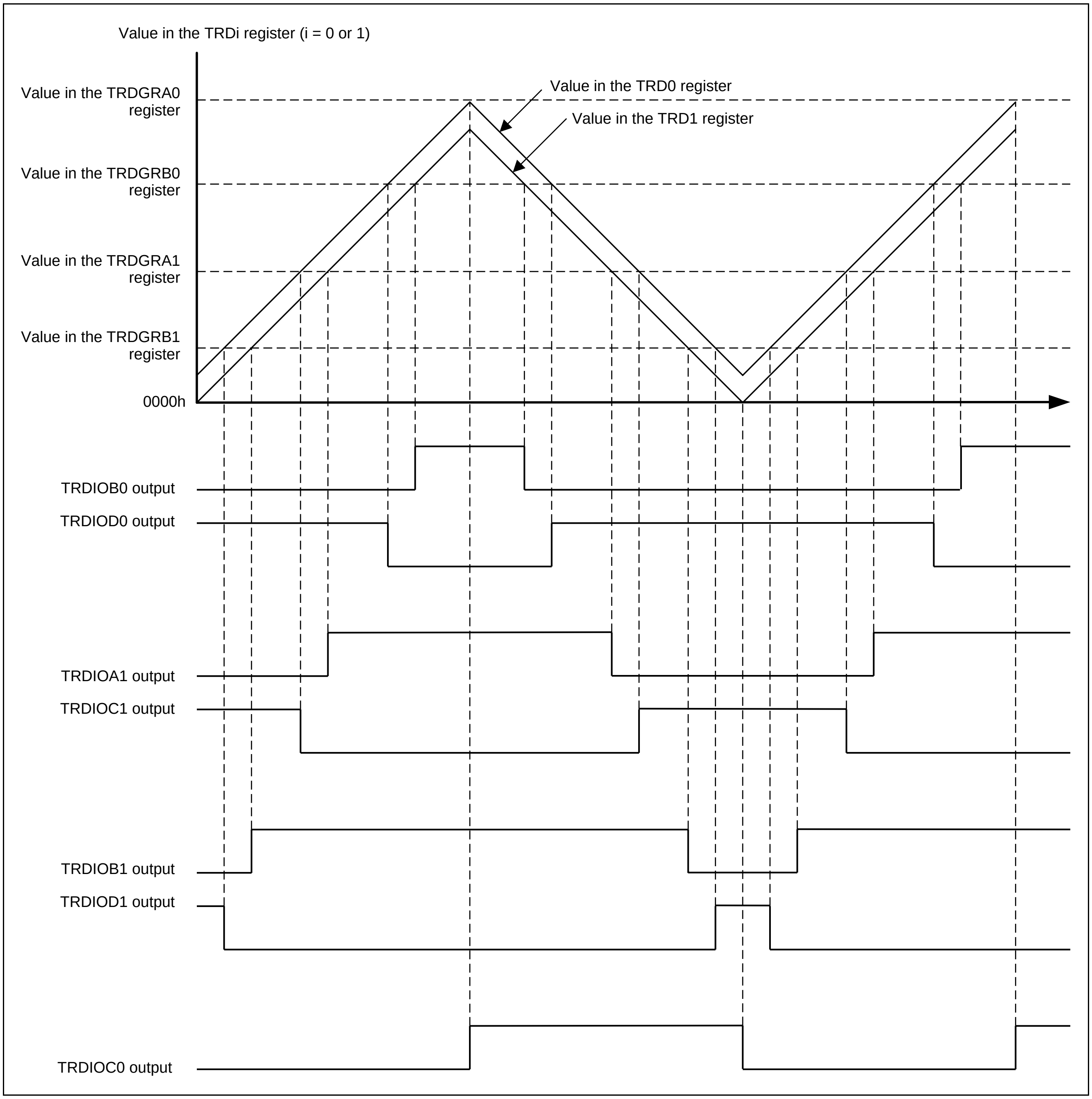


Figure 4. Complementary PWM Mode Output Model

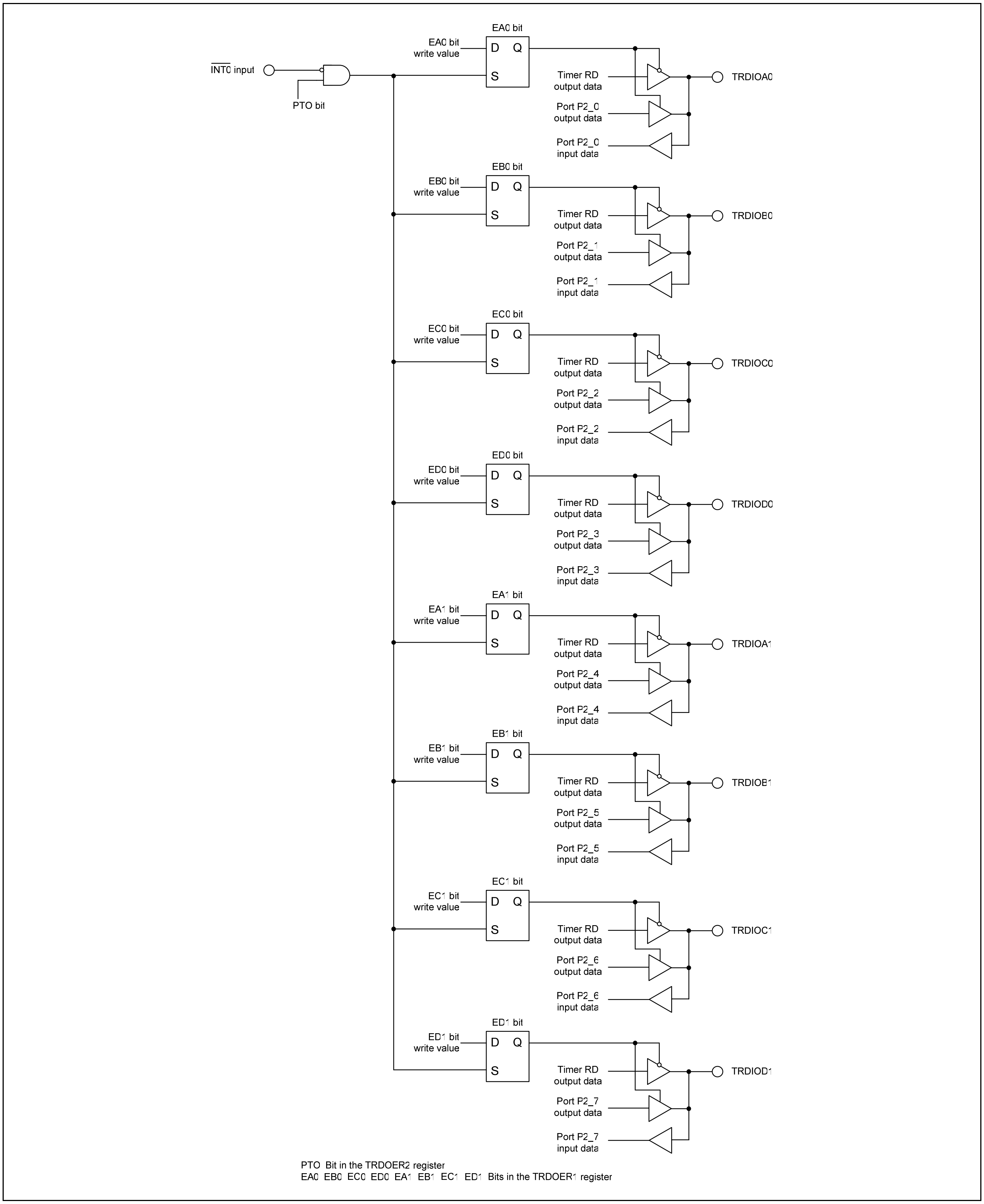


Figure 5. Pulse Output Forced Cutoff

4.3 General operation description

The block diagram in the figure below depicts how the BLDC motor is driven in this application. The six timer RD PWM outputs are connected to an intelligent power module (IPM) which in turn is connected to the three BLDC motor windings. The three Hall sensor outputs are connected to the three timer RC inputs through a conditioning circuit. If a change occurs on any of these three pins, an interrupt is generated. To monitor the overall current, a low value resistor is connected to the power bus. The voltage generated by this resistor is monitored by a comparator circuit whose output is changed from "H" to "L" when the power bus current is over a threshold value. This change will cause a hardware forced cutoff and an $\overline{\text{INT0}}$ interrupt. The timer RC input capture function is used to monitor the change in state of the Hall sensors, and the captured counter value is used to calculate the motor speed. Timer RD is used to generate the required complementary PWM waveform. The $\overline{\text{INT0}}$ interrupt is used in conjunction with timer RD to perform an overcurrent protection forced cutoff.

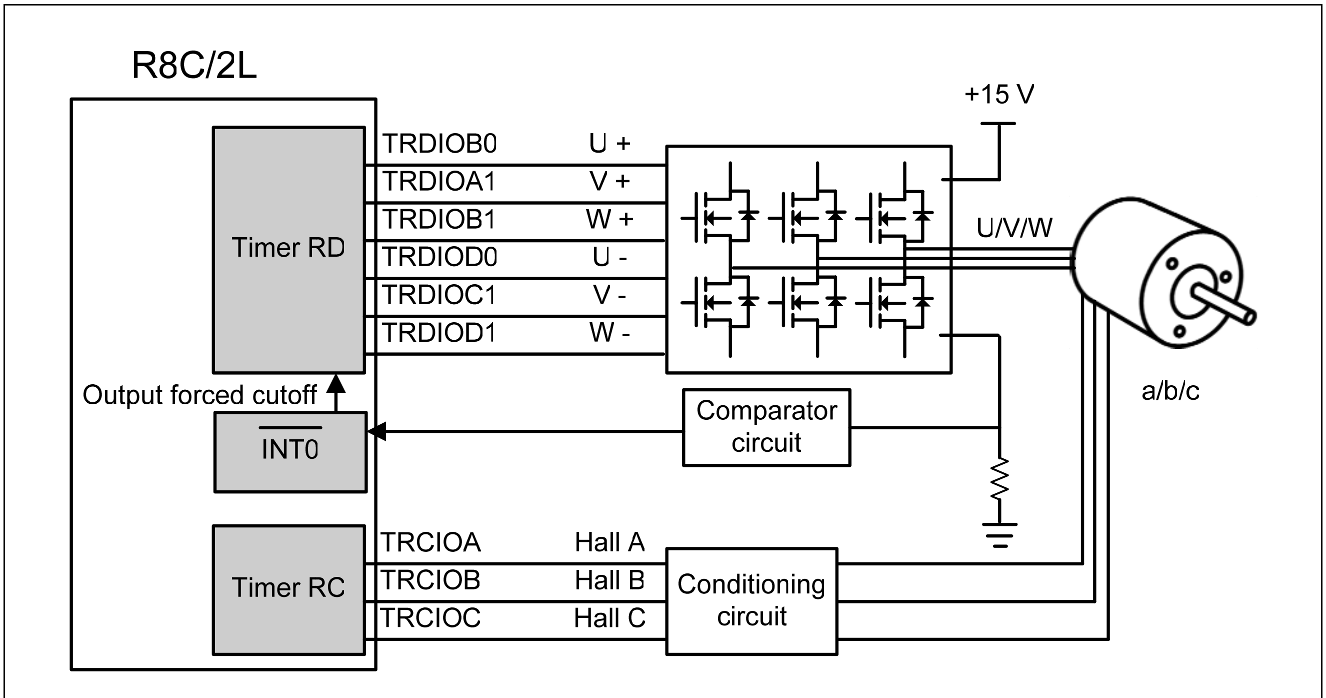


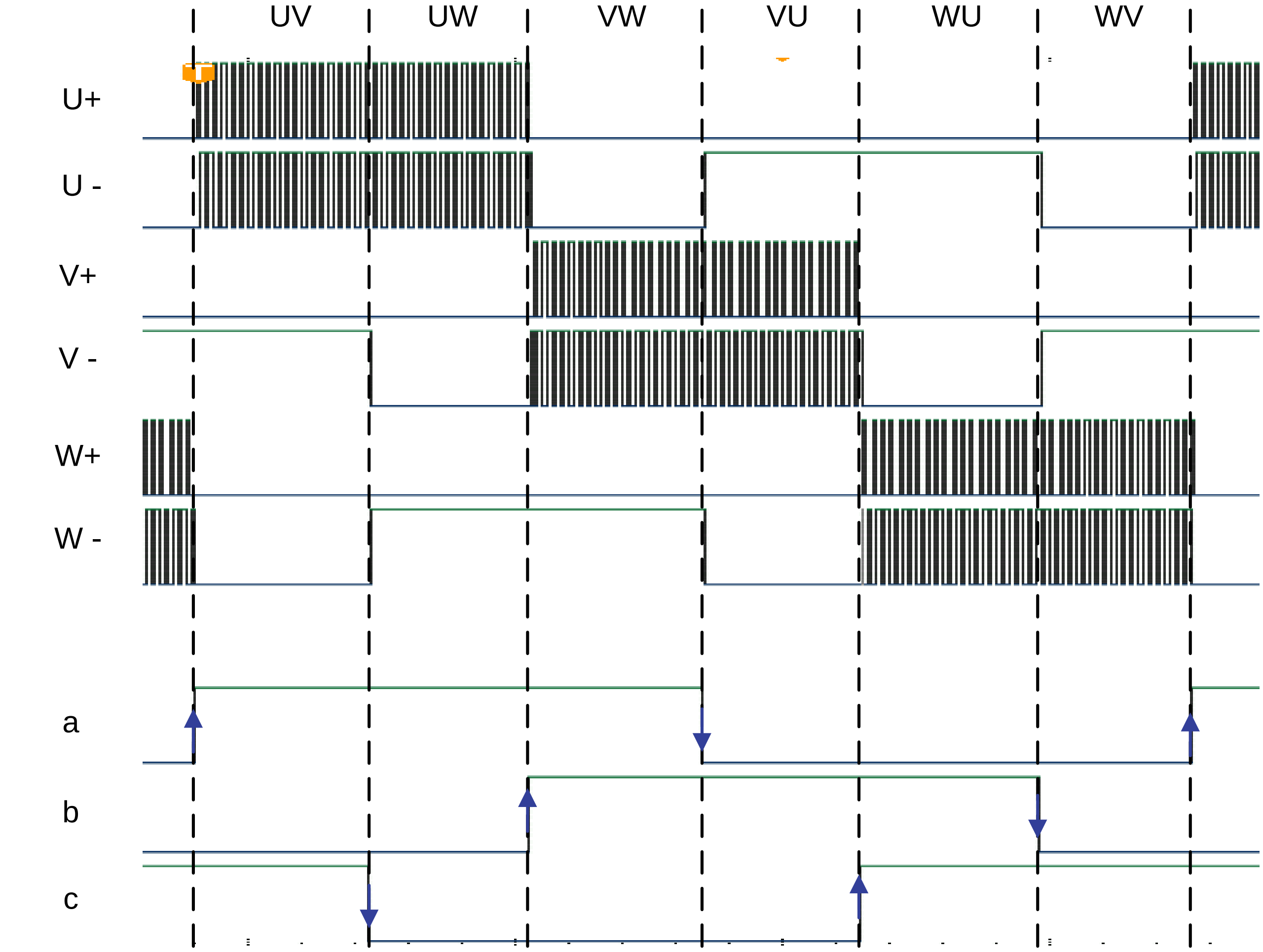
Figure 6. R8C/2L Based BLDC Motor Control

Table 2. Resource (Working Mode of Peripheral Functions)

Item	Selected Mode
Timer RC	Timer Mode (Input Capture Function)
Timer RD	Complementary PWM Mode
$\overline{\text{INT0}}$	Pulse Output Forced Cutoff input

In order to obtain a variable speed from the BLDC motor, voltage on terminals of the windings is modulated using the pulse width modulation (PWM) method illustrated in Figure 7.

During one state, the voltage is turned on and off at a carrier frequency. A PWM timer is used to modulate the output state of the pin. Modulation is typically performed at a carrier frequency higher than the state change frequency.



Hall sensor Value	101	100	110	010	011	001
P2	40h	80h	80h	08h	08h	40h
TRDOER1	F5h	F5h	AFh	AFh	5Fh	5Fh

Note: The output logic level of hall sensor depends on the characteristic of the sensor. And the commuting timing depends on the configuration of hall sensors. Therefore, the figure shown above is only applied to the motor described in this application note.

Figure 7. Six Step Commutation Timing

5. Setup procedure

5.1 Register settings

Table 3 lists the related registers' settings.

Table 3. Register Setting Table (1/2)

Register Name		Address	Setting Value	Function
CM0	System Clock Control Register 0	0006h	08h	XIN clock oscillates
CM1	System Clock Control Register 1	0007h	28h	XIN-XOUT drive capacity: High, no division mode
OCD	Oscillation Stop Detection Register	000Ch		Selects XIN clock, Oscillation stop detection function disabled
PRCR	Protect Register	000Ah	01h 00h	Enable and disable protection of critical registers
TRAMR	Timer RA Mode Register	0102h	10h	Timer mode, count source: f8
TRAPRE	Timer RA Prescaler Register	0103h	F9h	Set timer RA timer interval to 10 ms
TRA	Timer RA Register	0104h	63h	
TRAIC	Timer RA Interrupt Control Register	0056h	05h	Enable timer RA interrupt, priority level: 5
TRACR	Timer RA Control Register	0100h	01h	Start timer RA
PINSR3	Pin Select Register 3	00F7h	1Fh	Set to 1Fh when using timer RC
TRCMR	Timer RC Mode Register	0120h	88h	Timer Mode (Input Capture Function), start timer RC
TRCCR1	Timer RC Control Register 1	0121h	40h	Counter Source: f32
TRCIC	Timer RC Interrupt Control Register	0047h	06h	Enable timer RC Interrupt, priority level: 6
TRCIER	Timer RC Interrupt Enable Register	0122h	87h	Enable input capture interrupts on channels A, B, and C. Enable timer RC overflow interrupt
TRCIOR0	Timer RC I/O Control Register 0	0124h	6Eh	Input capture occurs at both rising and falling edge
TRCIOR1	Timer RC I/O Control Register 1	0125h	66h	Edges on channels A, B, and C
TRCDF	Timer RC Digital Filter Function Select Register	0131h	07h	Enable digital filter on channels A, B, and C digital filter's sampling clock: f32
TRDSTR	Timer RD Start Register	0137h	0Ch	Count continues after compare match between TRD0 and TRDGRA0, and between TRD1 and TRDGRA1
TRDMR	Timer RD Mode Register	0138h	E0h	TRDGRD0, TRDGRC1, and TRDGRD1 function as buffer registers for TRDGRB0, TRDGRA1, and TRDGRB1

Table 3. Register Setting Table (2/2)

Register Name		Address	Setting Value	Function
TRDFCR	Timer RD Function Control Register	013Ah	0Fh	Transfer value set in buffer registers to general registers at the compare match between TRD0 and TRDGRA0. Normal-phase and counter-phase output: Initial output is low, Active level is high
TRDOER1	Timer RD Output Master Enable Register 1	013Bh		
TRD0	Timer RD Counter 0	0146h/ 0147h	0048h	Set dead time: 3.6 us
TRD1	Timer RD Counter 1	0156h/ 0157h	0000h	Set to 0 before count start
TRDGRA0	Timer RD General Register A0	0148h/ 0149h	02E0h	Set carrier frequency: 15 kHz
TRDGRB0	Timer RD General Register B0	014Ah/ 014Bh		Set PWM active level width of normal-phase output
TRDGRA1	Timer RD General Register A1	0158h/ 0159h		
TRDGRB1	Timer RD General Register B1	015Ah/ 015Bh		
TRDGRD0	Timer RD General Register D0	014Eh/ 014Fh		
TRDGRC1	Timer RD General Register C1	015Ch/ 015Dh		
TRDGRD1	Timer RD General Register D1	015Eh/ 015Fh		
TRDSTR	Timer RD Start Register	0137h	0Fh	Start timer RD
INTEN	External Input Enable Register	00F9h	01h	Enable $\overline{\text{INT0}}$ input, one edge
INTF	$\overline{\text{INT}}$ input Filter Select Register	00FAh	03h	$\overline{\text{INT0}}$ input filtered with f32 sampling
TRDOER2	Timer RD Output Master Enable Register 2	013Ch	80h	Enable pulse output forced cutoff signal input $\overline{\text{INT0}}$
INT0IC	$\overline{\text{INT0}}$ Interrupt Control Register	005Dh	05h	Enable $\overline{\text{INT0}}$ interrupt, priority level: 5
PD4	Port P4 Direction Register	00EAh	00h	Set P4_5 as $\overline{\text{INT0}}$ input
PD1	Port P1 Direction Register	00E3h	00h	Set P1_1 as input capture port: TRCIOA and P1_2 as input capture port: TRCIOB
PD2	Port P2 Direction Register	00E6h	FFh	Set P2 as output PWM waveform output port
PD3	Port P3 Direction Register	00E7h	00h	Set P3_4 as input capture port: TRCIOC
PUR0	Pull-Up Control Register 0	00FCh	84h	Pull up P1_1, P1_2 and P3_4

5.2 Function Description

Table 4 lists the functions used in the BLDC motor control application.

Table 4. Function Description

Function Name	Function Description
main	C entry point
MCU_Clock_Init	Initialize MCU operation clock
Timer_RA_Init	Initialize timer RA to work in Timer Mode
Timer_RC_Init	Initialize timer RC to work in Input Capture Mode
Timer_RD_Init	Initialize timer RD to work in Complementary PWM Mode
State_Switch	Generate commutation sequence
Motor_Start	Motor starts
Delay_10ms	General delay purpose, delay for 10 ms
tra_handler	Timer RA interrupt service routine, used by delay function
trc_handler	Timer RC interrupt service routine, capture Hall sensors states
int0_handler	$\overline{\text{INT0}}$ interrupt service routine, over current protection

5.3 Globe Variable Description

Table 5 lists the globe variables used in the BLDC motor control application.

Table 5. Globe Variable Description

Globe Variable Name	Globe Variable Description
NewState	Next commutation state
DutyCycle	Timer RD PWM duty cycle value
CountCapture	Timer RC input capture counter value
CountRefH	Speed high limit
CountRefL	Speed low limit
ClockTick	1 tick delay
Counter_2s	2 second delay
SpeedFlag	Flag for indicating two different motor speeds
ErrorFlag	Flag for indicating overcurrent error

5.4 Software Description

1) Motor speed control

After reset, the motor will start to rotate at two pre-defined speeds (3000 rpm and 4000 rpm given a tolerance of 100 rpm) and toggle between one speed and the other at a 2 second interval.

Carrier frequency and duty cycle should be known as the requirement of the PWM control method. 15 kHz is selected for the carrier signal to be modulated.

In this application the angle between two consecutive Hall signals is 30 degrees by construction (two pole pairs mounted on the rotor). By using the Hall signal interrupts and the timer RC input capture function, the time between two consecutive Hall signals can be measured and speed can be computed.

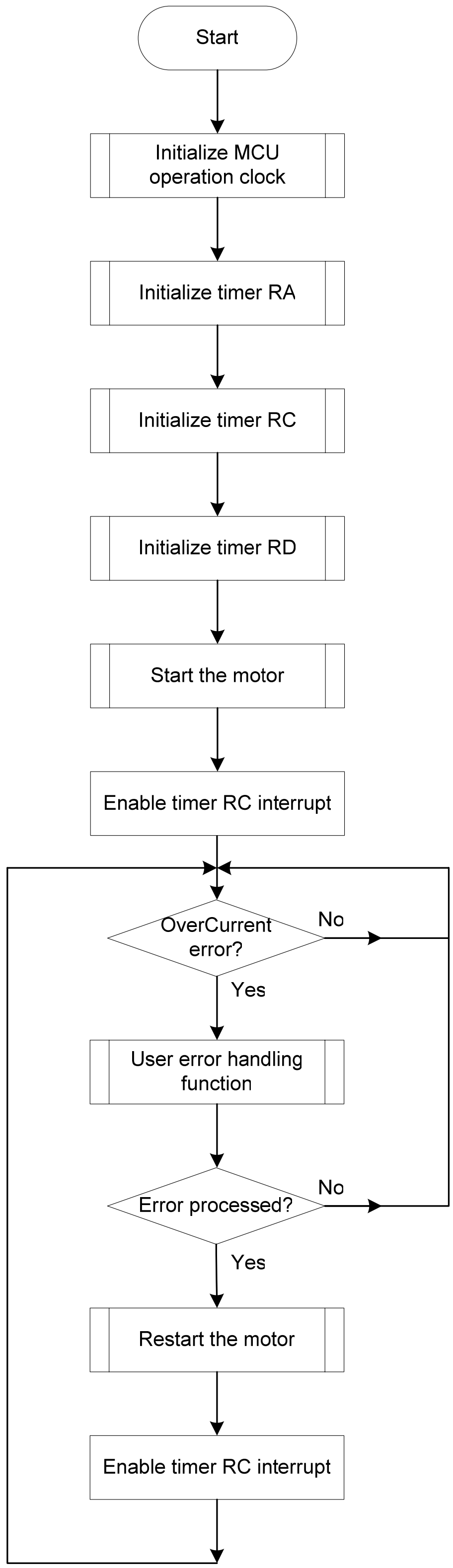
A simple control algorithm is used to adjust the duty cycle needed to maintain the desired speed. If the measured speed is high, the duty cycle is reduced; if the measured speed is low, the duty cycle is increased.

2) Starting the motor

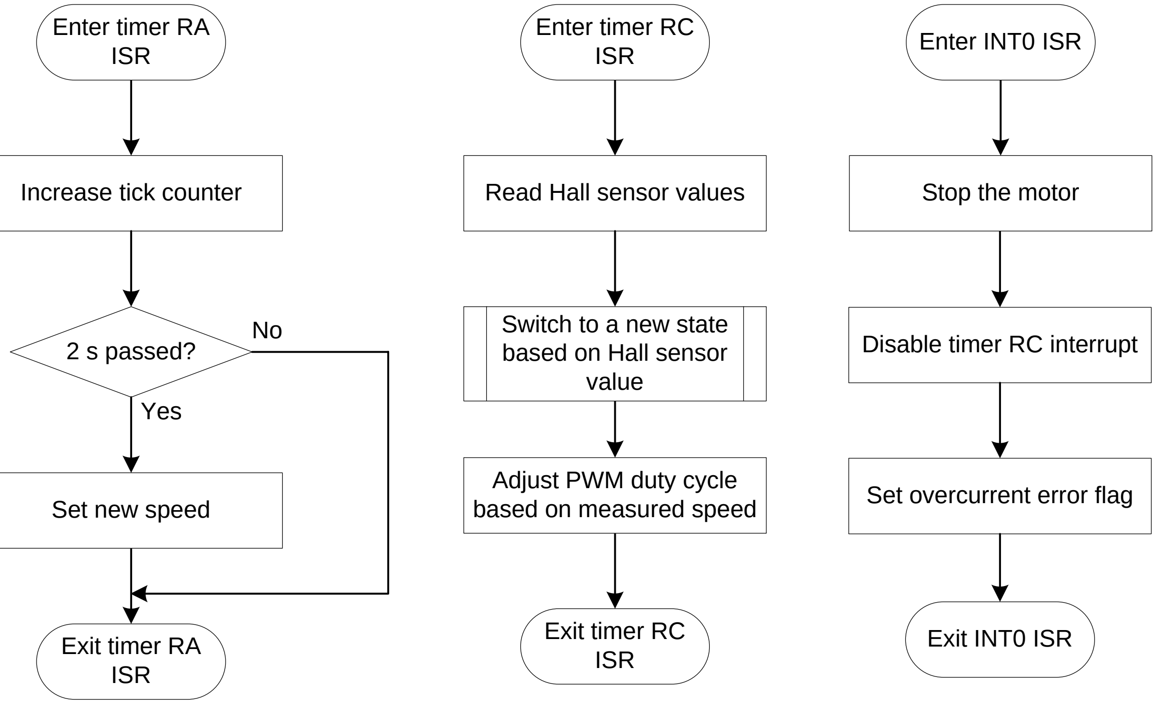
In this example, the motor is started at a 60% duty cycle with a fixed commutation period of about 500 rpm. This ensures that the motor has enough starting torque. Once the MCU starts to receive the Hall signals, the interrupt based commutation mechanism is stabilized.

5.5 Flowchart

5.5.1 Main function



5.5.2 Interrupt subroutine



6. Sample Programming Code

A sample program can be downloaded from the Renesas Technology Website.

To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

7. Reference

Hardware Manual

R8C/2K, 2L Group Hardware Manual

The latest version can be downloaded from the Renesas Technology Website.

Technical Update/Technical News

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