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H8/300L

Boot mode In-circuit Programming (Boot)

Introduction

The Renesas Flash Development Toolkit (FDT) is an onboard flash programming tool with user-friendly Graphical User Interface (GUI) for Renesas F-ZTAT (Flash Zero Turn Around Time) microcomputers. To shorten the development cycle, especially on reprogramming time of the mounted flash micon, it becomes essential to incorporate onboard programming feature onto the target board. This application note describes the hardware requirements for the H8/38024 flash micon in boot mode using FDT.

Target Device

H8/300L Super Low Power (SLP) Series - H8/38024F



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1. Overview

HD64F38024 micon has a 32-kbytes built-in flash memory. Onboard programming/erasing can be done in boot mode, in which the boot program built into the chip is started to erase or program of the entire flash memory.

Renesas Flash Development Toolkit (FDT) is an onboard programming GUI software, which connects the target board to the Host PC. This target board is mounted with HD64F38024 micon and built with onboard programming circuitry. The boot mode programming is achieved via SCI3 channel in asynchronous mode.

1.1 Boot Mode & Micro Kernel

Boot Mode conditions the internal FLASH circuitry and initiates an Auto Bootload sequence at RESET for programming/erasing the entire flash memory. Once the chip is set to boot mode, it will run a protected section of code known as the boot code. First, boot code negotiates a bit rate for an asynchronous serial connection (SCI3) with the host. Next, the boot code downloads the Micro Kernel (μ Kernel) at 9600 bps from the FDT software running on host PC.

 μ Kernel in FDT is responsible for initialising the device, particularly to set up a valid stack pointer, enable flash memory and configure the required communication ports. It also downloads the FDT Main Kernel, which interfaces with the write, read, erase and blank check modules at 38400 bps for flash operations. The design of FDT is based on a split kernel approach.

In boot mode, μ Kernel uGen38024.cde is fixed at pre-defined baud rate of 38400 and clock frequency of 9.83 MHz, so no customisation of the μ Kernel is allowed.





2. Hardware Requirements

A simple onboard programming circuitry consists of the following three blocks: Crystal oscillator block, Boot mode's setting block and Serial communication block.

2.1 Crystal Oscillator Block

The clock circuitry comprises of a 9.8304 MHz quartz crystal for the main clock and a 32.768 kHz quartz crystal for the sub clock. This 9.8304 MHz crystal on the H8/38024F target board allows FDT to download programming data at a baud rate of 38400 bps with bit error rate of 0%.

n = 0 for $\phi = 9.8304/2$ (MHz) = 4.9152 (MHz) $N = \frac{OSC \times 10^{6}}{64 \times B \times 2^{2n}} - 1$[1] Given OSC = 9.8304 (MHz), B = 38400 (bps) and n = 0, Hence, N = 3

 $Error = \left[\frac{\phi \times 10^{6}}{(N+1) \times 64 \times B \times 2^{2n-1}} - 1\right] \times 100\%$ Hence, Error = 0 %.

Therefore, a baud rate of 38400 bps is chosen for a main clock of 9.8034 MHz.

2.1.1 Conditions

Stable VCC with decoupling capacitor of 0.1µF to GND



2.2 Boot Mode's Setting Block

To enter into boot mode, it requires the conditions of TEST = 0, P95 = 0 and P34 = 1. After /RES_N ends, HD64F38024 micon will be set to boot mode. The Reset Timing diagram is as follows:



Figure 2.1 Reset Timing of Boot Mode

2.2.1 Conditions

P95 is set HIGH after /RES_N goes LOW for 20 states

2.3 Serial Communication Block

FDT links the Target board to the Host PC using the on-chip, three-wire serial communication channel [SCI3] on the H8/38024F micon. This requires a RS232 transceiver [eg. SP3232ECT] to translate the RS232 signals. The connection between the Target board and the Host PC is using serial cable with DB-9 connectors.







3. Block Diagram of Onboard Flash Circuitry

The block diagram of an onboard flash circuitry for H8/38024F is shown in Fig 3.1. The detailed circuit diagram and BOM List can be found in Appendix A and Appendix B respectively.



Figure 3.1

Block Diagram of Onboard Flash Circuitry





4. Basic Operation of FDT v2.2

4.1 Creating a New Workspace

Click on Start menu of Windows[®] and select **Program** -> **Renesas** -> **FLASH Development Toolkit 2.2** to open the Welcome to the FLASH Development Toolkit dialog box.

Welcome to the F	LASH Development Toolkit	?×
罐	Create a new Workspace	
	 Open an existing Workspace Open an exisiting Image file 	
	OK Car	ncel



□ Enter the workspace name and click **OK** button.







□ Click **Yes** button to run Project Wizard



Fig 4.3 FLASH Workspace Manager dialog box

□ Enter the project name, then click **Next** button

WERE CO 40 DO CO 90 C7 09 4	Welcome to the FLASH Development Toolkit Project Wizard. The
7 2A SA CALL OF COLLEGE OF COLLEG	Project Wizard will guide you through the steps necessary to create a new project.
Display Device Image	The first step is to specify the name of your project. A project name must be no more than 100 characters in length and
Target files on the second sec	contain only valid filename characters.
1 5E 8A 33 4(S) Commis.mot	Project Name:
Motor Control	BIINK_LED
Target files	You may also add some comments to the project
8 92 1A 20 01 Drive, mot 8 27 91 08 1. Sp Data, mot 6 F0 58 FD 57 pata anot	Comments may be edited after creation and serve as a useful means to fully describe the purpose of a project.
E 50 9A DE A9 C5 64 85 97 8 24 D4 4D 75 54 AD 2D F6 5 8 4F EF 64 80 83 6F 60 12 1	Add Comments

Fig 4.4 Project Name dialog box



Select Device H8/38024F from the drop-down list, otherwise click Other... button to specify the kernel file (.fcf)

hoose Device And Kernel		
Workspace Industrial Co	The FLASH Development Toolkit supports a number of Hitachi FLASH devices. Select the device you wish to use with this project from the list Select Device: H8/38024F Other	
Device Image Target, files LCD.mot Keyboard.mu Comms.mot Device Image Target, files Target, files Device Image Target, files Device Image Device Image Device Image Device Image Device Image Device Image Device Image Device Image	Protocol B Compiler Hitachi 4.0A Kernel Path D:'Program Files'Hitachi\FDT2.2\Kernels Kernel Version 1_0_00	
	<back next=""> Cancel</back>	

Fig 4.5 Choose Device And Kernel dialog box

□ Select a port and use the default baud rate of 38400 bps, then click the **Next** button.

Fig 4.6

Workspace 1 ap 50 Workspace 'Industrial Co	The FLASH Development Toolkit supports connection through the standard PC Serial port and the USB port. Use this page to select your desired communications port. All settings may be changed after the project is created.
B of EC-I Device Image 0 00 PDP Target files on 0 00 60 rs 93 LCB.motor	Select port: COM1
Motor Control Device Image	The Baud Rate setting specifies a suitable speed for serial connection based on the device characteristics and the Target clock. The default baud rate is set up for use with a standard HMSE Evaluation Board. If you have a different clock on your Target you may need to select a different speed.
5 5D 9A DE A5 55 64 65 97 8 24 D4 40 75 54 AD 2D 76 1 8 47 E2 64 80 83 57 55 15 1	Select Baud rate: 38400 💌

Communication dialog box



• Enter the numerical values for the input clock of **9.83** MHz



Fig 4.7 Device Setting dialog box

Choose **BOOT Mode** as the operating mode, then click **Next**

Workspace Workspace 'Industrial Co Display Device Image Target files LCD.mot Kayboard.mi	The FLASH Development Toolkit can connect to your device in a number of different ways. All the options on this page may be changed after the Project has been created. Select Connection: • BOOT Mode • USER Program Mode For BOOT Program mode the Target device erases its FLASH prior to connection. The Toolkit downloads programming kernels to be device as required • Last the device as required
A Control Device Image Target files Device.mot Target files Device.mot Device.mot Device.mot	Select Interface: Direct Connection
6 20 36 30 20 20 20 20 20 20 20 20 20 20 20 20 20	The Target device must be waiting in BOOT SCI mode, the Toolkit will perform the remainder of the boot sequence automatically.

Fig 4.8

Communication dialog box



□ Select the **Protection Level** and **Message Level** during programming, then click the **Finish** button



Fig 4.9 Programming Options dialog box

□ An empty workspace will appear

PFLASH Development Toolkit 2,2	
Elle Edit View Project Device Image Iools Window Help	
🙀 📽 📅 📴 😝 🖇 🖻 🛱 📖 🗠 🗠 🏢 🖬 🖏 🔛 月 👪 🖬	💽 🔊 🎽 🖺
Workspace Demo1': 1 Project	
X X <t< td=""><td></td></t<>	
For Help, press F1 Not Connected	





4.2 Data Programming to the Flash Memory in Boot Mode

□ Press **Reset Switch** (S1) once and select [**Device** -> **Connect to device**]

TUGH DETEMPTION I	fooliot 2.2 - Demo1					- 0
Bie Lick Vere Broent	Device Image Tools Window	Bill (12+C		11		
6 6 6 3	Erase FLASH blocks	Alt+R	本目 第三部の 日本	BWA_LED	1 22 26 20 25 26 26 20 26 20 26 26 26 26 26 26 26 26 26 26 26 26 26	
S Intel space Toront in the	Upload Image	AR+U		_		_
B Blink_LED	Blank check	Ak+8				
Device Image		6.0140				
-		12222				
		United in				
-						
Disconnecting Disconnected						
Disconnect oper	ation complete					
A La D. Commenciere A	Minh (FD /					

Fig 4.11 Connect to Device pop-up menu

□ Select **Target Files** and right-click to **Add Files to Project** ...

File Edit View Protect		
The Real True Cather	it Gavice Inode Toop Murgan Help	
8889	CONTRACTOR DE CO	R 2 4 4 5 6 6 6 6 8 8
Workspace Ternol * 1 Ternok Lub Ternok Theorem Target Hes	Add fors to Project 21 x1 Lock m Image: State and the sta	
Connecting to Configuration: "BOOT Mode' co Opening post " Loaded Coums D Initiating BOO Using micro Am Micro-Amping Boud Downloading ma Downloading ma Downloading ma Connection com Connection Com	<pre>device 'B0/380247' on 'COM1' mmetion - using emulated interface COM1' DL UL Executed COM1' device terrol download successful rotsl.icondersesful rotsl.icondersesful rate to 39800 bps ink Retuil 'PiPrograms Files/Nitachi\PDT2.2\Rennels/ProtB\38024\hitachi\1_0_00\der ymicad genete upiete</pre>	2 902 4. ode* w03002 4. ode*

Fig 4.12 Add Target to Project dialog box



Select the target module and right-click to **Download to Device**. This will program the flash device.



Fig 4.13 Download to Device pop-up menu



4.3 Viewing or Erasing The Device Data

- □ Select [Device -> Upload image ...] to display Upload Image dialog box
- **D** Enter the **Start** and **End addresses**
- Click **Upload** button to read the Flash Memory data

Upla	ad Image ? 🗙
	Start address:
	0x00
	End address:
	0x7fff
	Length:
	0x8000
	Absolute Image
	Upload Cancel

Fig 4.14 Upload Image dialog box

RENESAS

H8/300L Boot Mode In Circuit Programming

APPENDIX A: Circuit Diagram











Appendix B: BOM List

	Designators	Part Description	Qty	Remarks
1.	C1, C3	Cap Electrolytic 100nF/50V	2	
2.	C2	Cap Ceramic 10nF/50V 10%	1	
3.	C4, C14 – 15	Cap Ceramic 100nF/50V 10%	3	
4.	C5 – 6	Cap Ceramic 15pF/50V 5%	2	
5.	C7 – 8	Cap Ceramic 12pF/50V 5%	2	
6.	C9 – 13	Cap Electrolytic 1uF/50V	5	
7.	R1	Res 1/4w 1MΩ 2%	1	
8.	R2-6	Res 1/8w 10kΩ 5%	5	
9.	U1	H8/38024F, FP-80A	1	
10.	U2	IC SP3232ECT RS 232 Driver/Receiver	1	
11.	Y1	Crystal 32.768 kHz Cylinder 2x6	1	
12.	Y2	Crystal 9.8304 MHz HC49/U-S	1	
13.	P1	Connector D-Sub Female 9-way	1	
14.	S1 – 2	Switch Tactile Round	2	

Reference

- 1. Renesas FLASH Development Toolkit 2.2: User's Manual
- 2. H8/300L Super Low Power Series Low-cost CPU Board CPUBD-38024F User' CPUBD-38024F User's Manual
- 3. H8/38024 Series, H8/38024F-ZTAT[™] Hardware Manual
- 4. FLASH Development Toolkit Kernel Guide [for FDT v1.5]





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