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M32C/84, 85, 86, 87, 88 Group

Block Transfer Using DMA

1. Abstract

The document describes how to perform a DMA transfer from one desired space to another desired space, setting the source and destination addresses to the forward direction addresses.

Use the peripheral functions listed below:

- Timer A in timer mode
- Two DMAC channels

One byte of the internal RAM is used as temporary RAM.

2. Introduction

The application example described in this document is applied to the following MCUs and parameter(s):

MCUs: M32C/84 Group
 M32C/85 Group
 M32C/86 Group
 M32C/87 Group
 M32C/88 Group

This program can be used with other M16C Family MUCUs which have the same special function registers (SFRs) as the above MCUs. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

The content of the 129-byte ROM table is transferred to RAM byte-per-byte every time a timer A0 interrupt request occurs. DMA0 is used for transfer from the ROM table to the temporary RAM, and DMA1 is used for transfer from the temporary RAM to RAM.

3.1 Example Description

- (1) If a timer A0 interrupt request occurs, a DMA0 transfer request and DMA1 transfer request are generated simultaneously. DMA0 has priority for execution.
- (2) Upon receiving its transfer request, DMA0 transfers one byte of data from the ROM table to the temporary RAM.
 The source address is incremented simultaneously.
- (3) Next DMA1 receives its transfer request and transfers one byte of data from the temporary RAM to RAM.
 The source address it incremented simultaneously.

NOTE:

Set the timer A0 period to the number of DMA0 or DMA1 transfers or more.

Figure 1 shows the Block Transfer Operation Timing Using DMA.

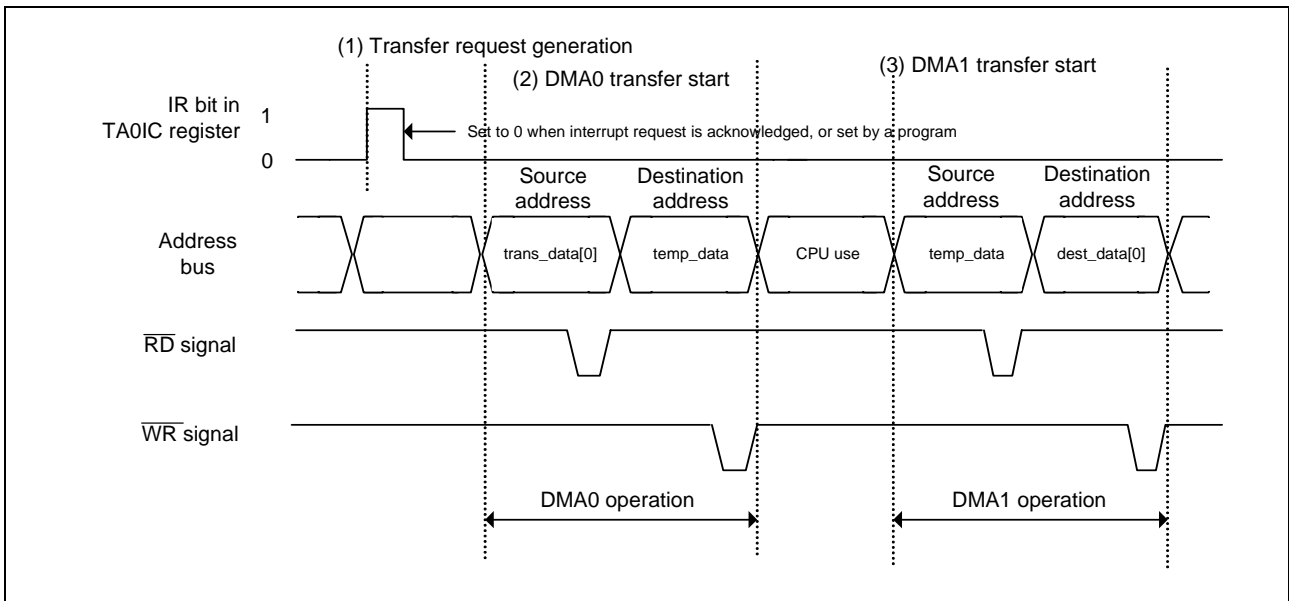


Figure 1 Block Transfer Operation Timing Using DMA

Figure 2 shows the Block Transfer Diagram Using DMA.

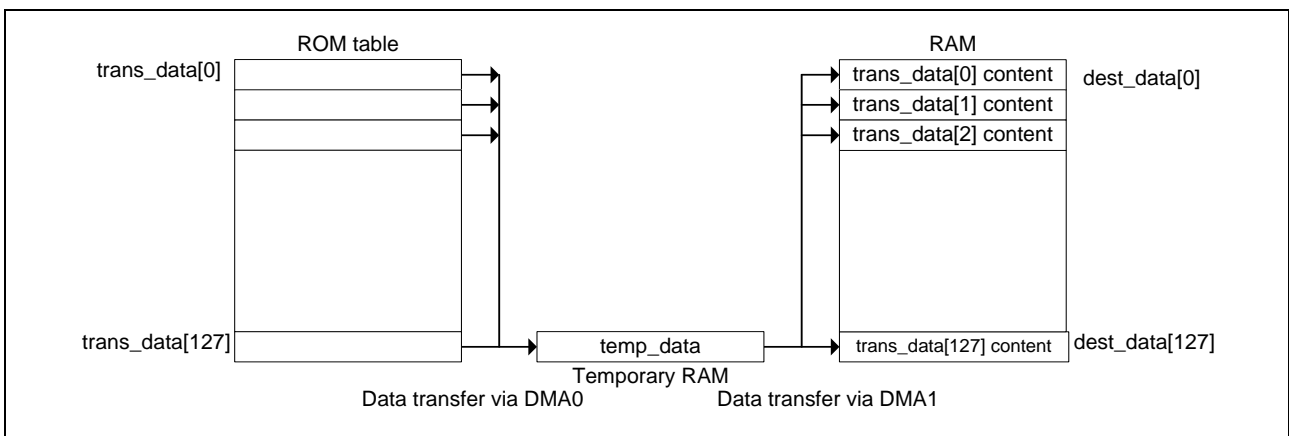
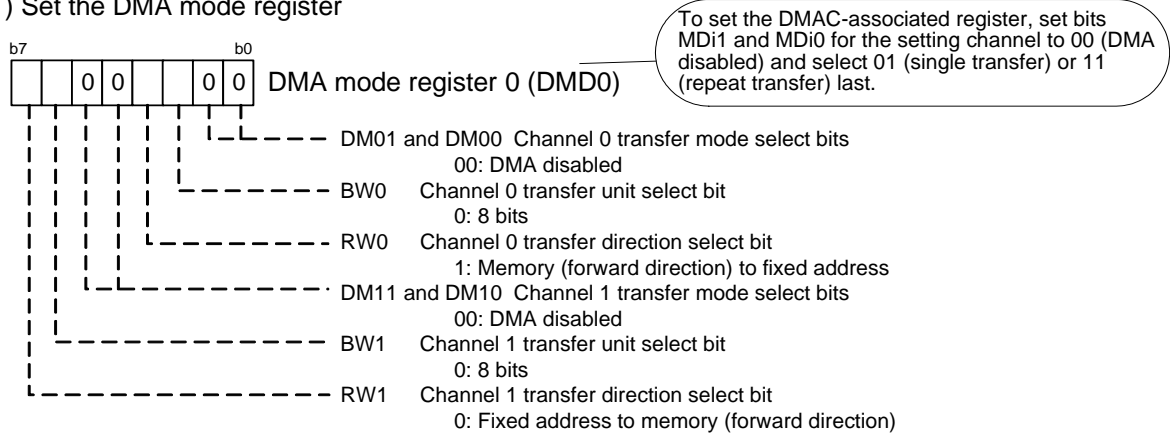


Figure 2 Block Transfer Diagram Using DMA

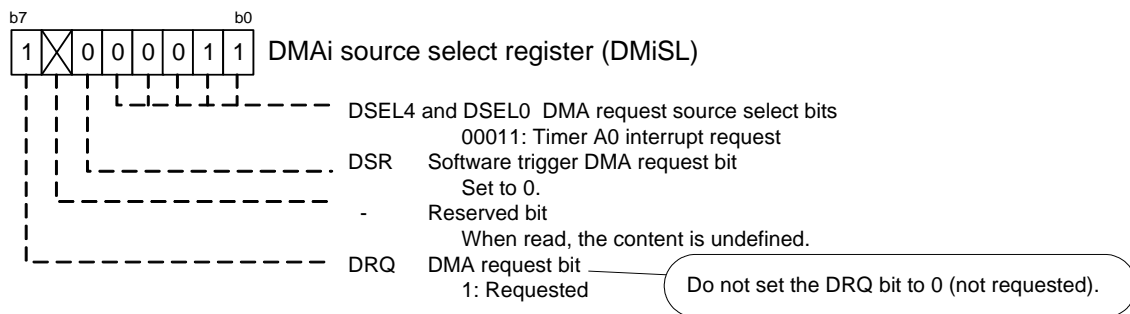
3.2 Setup

This section shows the setup sequence and values to perform **3.1 Example Description**. Refer to the MCUs Hardware Manual for details of individual registers.

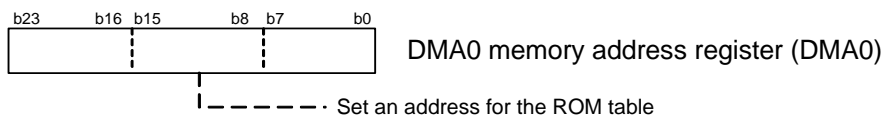
(1) Set the DMA mode register



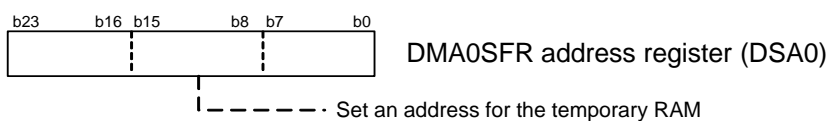
(2) Set the DMAi source select register



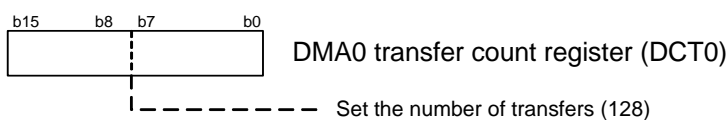
(3) Set the DMA0 memory address register



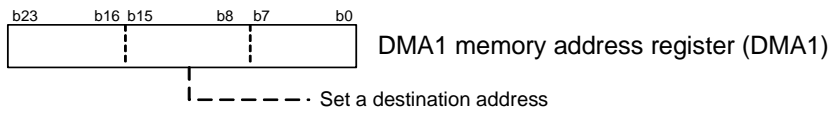
(4) Set the DMA0SFR address register



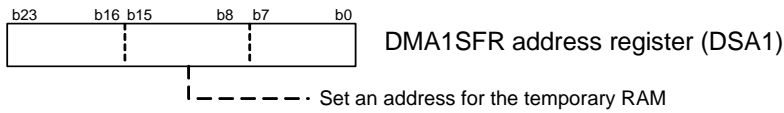
(5) Set the DMA0 transfer count register



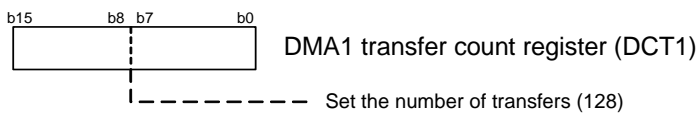
(6) Set the DMA1 memory address register



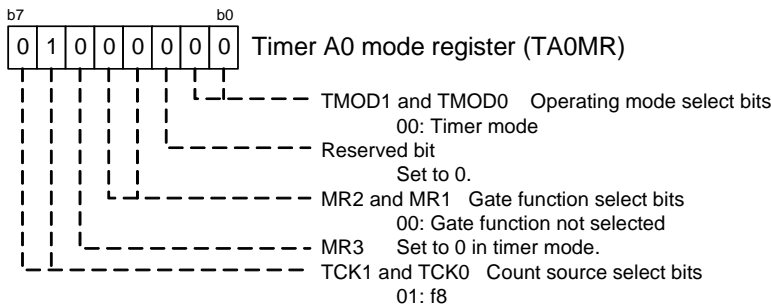
(7) Set the DMA1SFR address register



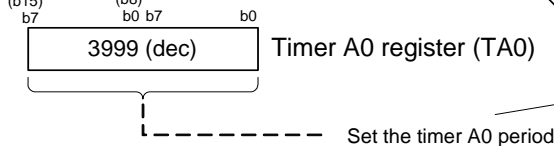
(8) Set the DMA1 transfer count register



(9) Set the timer A0 mode register

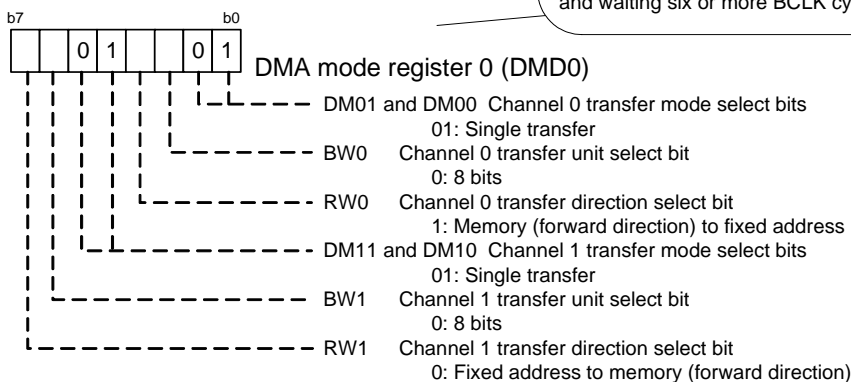


(10) Set the timer A0 register



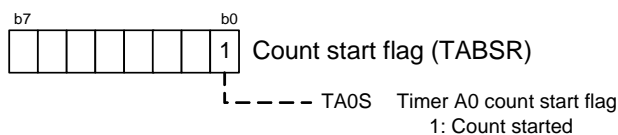
$X_{in} = 32 \text{ MHz}$
If the TA0 register setting value is n,
the timer A0 period is:
 $(n+1)/f8 = (3999+1)/((32 \times 10^6)/8) = 10^{-3} = 1 \text{ ms}$

(11) Set the DMA mode register



Enable DMA after setting the DMiSL register (i = 0 to 3) and waiting six or more BCLK cycles by a program.

(12) Set count start flag



4. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
For download, click “Application Notes” in the left-hand side menu of the M16C Family page.

5. Reference Documents

Hardware Manuals

M32C/84 Group Hardware Manual

M32C/85 Group Hardware Manual

M32C/86 Group Hardware Manual

M32C/87 Group Hardware Manual

M32C/88 Group Hardware Manual

The latest version can be downloaded from the Renesas Technology website.

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REVISION HISTORY	M32C/84, 85, 86, 87, 88 Group Block Transfer Using DMA
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		Page	Summary
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