Renesas Synergy™ Platform

Best Practices for Analog PCB Layout Using S1JA MCU

Introduction

This application note describes the best practices for analog PCB design using Renesas Synergy™ S1JA MCU Group.

Target Device

Renesas Synergy™ S1JA MCU Group

Contents

1. Overview

This Analog to Digital Converter (ADC) document offers best practices for analog PCB design, as well as a brief description of the S1JA ADC circuit.

1.1 S1JA Onboard ADC Offerings

An ADC is a system or circuit that converts an analog signal such as the output from a microphone or temperature sensor to a digital signal. The Renesas S1JA Microcontroller (MCU) includes two types of ADC converters:

- A Sigma-Delta ADC with 24-bits of resolution is attached to a programmable gain instrumentation amplifier able to take readings in either single ended or differential mode.
- A Successive Approximation ADC with 16-bits of resolution and is able to take readings in either differential or single-ended mode, it is attached to the outputs of the onboard operation amplifiers to allow internal buffering of analog inputs.

Both these units have unique features, such as extended programmable sample times and the ability to internally generate a bias current for external sensors. For the SIJA hardware manual, visit the S1JA MCU Group site on www.renesas.com.

1.2 Basics of ADC Measurement Accuracy

When examining the ADC's accuracy, it is important to focus on the system requirements; how small a signal change the system meant to react to. This is where least significant bit size (LSB) has the most impact, and thus signal range is critical. The following examples outline the impact LSB size has on a range of measurements.

The minimum stepsize is calculated as:

$$\frac{Total\ Range\ of\ Measurement}{2\text{^}(BitResolution)}$$

If measuring with the onboard converter a voltage range of…	LSB step size calculated for the 16-bit converter is…	LSB step size calculated for the 24-bit converter is…
+/-10V	$305uV$ per LSB	$1{,}192nV$ per LSB
+/- 2.5V	$76.3uV$ per LSB	$298nV$ per LSB
+/- 0.02V	$.610uV$ per LSB	$2nV$ per LSB

As the math shows, as the measurement gets smaller, the step size to be measured by one LSB shrinks into the noise; with the noise becoming more of an issue as gain is added to the system. How this issue relates to system or PCB design becomes evident when a simple effect of a voltage drop on a conductor is added to the example.

Let's assume a 1" conductor of ½ carrying a measurement current of roughly 10 µA. The resistive drop for the conductor alone is 1.3 µV; a drop detectable within the resolution of a 24-bit converter. This drop means as the measurement system increases in resolution, the amount of error towards the LSB end of the reading will be affected by the layout choices made.

1.3 Analog Signal Metrics

There are several key characteristics that define the ADC and its capabilities. These include the Signal-to-Noise ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SINAD), Effective Number of Bits (ENOB), Total Harmonic Distortion (THD), Least Significant Bit (LSB), and the signal voltage range. How to calculate these characteristics is widely published, with specific ADC values for the SIJA microcontroller found in the *S1JA Microcontroller Group User's Manual*.

2. Sources of Noise in Analog Circuit Design

2.1 Signal Types and Noise

All signals in a Printed Circuit Board (PCB) conduct electricity. These signals can generally be divided into three categories: power, digital, and analog. Each of these categories can cause degradation, resulting in the lack of accuracy in your measurement circuit.

- In general, PCB designs that supply a DC voltage are static, with respect to voltage and current. In addition, MCUs are usually tolerant to a small amount (usually in the millivolt range) of ripple. However, in practice, often the DC input voltage is used as an external reference to the ADC. It is here the ripple of the power supply becomes a concern, and it is generally advisable to either take the measurement with respect to the input voltage, or keep the voltage ripple to a minimum when it is compared to your measured signal.
- Digital signals are usually binary with well-defined voltage levels. These signals transition between specific high and low voltage levels and are used to convey logic data. Digital signals can be implemented in a wide range of voltage levels, with speeds ranging from nearly static to multiple Gigahertz. Due to the sharp edges and fast switching characteristics of digital signals, they can be relatively noisy. While digital signals are often not measured by the converter (it's usually done via a high speed comparator), the faster the rising edge, along with non-optimized trace routes, the more likely they can cause noise coupling issues near sensitive analog components.
- Analog signals differ from digital signals primarily in how the signals are used to interpret data. For most analog signals, data is extracted from the signal by interpreting either the voltage level, the current, or the signal frequency. Specialized circuitry is required to interpret the signal, which usually is then translated into digital data. This interpretation is the primary function of the Analog to Digital Converter (ADC), and it will be discussed later.

These types of signals all effect the accuracy of the converter's measurement, either through the reference, crosstalk, or layout design.

2.2 Power Domains (Analog versus Digital)

All Analog to Digital Converters contain circuits for both Analog and Digital logic, these circuits are called domains. Each domain has specific electrical characteristics. For successful operation of the ADC, the two domains typically are kept separate. Attention to the design and implementation of the power domains in a mixed signal system is critical.

2.2.1 Voltage Sources

The voltage sources in an electronic system can be a significant source of noise to both digital and analog circuits. Noise can be defined as unexpected or unwanted variation of a DC signal of voltage source. Analog systems can be very sensitive to voltage source noise, especially when the noise happens on analog reference voltages. Voltage source noise can easily translate to variation in the analog signal, which can result in false values detected by an ADC.

For example, if an analog reference voltage of 1.5 V has a 5-mV ripple noise component, this analog reference voltage is used as the reference in an amplification circuit for a 50-mV sinusoidal signal. When compared to ground, the actual level detection of the input signal could be incorrect by the amount of ripple noise at any point along the sinusoidal signal. If a point of the input signal has an actual voltage level of 20 mV, when compared to the noisy reference voltage, that point may be detected anywhere from 17.5 mV to 22.5 mV. If the gain in the amplification circuit is 100, the output becomes a signal from 1.75V to 2.25V.

Methods to reduce voltage source noise include correct selection of voltage converters, proper capacitive filtering, and proper routing of power regions.

Carefully consider the performance characteristics of any DC to DC converters, low dropout converters, or other DC power sources selected for use with analog circuits. Follow any design guidelines from the manufacturers of these devices to minimize the effects that they will have on the design. When selecting voltage source devices, try to choose devices with small ripple current values. For DC to DC converters, evaluate the switching frequency of the device, and try to avoid devices with a switching frequency that is close to the analog signals being evaluated.

Be sure enough bypassing capacitors are included on the output of each voltage source.

2.2.2 Unwanted Crosstalk

All conductors in a PCB can effect adjacent signals in the layout in what is called crosstalk. Crosstalk is the combination of mutually capacitive coupling and inductive coupling due to current flowing through adjacent conductors. The extent of crosstalk is highly dependent on the geometries of the layout, the dielectric materials of the PCB, and the switching frequencies of the signals. Many good discussions on crosstalk have been published that cover the physics involved. In general, the closer two signals are — the greater the effect each signal has on the other. For many digital interfaces, the effect of crosstalk is desirable, and using this effect is key to routing differential signal pairs.

To prevent unwanted crosstalk between conductors, separate dissimilar signals with large gaps between signals or signal groups. Use the guard band technique mentioned above to ensure sufficient spacing. Avoid parallel routing of signals or signal groups on adjacent layers.

2.2.3 Analog versus Digital Ground

In the past a general rule was to keep analog and digital circuitry separate, either physically or via a tightly controlled PCB floor plan. However, with the advent of MCUs, the separation of analog and digital return paths come together at the ADC, where analog signals are measured and converted to a digital count. As current flows from a voltage source to the converter, the return current flows in the opposite direction referred to as the return path. The return path is usually tightly coupled to the signal path, and correlates directly to inductance. This inductance scales resulting in a voltage drop, crosstalk, or in unwanted emissions, during transient switching periods. During these periods it is important to minimize the return current loop by providing a solid contiguous return path for current.

Methods to account for this condition are discussed in the next section.

3. Layout Considerations for ADC Circuits

3.1 Power and Ground Regions

To fully implement the separation of analog and digital domains, the power and ground areas associated with those domains should also be separated. It is highly recommended to have dedicated ground regions corresponding to each power region. For designs with a single, shared ground area, place a row of “stitching” vias along each side of the boundary between regions. Done correctly, stitching vias can reduce the length of the current loops for each domain and minimize the coupling between the domains.

One practice used to ensure domains are properly separated is to use guard band routing in the design. This routing is done by placing “dummy” traces (not connected to any net) in the space between analog and digital regions. These guard band traces are usually much wider than a normal signal trace (20 to 50 mils) and may be removed just prior to the completion of the design, so long as the resulting gap remains. The purpose is to force a large gap between the edges of the analog and digital domains.

3.2 Grounding Schemes

Return currents and impedances control the performance of your measurement system. Some of the common schemes utilized for PCB return paths are shown here. Before engineers place their first component, it is important that they have a tool box from which to pull designs.

While a solid copper plane should always be your first choice, these examples demonstrate that they may always not fit the application and that they also come in many different types. In general, reference systems can be split into the following categories:

- Figure 1 shows a single point return path that is found on low-cost designs, is focused on DC power up to a few megahertz, after which the impedance brought on the by length of the wires causes appreciable voltage drops between connections; or

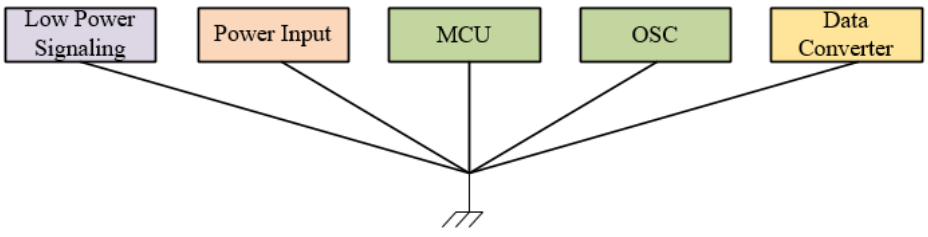

Figure 1. Single point return path example

- Figure 2 shows a hybrid single point return path, in which sections of the circuit with a common function, such as digital electronics, or an MCU and oscillator, are referenced together.

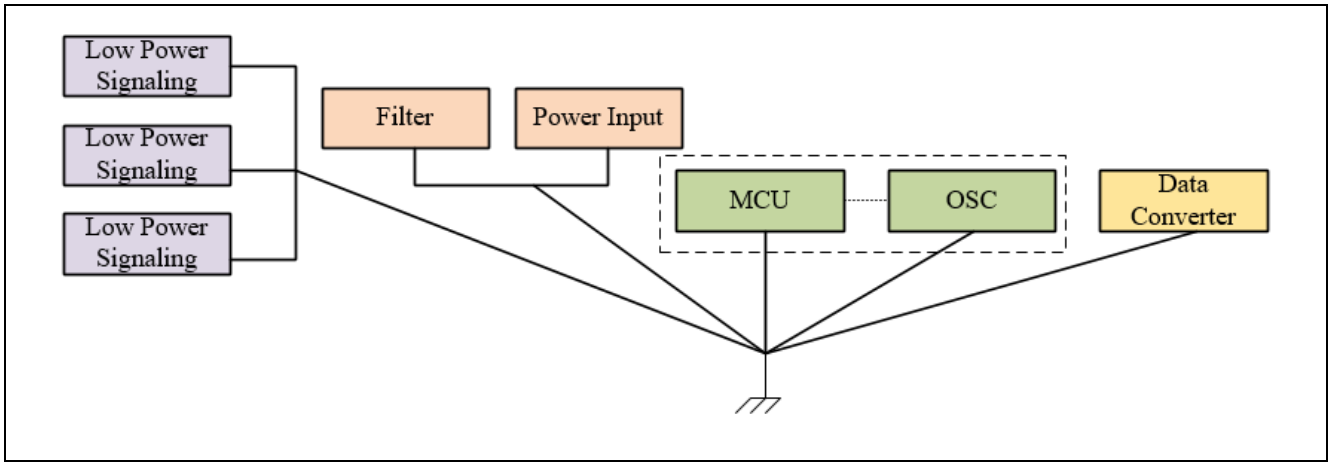

Figure 2. Hybrid single point return path

Figure 3 shows a multipoint reference system, which is a common improvement for a single-point reference scheme. Multipoint reference is commonly found on layouts requiring a high degree of performance at higher frequencies. These systems take the hybrid single-point scheme and improve upon it by making multiple connections that are shorter than 10 percent of the wavelength of the highest frequency signal traveling on the conductor.

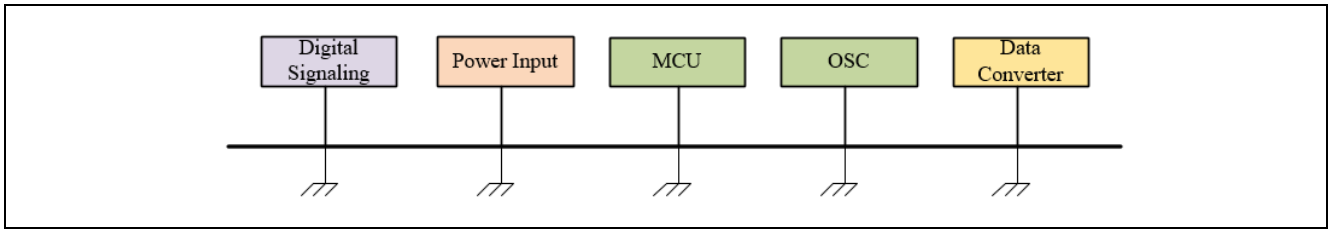

Figure 3. Multipoint reference, each module having their own tie to a common reference

3.3 Component Placement

The first method to reduce noise in an analog design is to physically separate analog and digital components whenever possible. Consider which portions of the design are analog and which are digital, then divide the layout into regions based on these domains. Diagram the system partition as a sketch or CAD file to represent the final product and where, in general, things could go. By doing this early in the design process:

- You can point out potential hazard points such as mounting hole issues; and
- Discover issues that may segment your return path, giving the layout engineer a head start on portioning their system.

By addressing the schematic and system requirements, the engineer doing the layout can zone off different sections of the board to get an idea of which groups of components will fit together. Figure 4 shows an example of a way of portioning a system.

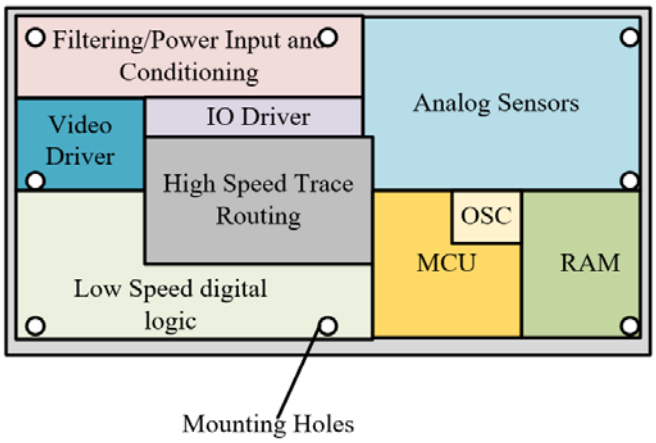

Figure 4. PCB Layout diagram example

Place the analog components in one region of the PCB, while placing the digital components in another region. In some cases, such as the Renesas S1JA MCU, a single component contains both analog and digital domains. In these cases, try place the mixed domain device at the boundary between the regions, and orient the device to minimize the areas where analog and digital signals may cross. If analog and digital domains must cross, try to restrict this to the borders between the regions. Note that these placement guidelines will benefit both analog and digital domains.

3.4 Routing Concerns

Figure 5 demonstrates an understanding in why routing — and as a corollary — a solid return path, is important in a design to minimize loop area and thus inductance in a signal path. Currents are thought of as wanting to take the path of least resistance back to the source, referred to as the idealized path back. However, as frequency increases return currents travel close to the signal path.

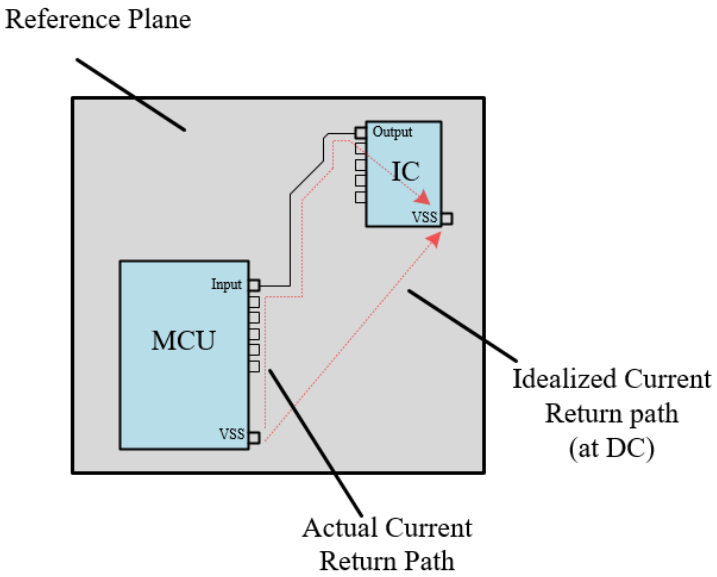

Figure 5. PCB routing diagram example

This means different things for different types of signals:

- For digital signals, the designer usually wants to control the impedance of these signals and as such the PCB traces for digital signals are typically designed to match the impedance of the related IC components. The impedance is controlled by the trace characteristics and the geometry of the trace to the return plane, a longer path, or a path over a segmented return plane will cause the impedance of the trace to change.

- For analog signals however, due to their speed it is uncommon for analog signals to have similar impedance requirements and as such the focus is mostly on noise free signals. Many analog designs are dependent on the impedance characteristics of the devices in the circuit, and any additional impedance, including that from the routing, can be detrimental to the performance of the circuit. As a rule, the lower impedance routing for analog signals will provide a cleaner signal and allow the circuit to perform as expected. It is recommended to use wider traces for analog signals. Also, it is also important to consider any requirements unique to the specific analog sensors chosen.

Analog signals can also be grouped by function or interface, and these groups should be routed separately from one another. For example, a design may include two analog sensors, one operating on a frequency of 500 kHz, and the other measuring the voltage of a relatively stable DC signal. These groups of signals should be separated from each other to prevent the 500-kHz signal from causing noise on the DC voltage in the other. Separate these signals with large gaps between the groups. Guard band traces can be used during layout to help force the additional separation; but, they should be removed prior to the completion of the design, leaving the gap intact.

In general, whenever possible, do not route signals across the boundaries between the analog and digital regions, especially on signal layers adjacent to the power or ground layers. When it is necessary to route analog signals across this boundary, try to route the traces perpendicular to the boundary, and minimize the length of the routing in the digital region.

3.5 Common PCB Stack-up Examples

This section covers a common set of PCB examples, but first it important to understand the basics that drive these decisions. From the previous section, it is evident that the goal of the PCB in a measurement system is control:

- The path of least impedance, which usually the path that is closest to the signal trace at higher frequencies; and circuit instability, or noise caused by voltage drops in conductors or cross coupling.
- For these reasons, there are a general set of rules that apply to stack-ups:
  - Always route a signal adjacent to a plane.
  - Signal layers should be routed close to their adjacent planes.
  - Power and return planes are to be placed near each other.
  - Critical traces spanning more than one layer should be confined to two layers on the adjacent to the same plane.
  - Multiple return planes are advantageous as they work to lower the impedance path of return currents.
  - Try to not split planes, either power or return. If you find that split planes are necessary, do not route a signal across them;
  - Keep the return loop area small by trying to have as contiguous of a return plane as possible, this will minimize loop area
  - If you have the choice of a power or return plane, choose the return plane;

Violating any one of these rules could increase your risk for emissions or cause impedance discontinuities leading to signal inaccuracies. The next section considers a few stack-up examples a layout engineer may use when designing their board.

3.5.1 2-Layer Design

Figure 6 shows a two-layer design, which is very common in most cases as it is one of the most cost-effective ways to implement a stack-up. In this case, it is especially important to be aware of current return paths. The power and ground must be routed as individual copper areas, or planes. A power plane could be implemented depending upon the requirements of the system, otherwise a single power net could be implemented. However, a solid copper return plane is necessary. Use caution to place analog routing and digital routing in separate areas of the design, since there is no power or ground layer between signal layers.

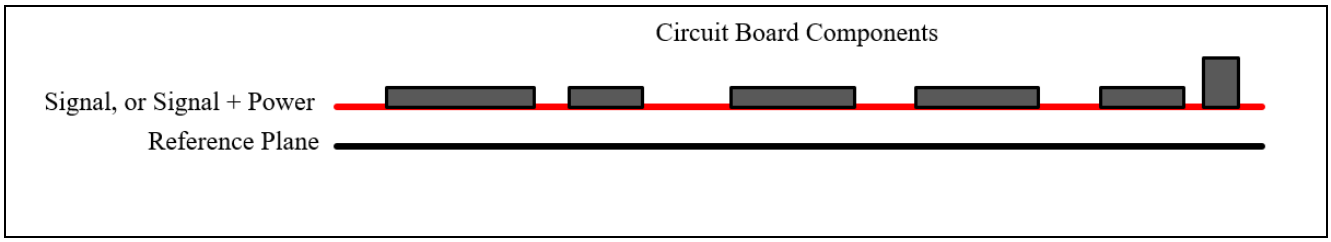

Figure 6. 2-Layer Design

3.5.2 4-Layer Design

Figure 7 shows that for the best signal quality in the minimum number of layers, a 4-layer design is a good choice. Both designs below adhere to a portion of the objectives mentioned previously; one sandwiches the signal in between the return layers, while another keeps the signals adjacent and on the outside.

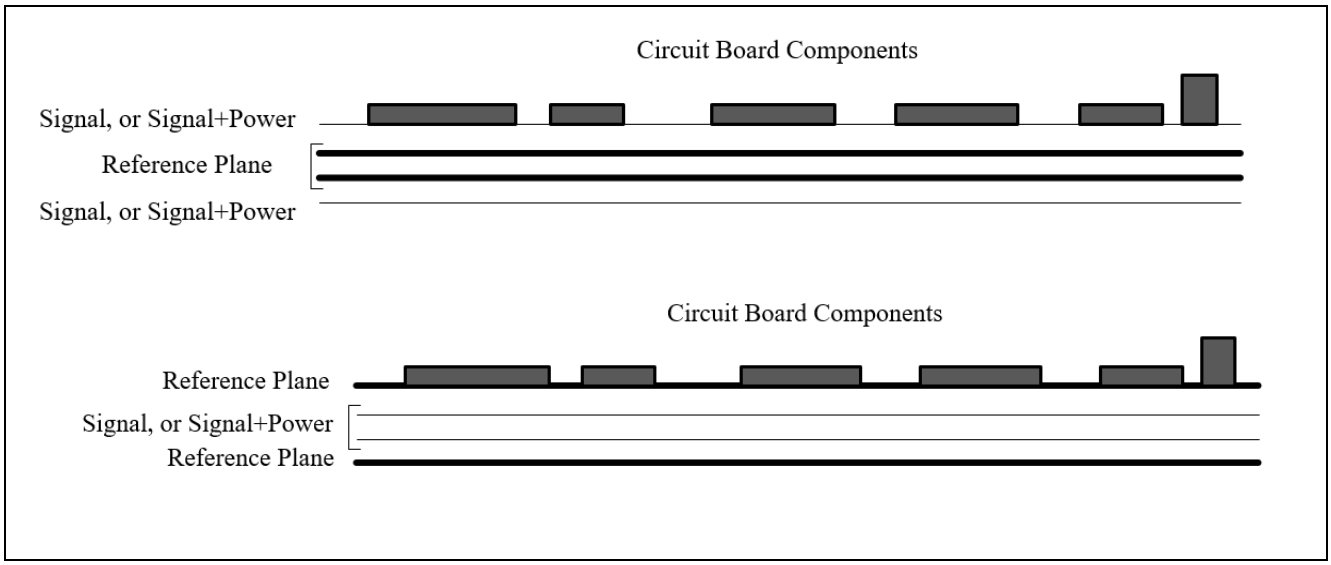

Figure 7. 4-Layer Design

3.5.3 6-Layer Design

Figure 8 shows that in more complex designs a stack-up with more layers may be required. For designs with 6 or more layers, organize the layers with alternating signal and ground/power planes. Use the internal power and ground planes as the reference for signal layers. For stack-ups with adjacent signal layers, such as the middle of a 6-layer stack-up, avoid routing analog and digital signals in the same area. If signals must be routed through the same area on adjacent layers, always try to use orthogonal routing between layers.

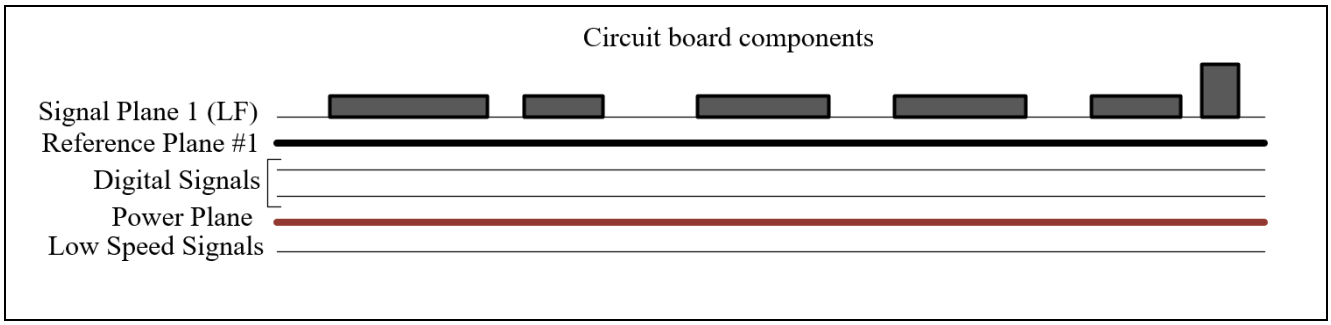

Figure 8. 6-Layer Design

4. S1JA Specific Requirements

4.1 What is the Renesas Synergy™ S1JA MCU?

The S1JA is a small, highly integrated Microcontroller Unit (MCU) with a dedicated analog front-end. S1JA includes a 16-bit SAR ADC, a 24-bit Sigma-Delta ADC, and Operational Amplifiers with configurable switches.

Additional features of the Renesas S1JA include:

- Arm® Cortex®-M23 core, operating up to 48 MHz
- Up to 256 KB code flash memory
- 32-KB SRAM
- 12-bit D/A converter
- 8-bit D/A converter

For details on the features and usage of the Renesas S1JA MCU, see the *S1JA MCU User's Manual*.

4.2 Required Support Components

The Sigma Delta ADC inside the Renesas S1JA requires two external capacitors for proper functionality. Connect a 0.47 µF external capacitor between ADREG and ground. Connect a 0.22 µF capacitor between SBIAS/VREFI and AVSS1. Refer to the Renesas *S1JA MCU User's Manual*, sections 33.3.2 and 33.3.3, for more details.

5. Additional Resources

See the Synergy Platform Website and Support links on the following page for additional resources. For example, to order the TB-S1JA Kit from Renesas or from a local distributor, visit the kit page (www.renesas.com/synergy/kits) on the Renesas website.

These links, in addition providing you with ordering information, enable you to download schematics, find relevant application projects, obtain technical updates, and more.

Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

Synergy Software	www.renesas.com/synergy/software
Synergy Software Package	www.renesas.com/synergy/ssp
Software add-ons	www.renesas.com/synergy/addons
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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan.11.19	—	Initial version

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