Application Note

DA1468x Application Hardware Design Guidelines

AN-B-061

Abstract

Minimal reference schematic, circuit explanation and design guidelines for BLE applications based on the DA14680-01, DA14681-01, DA14682-00 and the DA14683-00 SoCs.

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1 Terms and definitions

AQFN	Advanced Quad-Flat No-leads (package)
BLE	Bluetooth® Low Energy
BUCK	Type of DC/DC converter
CCCV	Constant Current Constant Voltage (battery charger type in the DA1468x)
CS	Chip Select
DC/DC	DC-to-DC Converter
DK	Development Kit
FTDI	Brand name of USB – UART interface
GPIO	General Purpose Input Output
OTP	One Time Programmable
PCB	printed circuit board
PTH	Plated Thru Hole
SDK	Software Development Kit
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transceiver
WLCSP	Wafer Level Chip Scale Package

2 References

[1] DA14680-01, DA14681-01, DA14682-00, DA14683-00 Datasheet, Dialog Semiconductor.

[2] DA1468x Pro-Development Kit, Dialog Semiconductor.

[3] AN-B-056 - DA14680_681 Recovery from System Level ESD Events, Dialog Semiconductor.

[4] AN-B-45 - DA1468x Booting from serial interfaces, Dialog Semiconductor.

3 Introduction

The DA1468x family are flexible System-on-Chips combining an application processor, memories, cryptography engine, power management unit, digital and analog peripherals and a Bluetooth® Smart MAC engine and radio transceiver. The chips are based on an ARM® Cortex®-M0 CPU delivering up to 84 DMIPS and provides a flexible memory architecture, enabling code execution from embedded memory (RAM, ROM) or non-volatile memory (FLASH, OTP).

For the DA14680/682, a QSPI flash of 8Mbit capacity is embedded in the package, whereas for the DA14681/683 the QSPI flash is resided externally and it is connected to the chip with the QSPI bus.

There are two available packages for the DA14681 and DA14683: WLCSP53 and AQFN60.
And one package is available for the DA14680 and DA14682 having the embedded QSPI Flash: AQFN60.

Table 1: DA14680/14682 and DA14681/14683 chip options

Chip	package	No of pins	QSPI Flash
DA14680/682	AQFN60	60	8Mbit embedded
DA14681/683	WLCSP53	53	External QSPI flash
	AQFN60	60	

The purpose of this document is to present the absolute necessary circuit required for proper operation of DA1468x. Based on this, system designers can build a BLE application on the top of it. Recommended schematic, chip interfaces and surrounding components as well as PCB layout guidelines of the DA1468x SoC family are provided.

4 Device revision numbering and Marking

The revision number of the chip can be read from the device by reading below ARM registers (Table 2 and Table 3). The combination of this will explain the commercial chip revision (Table 4)

Table 2 CHIP_REVISION_REG (0x50003204)

Bit	Mode	Symbol	Description	Reset
7:0	R	REVISION_ID	Chip version, corresponds with type number in ASCII. 0x41 = ‘A’, 0x42 = ‘B’.	-

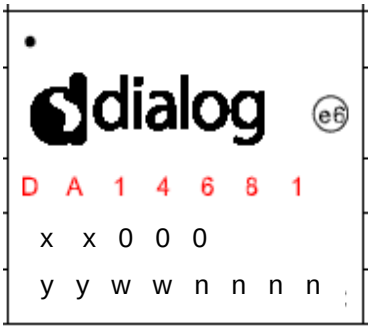
Table 3 CHIP_TEST1_REG (Minor revision)

Bit	Mode	Symbol	Description	Reset
7:0	R	MINOR	0x00 = ‘A’, ..., 0x03 = ’D’, 0x07 = ‘E’.	-

The chip’s commercial version number can be read from Table 4, below:

Table 4 Chip revision numbering

Commercial number	CHIP_REVISION_REG (0x50003204)	CHIP_TEST1_REG (0x5000320A)
DA14680-01/681-01 DA14682-00/683-00	0x41 (A) 0x42 (B)	0x07 (E) 0x01 (B)



Version format: xx = commercial chip revision: ‘00’ or ‘01’.

Date code format: yy = Year, ww = Week, nnnn = Dialog internal number

5 Minimal design for the DA1468x SoC

The DA1468x SoC requires a minimum number of external components for proper operation.
These are a 16MHz crystal, a DCDC inductor and a number of supply rail decoupling caps.
The absolute necessary sections required for a minimal system operation are the Power section, Crystals, UART, JTAG, Flash memory and Radio section.
The external QSPI flash memory chip is only required for the DA14681 and DA14683, which do not have an embedded flash memory.
A 32MHz crystal is only supported by the DA14682 and the DA14683. 16 MHz crystal operation is supported by all types.
The 32.768 KHz crystal is optional, alternatively the internal accurate RCX oscillator can be used as sleep clock.

Below are the block diagram and minimal schematics for the two packages AQFN60 and WLCSP53. Only the schematics for the DA14681 and DA14683 are given, the DA14680 and DA14682 schematics are identical except for not having the external QSPI flash chip.
Please be aware that the DA14680 and DA14682 QSPI signals are not available externally since these pins are not bonded out. Hence the 10K pull-up resistor on the DA14680's and DA14682's /CS (P0_5) pin can be omitted as well. This 10K pull-up resistor is R3 in the schematics.
Please note that the VDDIO pin, for the interface supply voltage of the embedded QSPI flash, still needs to be connected to V18, the 1.8V supply rail for the internal QSPI flash.

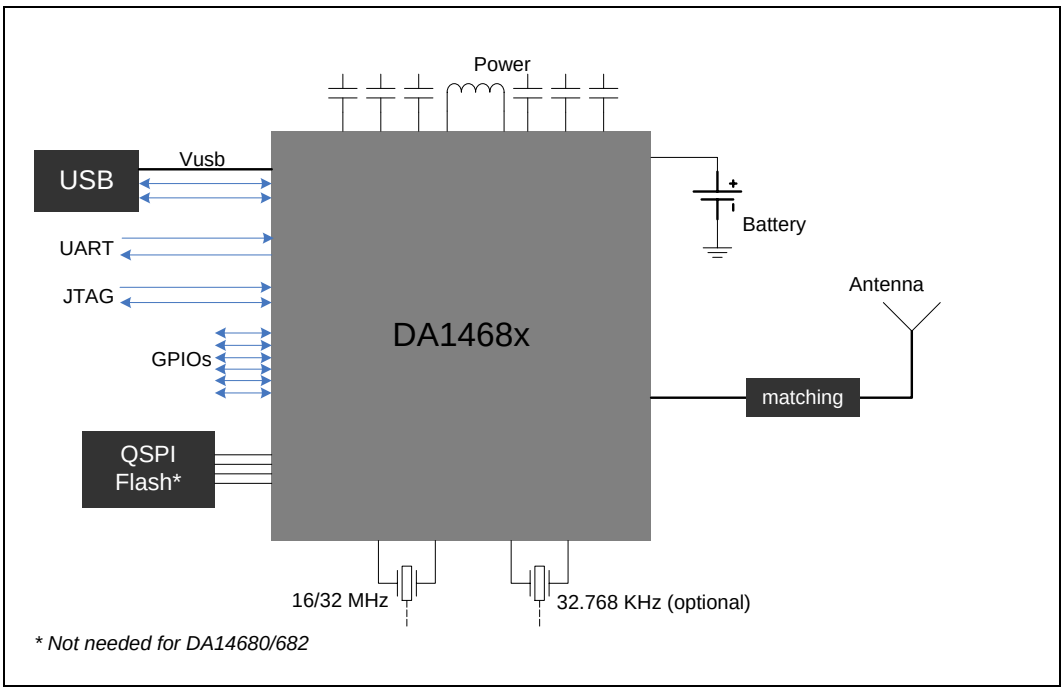


Figure 1: Block diagram of the DA1468x minimal design

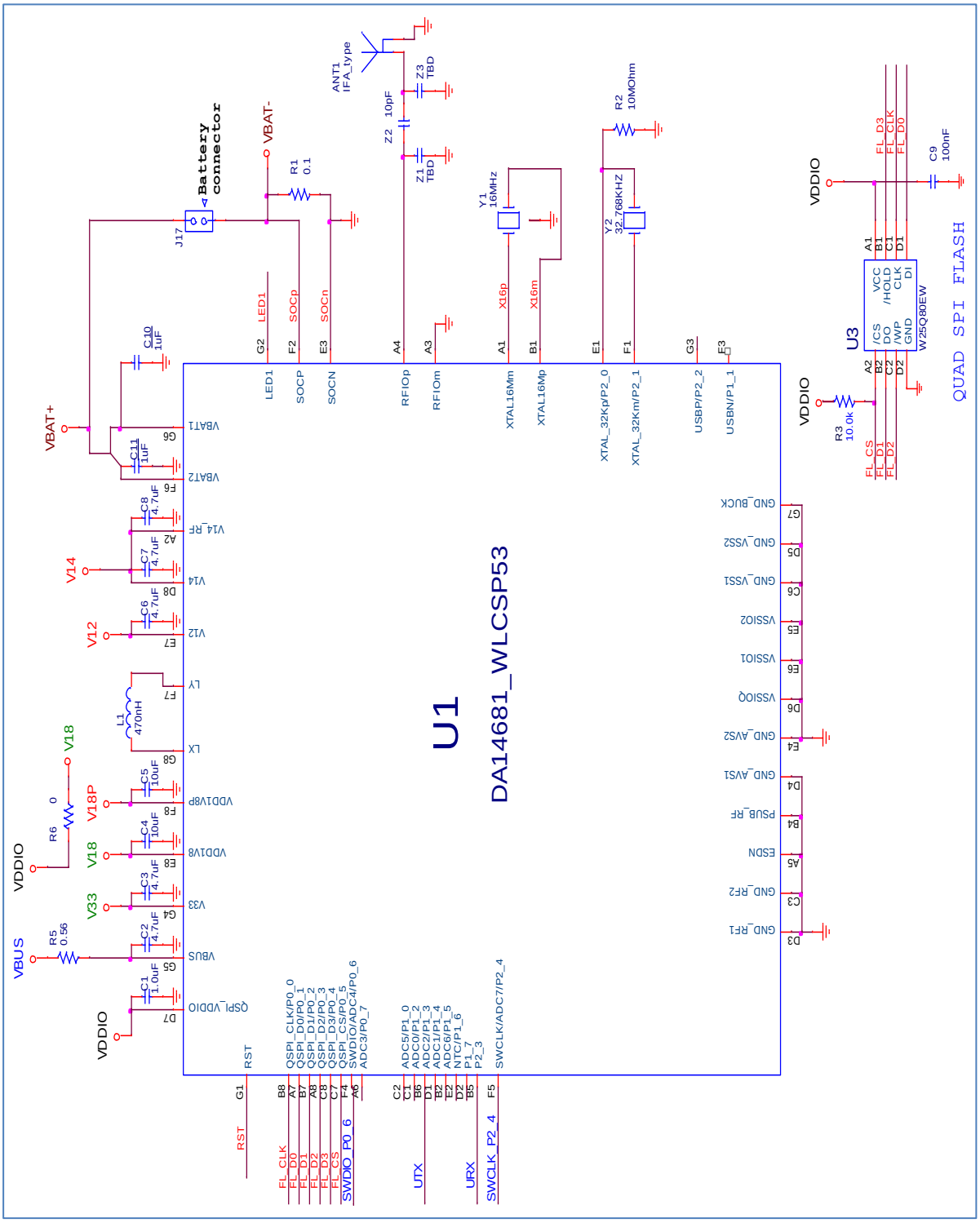


Figure 2: Minimal design for DA14681-01 WLCSP53 package

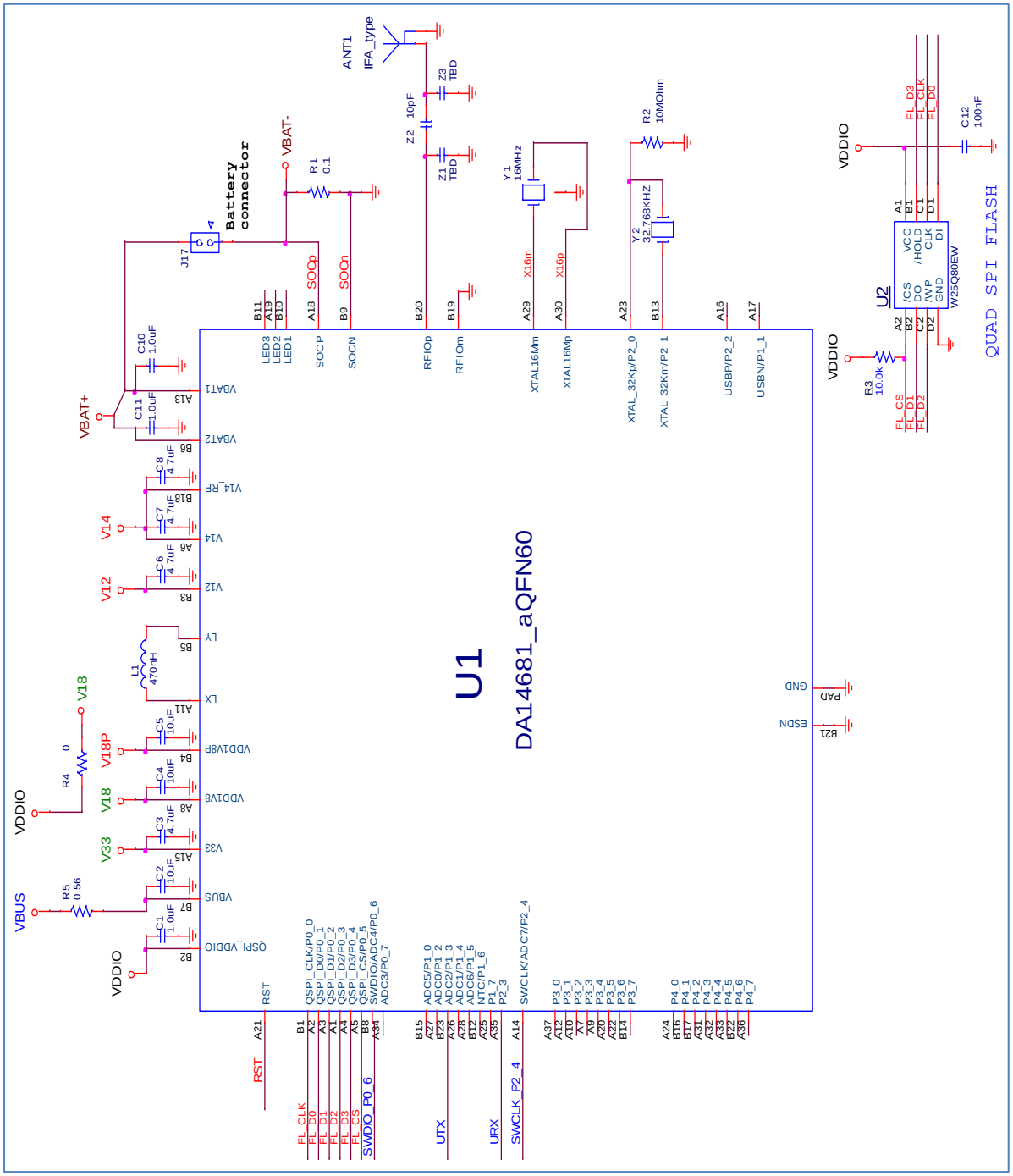


Figure 3: Minimal design for DA14681-01 AQFN60 package

Note: for the DA14680-01 (embedded flash), U2, R3, C12 are not present. And P0_0~P0_5 are N.C.

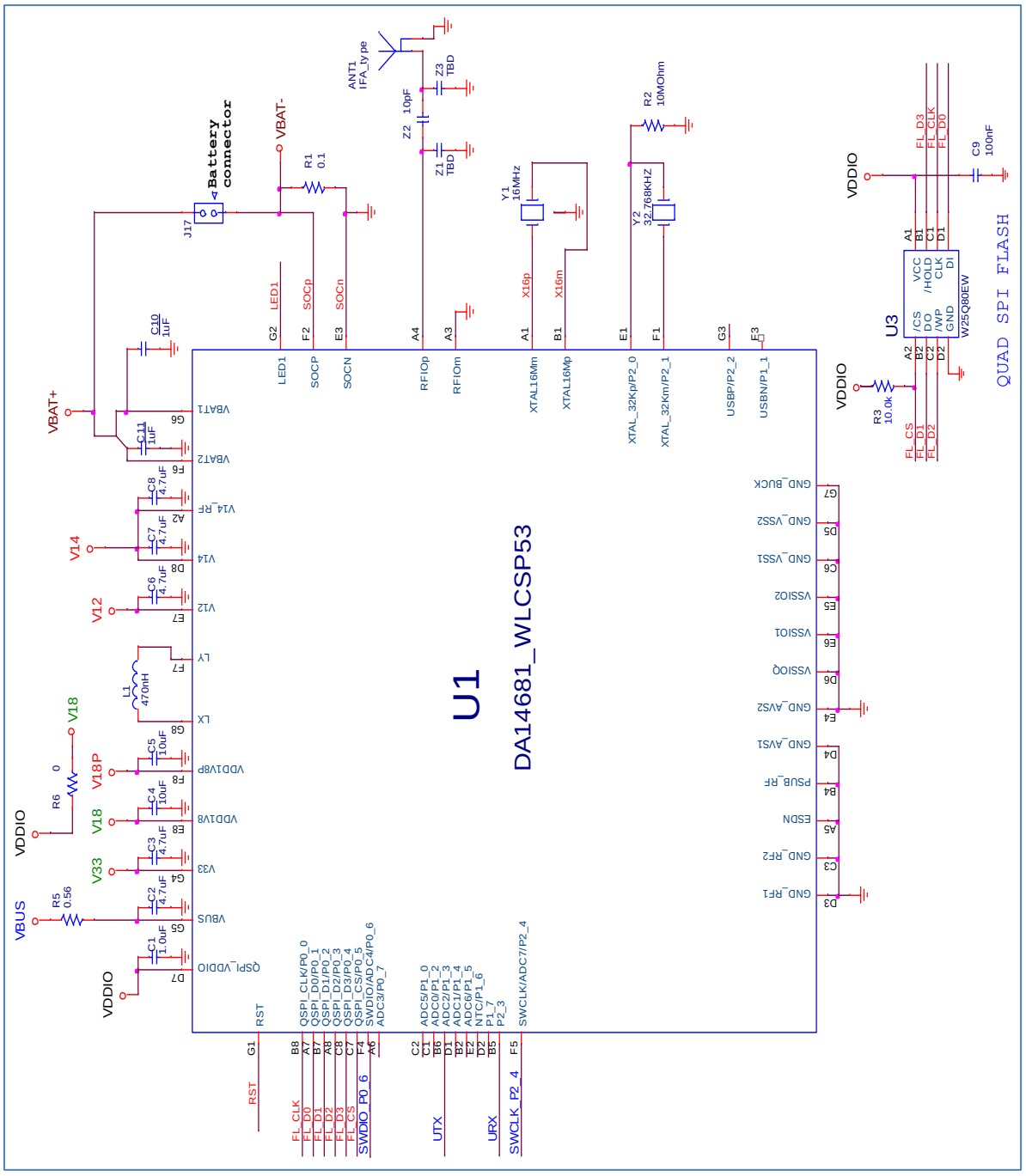


Figure 4: Minimal design for DA14683-00 WLCSP53 package

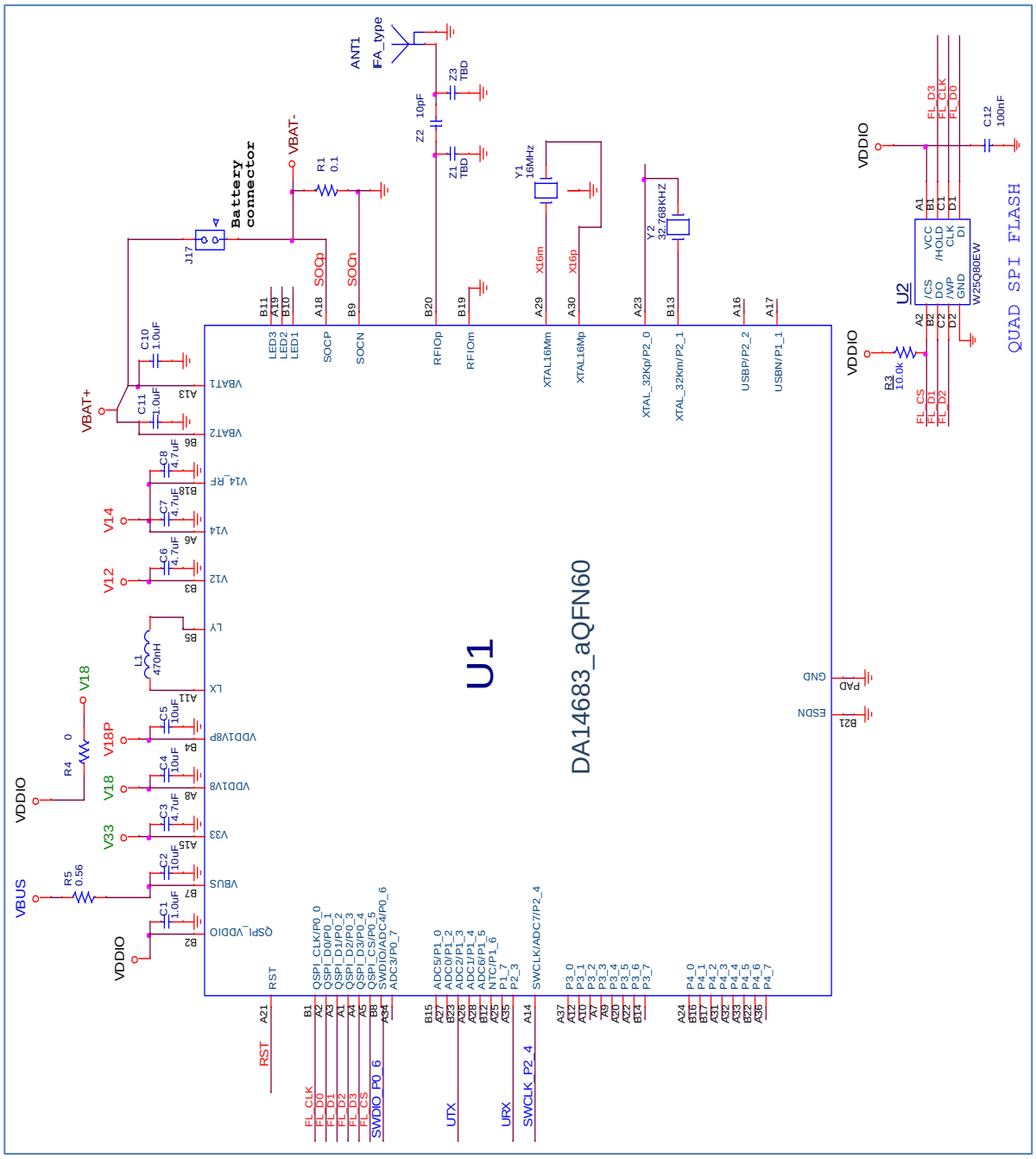


Figure 5: Minimal design for DA14683-00 AQFN60 package

Note: for the DA14682-01 (embedded flash), U2, R3, C12 are not present. And P0_0~P0_5 are N.C.

5.1 Power section of DA1468x

The DA1468x is supplied from a power source or battery connected to pin VBAT1 and VBAT2. The battery charging is accomplished by connecting an external +5V supply on the VBUS pin. The charging procedure is implemented in the software. When the +5V supply is connected, the DA1468x system operates with or without battery presence. The VBUS voltage range: 4.2V min. and 5.75V max.

The DA1468x SoC contains internally all power management for proper and safe system operation. Below the required external components are shown:

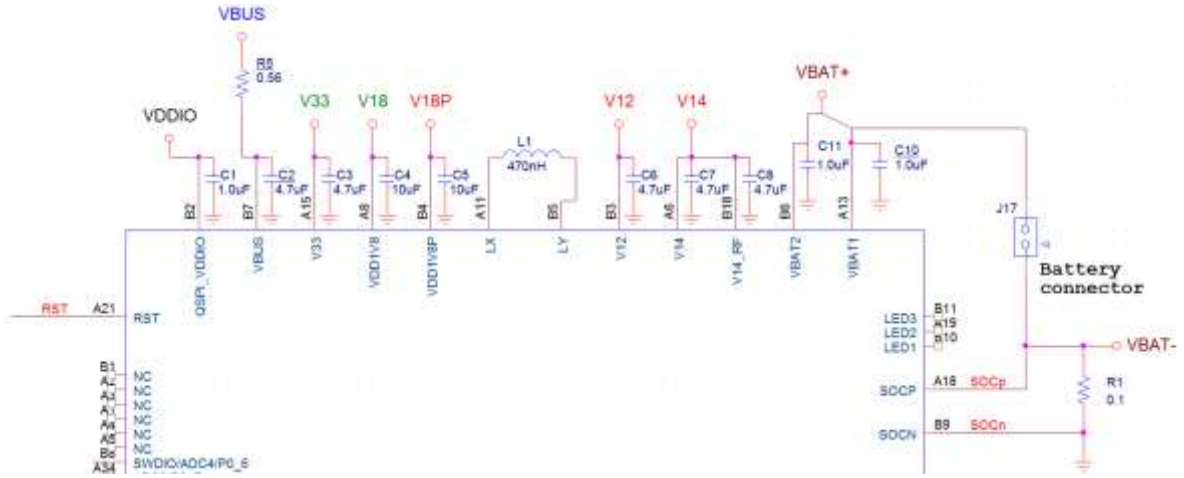


Figure 6: The power section of the DA1468x

VBUS: is the battery CCCV charger input as well as the USB bus voltage. It also supplies the 3.3V USB LDO providing power to the V33 rail. A decoupling capacitor equal to or less than 10 µF must be placed close to the VBUS pin. The absolute maximum allowed voltage for this pin is 6.5V.

It strongly advised to apply a 4.7 µF - 10V decoupling capacitor (C2: 0402 package) in combination with a 0.56 Ohm resistor (R5) in series with the VBUS pin. An alternative combination would be a 10 µF - 10V capacitor and a 0.39 Ohm resistor in series. Please refer to section 5.7.2.

VBAT1: the battery is connected to this pin and supplies the 3.3V VBAT LDO. A minimum value of 1µF for the decoupling capacitor (C10), is required close to the pin (0402 package, 10V). The voltage range for VBAT1 is 1.7V to 4.75V. The absolute maximum allowed voltage for this pin is 6V.

VBAT2: is the input supply pin for the SIMO DCDC converter. It is connected externally to VBAT1. As minimum, a 1 µF decoupling capacitor (C11), is required nearby the pin (0402 package, 10V).

V33: the 3.3V LDO output rail. Supplied by the VBAT1 or the VBUS pin. A ceramic decoupling capacitor of 4.7 µF (C3), should be added (0402 package, 6.3V). The V33 LDOs are capable to deliver up to 100 mA in active mode and up to 3 mA (DA14680/681) or 10 mA (DA14682/683) in sleep mode. The V33 rail cannot be turned off (it's required for e.g. the bandgap reference).

SIMO DC/DC converter outputs when active are: V18P, V18, V14 and V12. The inductor needed for DCDC operation is connected externally. The low RDC inductor (L1) of 470nH, size 0805 is connected to the LX/ LY pins.

V18 & V18P: these supply rails can deliver power to external devices, even when the system is in sleep mode. Decoupling ceramic capacitors (C4 & C5) of 10µF (0603 package, 16V) must be placed as close as possible to the V18 and V18P pins.
The V18 (VDD1V8) rail is assigned to supply the external QSPI Flash memory.
The V18P (VDD1V8P) rail is assigned to be used for supplying external devices like sensors or a RF power amplifier. The V18P supply rail is also used to supply the GPIOs when these are set to use the 1.8V supply. The current delivery capability of the V18 and V18P's rails in active mode is 75mA, whereas in sleep mode it is 3 mA (DA14680/681) or 10 mA (DA14682/683).
Please note that when not used, the V18 and V18P supply rails can be switched off completely.

V12: this power rail supplies the digital core of the DA1468x and delivers up to 50 mA at 1.2 V when in active mode. This rail should not be used for supplying external devices. A 4.7µF decoupling capacitor (C6), is required (0402 package, 10V).

V14: this output rail delivers up to 20 mA at 1.4V and should not be used for supplying other devices. A 4.7µF decoupling capacitor (C7), is required to be placed close to the V14 pin (0402 size, 10V).

V14_RF: the BLE radio supply input pin. It is connected to the V14 rail. The V14_RF supplies the internal RF circuits via a number of dedicated internal 1.2V LDOs. A 4.7µF decoupling capacitor (C8), is required, and should be placed as close to the V14_RF pin as possible. A good decoupling of this RF supply is important for a good and stable RF-performance (0402 package, 10V).

VDDIO: the Flash QSPI interface supply voltage. It connects to the supply rail used by the flash, normally V18. For the SoCs having the embedded flash memory, the VDDIO pin must be connected to V18. A 1µF decoupling capacitor (C1), needs to be placed at this pin (0402 package, 6.3V).

Note: The DA14682/683 chips have the capability to discharge both 1.8V rails and the 1.4V rail by a HW-Reset or by SW. Please refer to Section 5.1.2 or to the DA14682/683 datasheet [1] for details.

Table 5: Suggested decoupling capacitors for the power section

Reference	Description	Value	Package	Manufacturer Part Number
C1	CAP CER 6.3V 10% X5R	1.0 µF	0402	muRata GRM155R60J105KE19
C10, C11	CAP CER 10V 10% X5R	1.0 µF	0402	muRata GRM155R61A105KE5J
C3	CAP CER 6.3V 20% X5R	4.7 µF	0402	muRata GRM155R60J475ME47
C2, C6, C7, C8	CAP CER 10V 20% X5R	4.7 µF	0402	muRata ZRB15XR61A475ME01 or GRM155R61A475MEAA
C4, C5	CAP CER 16V 20% X5R	10 µF	0603	muRata GRM188R61C106MA73

Note: please consider 0603 size for C2, C10 and C11 for larger effective capacitance at 5V or 4V.

Table 6: SIMO DC/DC inductor examples and characteristics

Part Number	Taiyo Yuden CKP2012NR47M-T	Taiyo Yuden BRL2012TR47M6	SunLord MPM201206SR47	muRata DFE160808S-R47
Value	0.47 µH	0.47 µH	0.47 µH	0.47 µH
DC Resistance R_{DC}	0.08 Ω max	0.063 Ω max	0.086 Ω max	0.064 Ω max
Saturation Current	1.2 A	1.5 A	2.0 A	2.4 A
Size L x W x H (mm)	2.0 x 1.2 x 1.0	2.0 x 1.25 x 1.0	2.0 x 1.2 x 0.6	1.6 x 0.8 x 0.8

A 470nH power inductor is used for the SIMO DCDC converter. The DC resistance affects the efficiency as well as the ripple of the DCDC converter outputs. An inductor having a saturation current of at least 1A and a R_{DC} of maximum 0.1 Ohm guarantees a good performance. For the PRO-development kit, an inductor with saturation current of 1.2A and DC resistance of 0.06 Ohm is used.

The ceramic capacitors are placed as close as possible to the pins of the chip for reducing the parasitic inductance and improving the performance. Where it is available a small package (0402) was used. The capacitor values and working voltages have been selected for covering the capacitance de-rating phenomenon when a DC bias voltage is applied on the ceramic capacitor. The capacitance de-rating is highly dependent on the rated voltage, the technology (e.g. X5R vs. X7R) and the size of the multi-layer ceramic capacitor. In Figure 7, the capacitance de-rating for two different packages 0402 and 0603 of a 4.7µF/6.3V/X5R ceramic capacitor of Murata are presented. Quite a similar difference can be seen for 0402 sized 4.7µF/X5R capacitors, but having a rated voltage of 6.3V or 10V: the capacitance values at 5V are respectively 1µF and 2µF. To compensate or reduce the negative effect of this DC-bias derating, it is advised to either apply a larger size (0603 instead of 0402), a type having a higher rated voltage, e.g. 10V instead of 6.3V, or just a larger value.

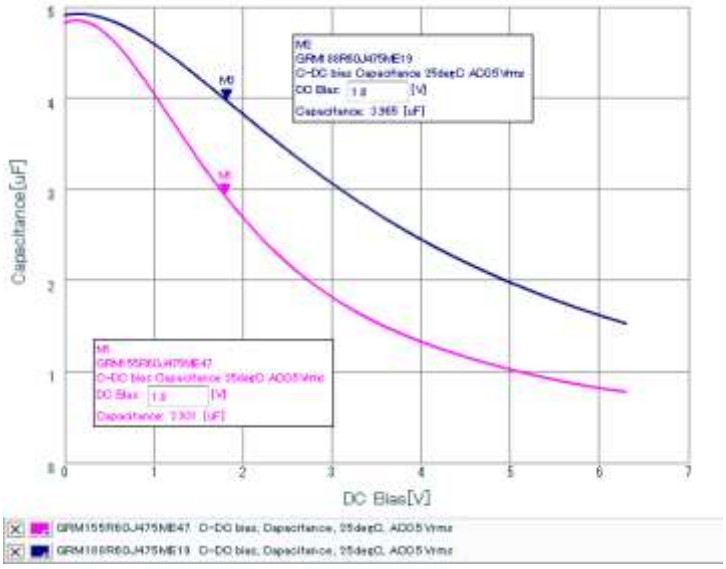


Figure 7: 4.7µF- 6.3V capacitance change for 0402 (purple) and 0603 (blue)

5.1.1 Supplying external loads

There are different ways to supply external loads from the DA1468x- SoC :

- V33 power rail. The V33 voltage is generated from VBUS or VBAT using the internal 3.3V LDOs. External loads up to 100 mA can be supplied by the V33 supply in active mode.
  The current capability of the V33 rail in sleep mode is 10 mA (DA14682/683).
  For the DA14680/681, the V33 rail current capability during sleep is less: 3mA.
- V18 and V18P power rail: the V18 (VDD1V8) rail is used for supplying the QSPI flash memory. The V18P (VDD1V8P) rail is used to supply peripherals like sensors.
  The current capability of these rails is 75 mA in active mode and 10 mA in sleep mode.
  With the DA14680/681 chips, the current capability of the two 1.8V rails during sleep is 3 mA.
- The GPIOs supply-rail can be configured to 1.8V or 3.3V. When set to 1.8V, the GPIO is supplied from V18P, VDD1V8P. Whereas for 3.3V it is supplied from the 3.3V LDO, V33. Refer to Figure 8.

  The GPIO's output current capability is 4.8 mA. The GPIO supply power delivered to the load needs to be taken into consideration into the power budget of the total system. The GPIOs can be used for supplying light loads, e.g. a LED, NTC resistor network or a low-power sensor. The maximum source or sink current per GPIO is 4.8 mA. The system designer must take into consideration the current capability of the voltage rails that supplies the GPIOs during sleep mode.

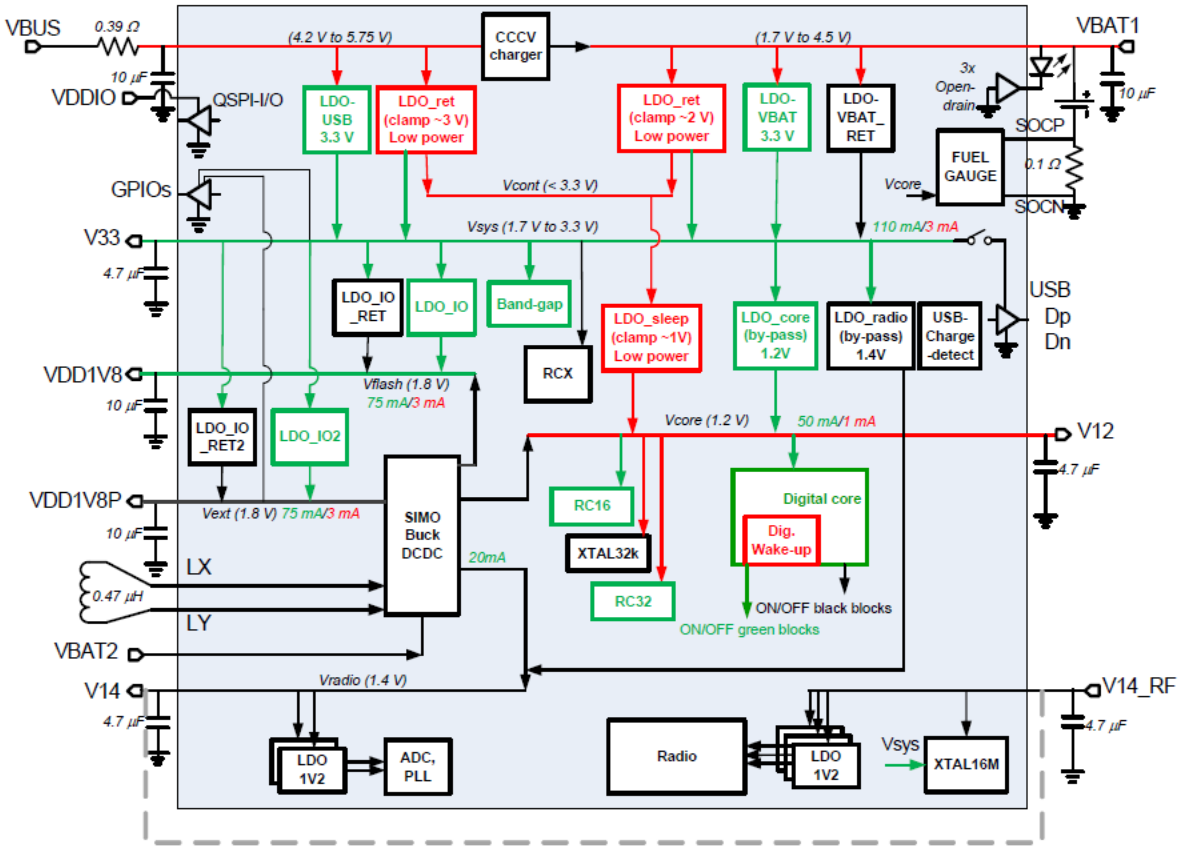


Figure 8: DA1468x power management unit block diagram

Always on | Hardware enabled | Software Enabled

Table 7: DA1468x supply rail capabilities overview

Supply rails	DA14680/681	DA14682/683
V18 / V18P active	75 mA	75 mA
V18 / V18P sleep	3 mA	10 mA
V33 active	100 mA	100 mA
V33 sleep	3 mA	10 mA

5.1.2 Supply rails discharging

Device:	DA14680	DA14681	DA14682	DA14683
Rail discharging	✗	✗	✓	✓

The DA14682/683 chips have the capability to discharge both 1.8V rails and the 1.4V rail by a HW-

Reset (PMU_RESET_RAIL_REG) or by SW (DISCHARGE_RAIL_REG). The DA14680/681 chips don't possess this function.
Below Figure 9 shows the rails being discharged by a HW-Reset. The whole discharge – charge cycle takes about 4 msec. Figure 10 shows the FSM timing diagram. For details about the rail discharging functionality, please refer to the 'Rails Discharging' section of the 'Reset and BOD' chapter in the DA14682 and the DA14683 datasheet.

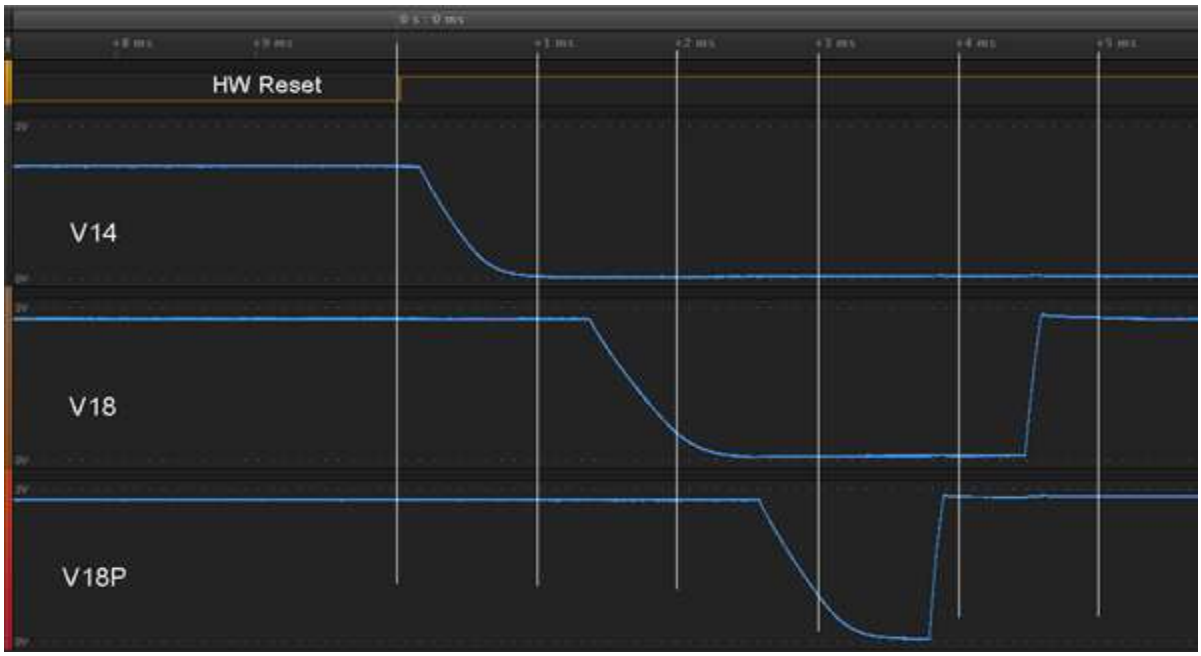


Figure 9: V14, V18, V18P rails discharging by HW Reset

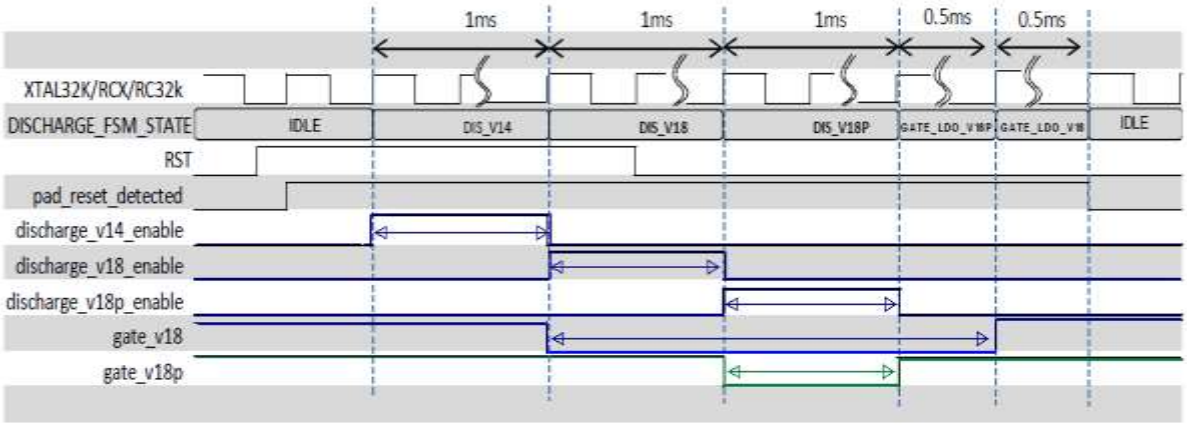


Figure 10: Discharging rails FSM timing

5.1.3 SIMO Buck DC/DC Characteristics

The general properties of the DA1468x Buck DC/DC converter:

DC/DC type:	Single Inductor Multiple Outputs (SIMO)
Operation mode:	Discontinuous Conduction Mode (DCM)
Reference voltage:	1.20 V
Switching Frequency:	2 MHz typically, depends on the loads
Inductor ripple current:	1 A maximum, depends on the loads
FET switches On resistance:	0.5 Ohm nominal
Start-Up time:	10 µsec typical

The DA1468x buck DC/DC Converter is tailored for the DA1468x application and works different from most stand-alone buck DC/DC converters that use Continuous Conduction Mode (CCM) and have either voltage- or current feedback. Instead, in the DA1468x buck DC/DC each rail has its own comparator. Please refer to Figure 11 below.
If the output voltage of a rail is too low, a charge cycle is triggered. Additionally, the rails are not charged in a fixed sequence, the sequence dynamically can be changed depending on the rail priority. The converter tries to charge each output every 2 µsec, and since there are four outputs there's one pulse every 0.5 µsec, leading to a typical switching frequency of 2 MHz.

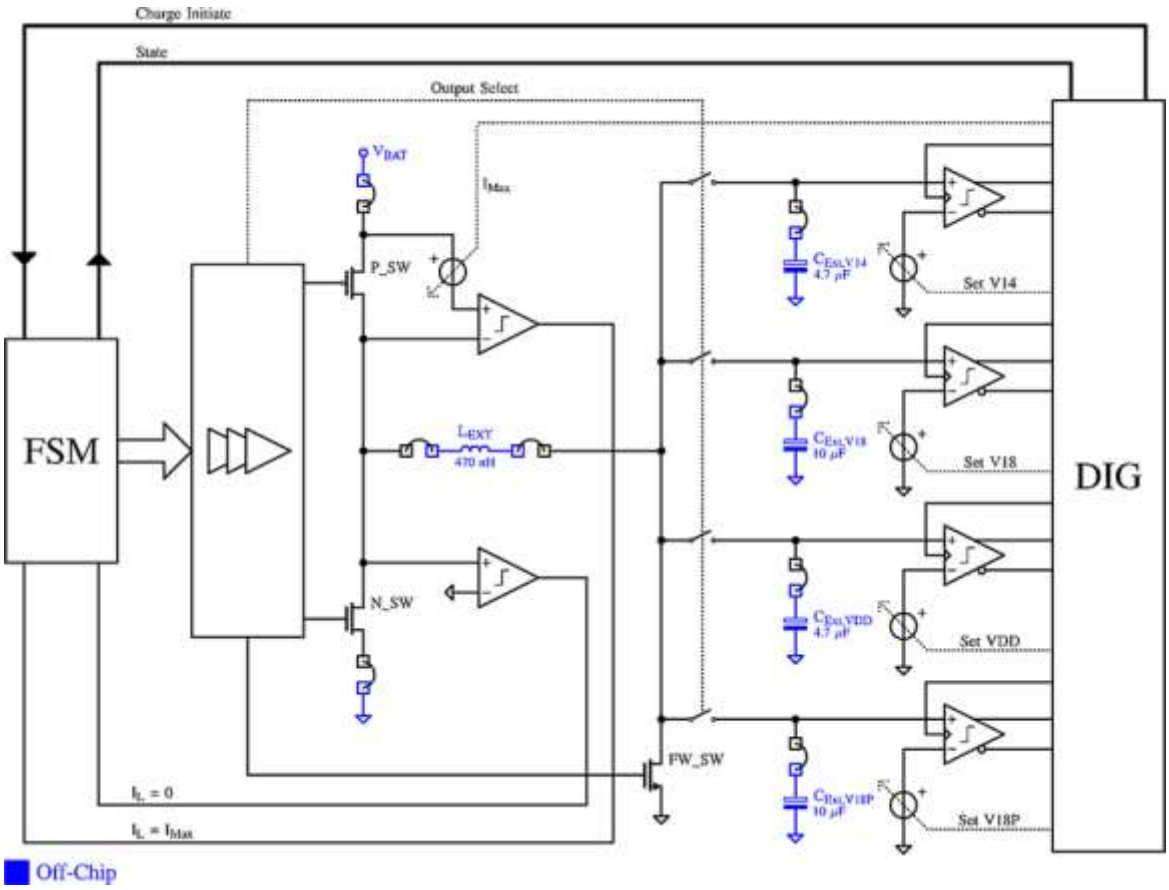


Figure 11: SIMO BUCK DC/DC Block Diagram

It does this by measuring the time between pulses and adjusting the inductor current limit to keep

the rail voltage within certain limits. However, since there is a minimum current limit there is a point where it cannot regulate lower and the frequency will have to decrease. Likewise, if the current is at its maximum and the load is increased further there comes a point where the frequency has to increase in order to deliver enough charge. The highest frequency is expected to stay below 4 MHz.

The DCM operation mode leads to a DC/DC inductor (ripple) current that switches from 0 A to the maximum current, which is 1 A maximum for the 1.8 V rails, and about 400 mA for the 1.2 V and 1.4 V rails. This sets the requirement for the saturation current of the DC/DC inductor: 1 A minimum.

The DC/DC inductor was chosen as a compromise between switching frequency and voltage ripple:

- Switching frequency: a smaller inductance results in a faster build-up of inductor current and means that for a given current limit less charge is dumped in the capacitor per cycle so a higher frequency is required.
- Voltage ripple: a bigger inductance means more charge is delivered per cycle means higher ripple. There are many optimizations possible here, but a 470 nH inductor seemed most suited for the buck DC/DC in the DA1468x application.

The buck DC/DC takes about 10 µs to start up when its enable signal is set. It then immediately starts supplying the outputs, the L-C values are of no importance for that.
The DC/DC's dynamic behaviour, overshoot, undershoot, etc.is a bit more difficult to describe mathematically than for a current or voltage feedback converter. As mentioned, the DA1468x buck DC/DC converter uses a different mechanism to regulate the outputs.
In short: it samples all four outputs and will start a charge cycle if it finds one or more are too low, it then measures how long it takes until a new cycle is required and adjusts the current limit to try and keep this time constant. Because of this mechanism, it takes several cycles to get to the new current limit when a load step is presented at an output, meaning it will be a bit slower than a converter with a proportional feedback path. It also means the voltage transient at one output depends on the load on all other outputs, since only one output can be active at any given time.
In general the buck DC/DC inductor value (470 nH) is pretty optimal for the DA1468x design, and increasing the output capacitor values will reduce the voltage ripple and the magnitude of the load transients.

5.2 I/O pins

The DA1468x has software-configurable I/O pin assignment, organized into ports Port 0, Port1, Port2 Port 3 and Port 4. Only ports 0, 1 and 2 are available for the WLCSP53 package. All ports are available in the AQFN60 package. Very useful, for system design characteristics for the I/O pins operation are:

- Fully programmable pin assignment:
  Pxy_MODE_REGs provide, (through PID) a multiplexing function to the IOs of the on-chip peripherals as well as the direction of the pin. A pin can be assigned to a general purpose port (PID=00), to UART, to other serial interfaces or PWM output.

- Selectable 25 KOhm pull-up or pull-down resistors per pin.
- GPIOs can be configured individually as 1.8V or 3.3V. The 1.8V is provided by V18P.
- Programmable open-drain functionality.
- Fixed assignment for analog pins ADC[7:0], QSPI, JTAG, USB and NTC.
- Pins retain their last state when system enters the Sleep or Deep Sleep mode.
- P0_6 is kept powered while in sleep/deep-sleep mode, controlled by Timer1 PWM5 signal.

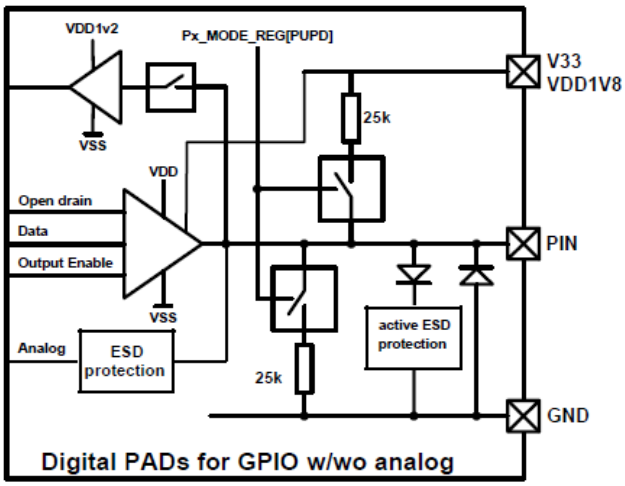


Figure 12: PAD I/O configuration

NOTES

Please observe the following guidelines when using the GPIOs:

- To use P1_1 in GPIO mode, USBPAD_REG[USBPAD_EN] must be set.
- To use P2_2 in GPIO mode, USBPAD_REG[USBPAD_EN] must be set
- On all DA1468x SoCs, P1_1 and P2_2 (USB pad by default) cannot be configured as generic GPIO output mode if they need to be kept active in sleep mode. In sleep mode these pins go to High-Z (reset state). For this reason P1_1 and P2_2 must not be used for supplying purposes. And use these GPIOs with 3.3V supply only.
- P1_0 and P1_5 will affect the radio performance and PLL96M stability when toggling quickly. It is recommended to toggle these pins at a low rate only and not at all while the radio is active or the PLL96M is used.

5.3 Crystals and clocks

The DA1468x SoC is equipped with two Digitally Controlled Crystal Oscillators (DXCO), one at 16 MHz or 32 MHz (XTAL16M/XTAL32M), and a second at 32.768 KHz (XTAL32K).
The 32.768 KHz crystal oscillator has no trimming capabilities and can be used as the low power clock for the Extended/Deep Sleep modes.
The 16 MHz/32 MHz crystal oscillator can be trimmed using the internal capacitor bank. The allowed load-capacitance of the crystal ranges from 4 pF to 12 pF.

5.3.1 16 MHz and 32 MHz clock

Device:	DA14680	DA14681	DA14682	DA14683
16 MHz crystal	✓	✓	✓	✓
32 MHz crystal	✗	✗	✓	✓

The DA1468x requires an accurate clock for a proper operation. The clock can be generated either by using an external 16 MHz or 32 MHz crystal, or by applying an external 16 MHz clock signal.

The 16/32 MHz crystal oscillator can be trimmed. No external components are required other than the crystal itself. If the crystal has a case connection, it is advised to connect the case to ground.
Register CLK_FREQ_TRIM_REG controls the trimming of the 16/32 MHz crystal oscillator.
Usage of a 32 MHz crystal is only supported by the DA14682 and the DA14683 versions of the chip, not by the DA14680 and DA14681 chip versions.

The crystal or the external clock must meet the 16 MHz or 32 MHz crystal oscillator recommended operating conditions as listed below in below tables.

Parameter	Description	Conditions	Min	Typ	Max	Unit
$f_{XTAL}(16M)$	crystal oscillator frequency			16		MHz
ESR(16M)	equivalent series resistance				100	Ω
$C_L(16M)$	load capacitance	No external capacitors are required.	4	10	12	pF
$C_0(16M)$	shunt capacitance	No external capacitors are required.			5	pF
$\Delta f_{XTAL}(16M)$	crystal frequency tolerance	After optional trimming; including aging and temperature drift (Note 21)	-20		20	ppm

Parameter	Description	Conditions	Min	Typ	Max	Unit
$\Delta f_{XTAL(16M)UNT}$	crystal frequency tolerance	Untrimmed; including aging and temperature drift **(Note 22)**	-40		40	ppm
$P_{DRV(MAX)(16M)}$	maximum drive power	**(Note 23)**	100			µW
$V_{CLK(EXT)(16M)}$	external clock voltage	In case of external clock source on XTAL16Mp (XTAL16Mm floating or connected to mid-level 0.6 V)	1	1.2		V
$\varphi_{N(EXTERNAL)16M}$	phase noise	f_C = 50 kHz; in case of external clock source			-130	dBc/Hz

Note 21: Using the internal varicaps a wide range of crystals can be trimmed to the required tolerance.
Note 22: Maximum allowed frequency tolerance for compensation by the internal varicap trimming mechanism.
Note 23: Select a crystal which can handle a drive level of at least this specification.

Parameter	Description	Conditions	Min	Typ	Max	Unit
$f_{XTAL}(32M)$	crystal oscillator frequency			32		MHz
ESR(32M)	equivalent series resistance				60	Ω
$C_L(32M)$	load capacitance	No external capacitors are required	4	6	12	pF
$C_0(32M)$	shunt capacitance				5	pF

Figure 13: 16 MHz or 32 MHz crystal oscillator, recommended operating conditions

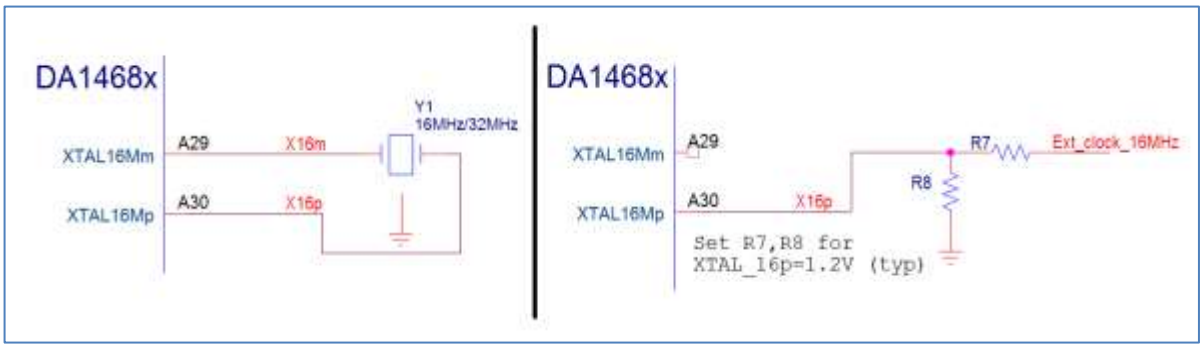


Figure 14: Connection of the crystal (left) and external 16 MHz clock (right) for AQFN package

In Table 8 and in Table 9 below there are examples of some 16 MHz and 32 MHz crystals that meet the specification described above in Figure 13.

Table 8: 16 MHz crystal examples and characteristics

Part Number	TXC 8Y16070015	River Eletec FCX-06 LF 16.000 MHz	Kyocera CX2016DB16000F0FLLC1	NDK NX2520SA	TXC 7M16070029
Frequency	16.000 MHz	16.000 MHz	16.000 MHz	16.000 MHz	16.000 MHz
Accuracy (please check for other possible types)	±10 ppm	±10 ppm	±10 ppm	±10 ppm	±10 ppm
Load Capacitance (C_L)	10 pF	10 pF	10 pF	10 pF	10 pF
Shunt Capacitance (C_0)	2 pF max.	0.5 pF typ.	0.6 pF typ.	0.7 pF typ.	3 pF max.
Equivalent Series Resistance (ESR)	100 Ω max.	80 Ω max.	100 Ω max.	80 Ω max.	50 Ω max.
Drive Level (P_D)	100 µW	< 200 µW	100 µW	100 µW	100 µW
Size L x W x H (mm)	2.0 x 1.6 x 0.5	2.0 x 1.6 x 0.5	2.0 x 1.6 x 0.45	2.5 x 2.0 x 0.5	3.2 x 2.5 x 0.7

Table 9: 32 MHz crystal examples and characteristics

Part Number	River Eletec FCX-06 32000	Kyocera CX2016DB32000	NDK NX2016SA 32000	EPSON FA-128 2016	TXC 8Q32070005
Frequency	32.000 MHz	32.000 MHz	32.000 MHz	32.000 MHz	32.000 MHz
Accuracy (please check for other possible types)	±10 ppm	±10 ppm	±20 ppm	±10 ppm	±10 ppm
Load Capacitance (C_L)	5 pF	8 ~ 11 pF	6.5 ~ 8 pF	6 ~ 8 pF	6 pF
Shunt Capacitance (C_0)	0.64 pF typ.	?	0.6 pF typ.	< 3 pF	-
Equivalent Series Resistance (ESR)	60 Ω max.	60 Ω max.	60 Ω max.	60 Ω max.	60 Ω max.
Drive Level (P_D)	100 µW	100 µW	< 200 µW	100 µW	100 µW
Size L x W x H (mm)	2.0 x 1.6 x 0.5	2.0 x 1.6 x 0.4	2.0 x 1.6 x 0.45	2.0 x 1.6 x 0.5	1.6 x 1.2 x 0.35

5.3.2 32.768 KHz clock

Device:	DA14680	DA14681	DA14682	DA14683
10 MOhm at XTAL32Kp required?	✓	✓	✗	✗

The DA1468x utilizes a low power, low frequency clock for extended and deep sleep modes. This can be achieved with either the 32.768 KHz crystal oscillator (using an external 32.768 KHz crystal) or the internal RCX oscillator. When using the RCX oscillator, no crystal is needed. The utilization of the external crystal provides a tighter timing, better accuracy, but adds the cost of the crystal. This crystal oscillator cannot be trimmed. The DA1468x offers a load-capacitance of 7 pF, and typically no external load capacitors are required. The DA14680 and DA14681 chips require a 10 MOhm resistor from the XTAL32Kp pin to ground, the DA14682 and DA14683 do not need this. The external crystal must meet the recommended operating conditions as indicated below:

Parameter	Description	Conditions	Min	Typ	Max	Unit
$f_{CLK\_EXT\_32K}$	external clock frequency	at pin XTAL32KP/P2_0 in GPIO mode	10		100	kHz
$V_{CLK\_EXT\_32K}$	external clock voltage	at pin XTAL32KP/P2_0 in GPIO mode	1	1.2		V
f_{XTAL_32K}	crystal oscillator frequency		30	32.768	35	kHz
ESR_{32K}	equivalent series resistance				100	kΩ
C_{L_32K}	load capacitance	No external capacitors are required for a 6 pF or 7 pF crystal.	6	7	9	pF
C_{0_32K}	shunt capacitance			1	2	pF
Δf_{XTAL_32K}	crystal frequency tolerance (including aging)	Timing accuracy is dominated by crystal accuracy. A much smaller value is preferred.	-250		250	ppm
$P_{DRV\_MAX\_32K}$	maximum drive power	**(Note 27)**	0.1			µW

Note 27: Select a crystal that can handle a drive level of at least this specification.

Figure 15: 32.768 KHz crystal oscillator, recommended operating conditions

In Table 10, there are examples of crystals that meet the specification described above.

Table 10: 32.768 KHz crystal examples and characteristics

Part Number	Abracon ABS07-32.768KHZ-7-T	Abracon ABS06-32.768kHz-7-T	NDK NX3215SA-32.768K-STD-MUA-14	ECS Inc. ECX-12_32.768KHz	Hosonic ETDG003270003E
Frequency	32.768 KHz	32.768 KHz	32.768 KHz	32.768 KHz	32.768 KHz
Accuracy	± 20 ppm	± 20 ppm	± 20 ppm	± 20 ppm	± 20 ppm
Load Capacitance (C_L)	7 pF	7 pF	6 pF	7 pF	7 pF
Shunt Capacitance (C_0)	0.9~1.2 pF	1.5 pF	1.5 pF max.	1.3 pF	1.0 pF
Equivalent Series Resistance (ESR)	70 KΩ max.	90 KΩ max.	70 KΩ max.	90 KΩ max.	90 KΩ max.
Drive Level (P_D)	< 0.5 µW	< 0.5 µW	< 0.5 µW	< 0.5 µW	< 0.5 µW
Size L x W x H (mm)	3.2 x 1.5 x 0.9	2.0 x 1.2 x 0.6	3.2 x 1.5 x 0.8	2.0 x 1.2 x 0.6	2.0 x 1.2 x 0.6

For applying a 32.768 KHz square wave clock signal having an amplitude of 1.8Vpp from an external source (e.g. MCU) to the P2_0 pin of the DA1468x, the following procedure needs to be applied:

- XTAL32K oscillator must be disabled by applying:

  CLK_32K_REG [XTAL32K_ENABLE] = 0x0
- CLK32K_SOURCE must be set to select external clock signal:

CLK_CTRL_REG [CLK32K_SOURCE] = 0x3

- P2_0 must be set into GPIO function:

  P20_MODE_REG [PID] =0x0

- Direction of the pin must be input:

  P20_MODE_REG [PUPD] =0x0

5.3.3 Generating a clock output from the DA1468x

The DA1468x SoC can output one clock signal at a time, the output GPIO selection is flexible. Assuming we want to output the 16 MHz clock at GPIO P1_0, following must be set:

- P10_MODE_REG: PUPD set to 0x3 - Set P1_0 as Output
- P10_MODE_REG: PID set to 0x34 (52) for CLOCK.
- GPIO_CLK_SEL: FUNC_CLOCK_SEL set to 0x3 for the 16MHz Xtal clock.

Please find below the tables showing the P1_0 register settings: P10_MODE_REG (0x5000302E), and GPIO Clock Selection: FUNC_CLOCK_SEL (0x500030D0).

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x0
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, Pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
7:6	-	-	Reserved	0x0

Bit	Mode	Symbol	Description	Reset
5:0	R/W	PID (continued)	48: COEX_EXT_ACT0 49: COEX_EXT_ACT1 50: COEX_SMART_ACT 51: COEX_SMART_PRI 52: CLOCK 53: ONESHOT 54: PWM5 55: PORT0_DCF 56: PORT1_DCF 57: PORT2_DCF 58: PORT3_DCF 59: PORT4_DCF 60: RF_ANT_TRIM[0] 61: RF_ANT_TRIM[1] 62: RF_ANT_TRIM[2]	0x0

Figure 16: Clock output, P10_MODE_REG - PUPD and PID selection

GPIO_CLK_SEL (0x500030D0)

Bit	Mode	Symbol	Description	Reset
15:3	-	-	Reserved	0x0
2:0	R/W	FUNC_CLOCK_SEL	Select which clock to map when PID = FUNC_CLOCK. 0x0: XTAL32K 0x1: RC32K 0x2: RCX32K 0x3: XTAL16M 0x4: RC16M 0x5: DIVN	0x0

Figure 17: Clock output, GPIO_CLK_SEL - FUNC_CLK_SEL, clock selection

5.4 UART

The UART section consists of the UTX and URX signals, which by default are assigned to the P1_3 and the P2_3 GPIOs pins respectively. The baud rate of this pair during booting is set to 57.6 Kbd. Using other UART boot pairs is possible, e.g. P1_0/P1_5 or P1_2/P1_4 both @ 57.6 Kbd [4]

Note: the P0 serial boot ports mentioned in AN-B-046 [4] cannot be used when a QSPI Flash memory is used. The QSPI interface uses GPIOs P0_0 thru P0_5.

Table 11: Default UART pins

	Function	Pin name	AQFN60 Pin	WLCSP Pin
UART	UART transmit (UTX)	P1_3	B23	B6
	UART receive (URX)	P2_3	A35	B5

5.5 SWD (JTAG)

P0_6 and P2_4 are assigned to the SWDIO and SWCLK signals respectively.
P0_6 and P2_4 can be used as GPIOs when they will not be used as SWD (serial wire debugging) interface.

Table 12: JTAG pins

	Function	Pin name	AQFN60 Pin	WLCSP Pin
JTAG	JTAG data (SWDIO)	P0_6	B8	F4
	JTAG clock (SWCLK)	P2_4	A14	F5

5.6 QSPI Flash memory

Device:	DA14680	DA14681	DA14682	DA14683
Embedded QSPI Flash	✓	✗	✓	✗

The DA14680/682 chip versions contain an embedded low power 8Mbit QSPI flash, which is used to directly execute code from it (using the CPU cache) or mirror the contents from it into the SysRAM.
Please note that for these DA14680/682 chips, the corresponding six QSPI signals are not connected to pins P0_0 thru P0_5.
The VDDIO pin though, needs to be connected to the 1.8V power supply, which is the DA14680/682's V18 rail.

The DA14681/683 SoCs can use an external low power Quad-SPI FLASH.
The recommended part, also used on the PRO development kit, is the W25Q80EW (8Mbit) QSPI flash memory, WLCSP package. This is a power efficient QSPI flash having a supply voltage of 1.8V.
As the maximum operating frequency of the QSPI interface is 96 MHz, for achieving the best performance, a suitable QSPI Flash memory that can operate at this clock frequency is strongly suggested.

For avoiding signal integrity issues, keep the distance between the processor and the flash memory as short as possible. If needed, apply 47Ω to 56Ω termination series resistors in all six QSPI lines. The in Figure 3 and in Figure 4 indicated 10K pull-up resistor at the QSPI Flash CS pin is not mandatory, the DA14681/683 QSPI_CS port will also pull the CS line high.

5.7 USB and VBUS

The USB interface is an integrated USB controller compatible with the USB 1.1 FS specification.
It's advised not to apply series termination resistors in the DA1468x USBP and USBN data lines like commonly done, the DA1468x doesn't need these resistors and they will negatively affect the USB's signal integrity, deteriorating the rise- and fall-times too much when using longer USB cables.
The USB transceiver module is accessed through the USBP (D+) and USBN (D-) signals which are multiplexed with the P2_2 and P1_1 GPIOs respectively. It is important to configure P1_1 and P2_2 as USB pins before the USB block is enabled, or USB block may be damaged if voltage applied to the pins (when they are configured as GPIOs). For using P1_1 and P2_2 in GPIO mode, USBPAD_REG [USBPAD_EN] must be set.

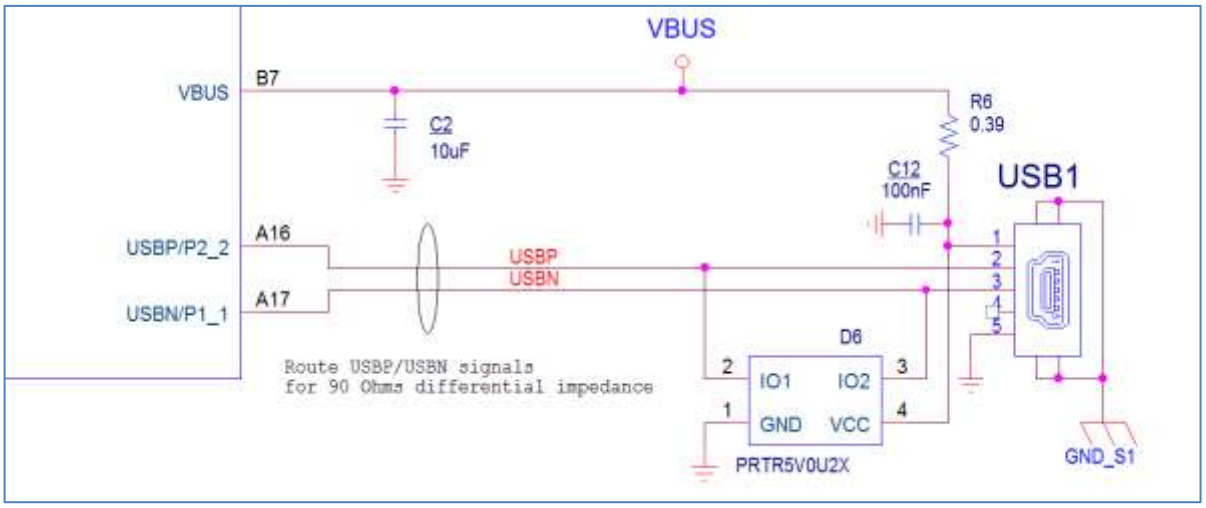


Figure 18: Recommended topology for USB functionality

5.7.1 USB ESD measures

In Figure 18, a recommended configuration is illustrated, and an ESD protection circuit like the ESD diode PRTR5V0U2X must be in place for ESD protection of the USB lines.
In case USB functionality is not required but charging functionality is wished, charger contact pins can be applied in the application for instance to provide +5 V to the VBUS pin of the DA1468x device.
For ESD reasons, make sure an ESD protection device is applied directly between the two charger pins.
The ESD diode at the +5 V VBUS supply should have a high enough reverse stand-off voltage or maximum reverse working voltage to make sure it's not conducting at expected and allowed VBUS voltages: e.g. 5.75 V.
Please make sure to have a short and solid ground connection, having a low impedance, to the ground terminal of the ESD protection device. Please read also section 5.9 for layout related ESD topics.

5.7.2 VBUS circuitry.

The suggested VBUS R-C filter circuit, consisting of R6 and C2, is explained here. The USB port is used for the charger supply and the USB cable provides power to the VBUS pin of the DA1468x SoC. The USB cable exhibits mainly an inductor L, and its value is related to the length of the cable. At the VBUS pin of the DA1468x chip, there is a ceramic supply decoupling capacitor (C2). When the USB cable is plugged-in at the connector, there is a step-voltage applied to the LC series resonator. Depending on the quality of this resonator, a voltage of twice the initial USB voltage can be present on this VBUS pin (2 x 5V = 10V). **This can result in damaging the circuits inside the DA14680 and must therefore be avoided !**

A way of protecting the DA1468x against high peak voltages during USB-cable insertion is to lower the Q factor of the resonator circuit by adding a series resistor in the line: R6.
This series resistor increases the “Damping” of the LC circuit. For an L-C series circuit the damping is defined as: $Damping = \frac{R6}{2}\ x\ \sqrt{\frac{C2}{L}}$

It is beneficial to have a large capacitor on the VBUS pin. A larger capacitor value results in a lower value of the series resistor when a certain amount of damping is required.

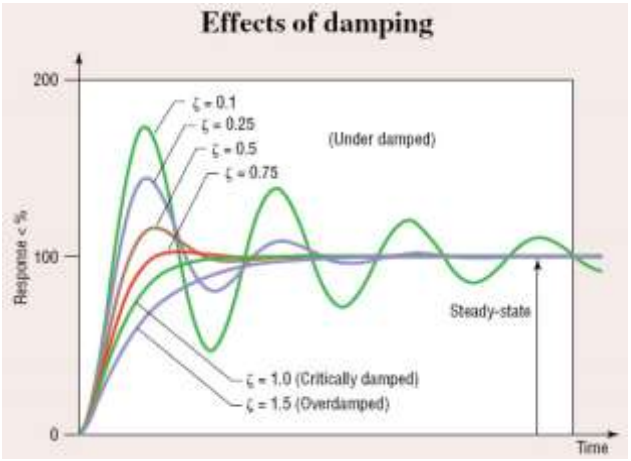


Figure 19: Relation between damping and step-response of a series LC resonator

When the inductance has increased because of a longer cable and the series resistance is not adapted, the step-response will show more ringing (with a higher amplitude). Next plots are taken from a system with sufficient damping for a 60 cm cable connection, whereas, when the length of the cable is increased to 150 cm, the damping reduces leading to larger voltage overshoots.

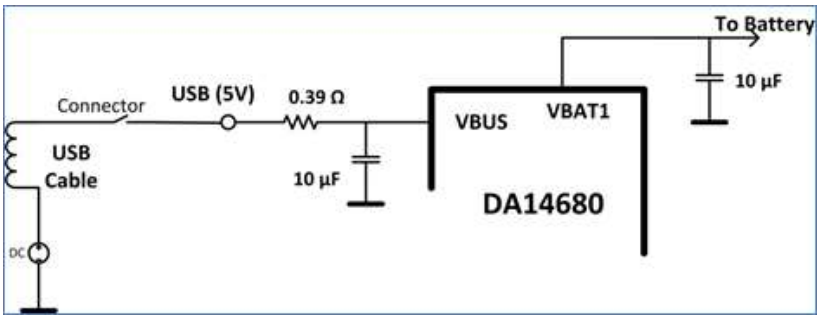


Figure 20: Used USB circuit for testing

The pink coloured traces show the VBUS voltage, the blue traces show the VBUS current.

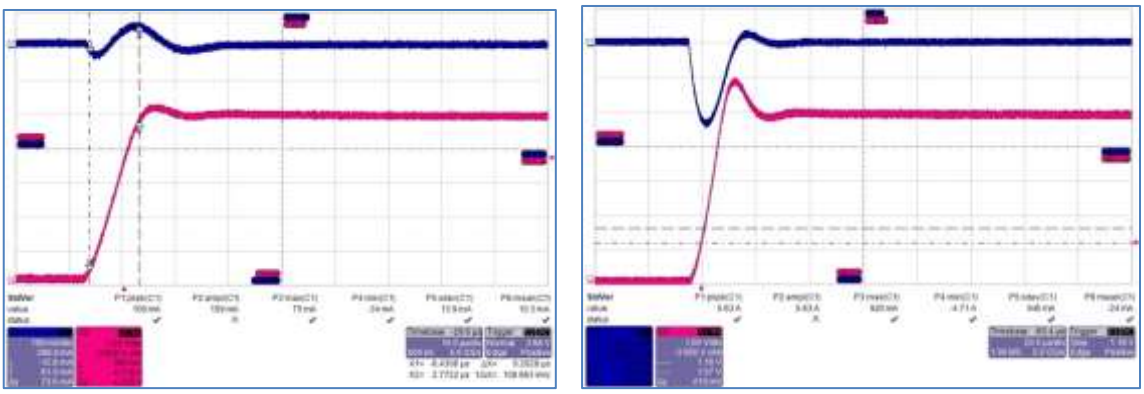


Figure 21: Step response with 60 cm (left) and 150 cm (right) cable (non USB-cable). A damping network of 0.39 Ω and 10 µF capacitor on VBUS is used.

For a longer cable length (300 cm), the ringing (and overshoot) gets worse:

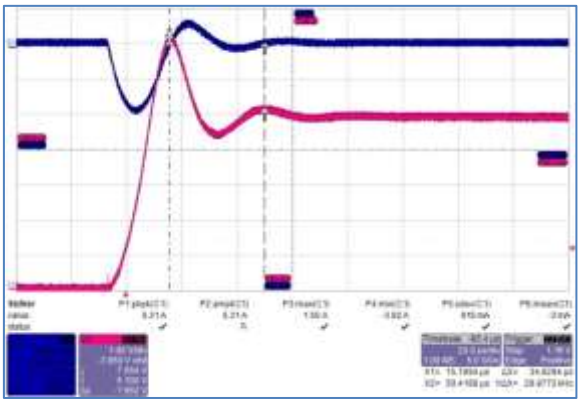


Figure 22: Step response with 300 cm cable (non USB-cable) and the same damping network as above (0.39 Ω and 10 µF capacitor on VBUS).

The construction of an USB cable (where the positive and negative wires are close together) is much better regarding the amount of inductance. When a 1.5 meter USB cable is used in the same situation as above gives the below step-response: Figure 22.

So the 0.39 Ω series resistor and a 10 µF capacitor on the VBUS will give sufficient damping for short to middle length USB-cables. This configuration is recommended for typical cases.
When longer cables are used, higher resistor values might be needed to achieve sufficient damping. Maximum charge current and allowed voltage drop over the series resistor can limit the amount of damping in that case.

Selection of the resistor value must be done with care. With a high value resistor, the input VBUS voltage could be decreased to a level that eventually the required charging voltage level cannot be reached anymore. Also a high peak current (e.g. due to vibrator motor operation) will cause a sudden drop on the VBUS input and possibly trigger an unexpected USB detach interrupt.

Alternatively to the mentioned 0.39 Ω and 10 µF parts, a 0.56 Ω resistor and a 4.7 µF capacitor, or a 0.47 Ω and a 6.8 µF can be used. These R-C combinations will result in the same damping value. Preferably the capacitors should be at least 10 V types.

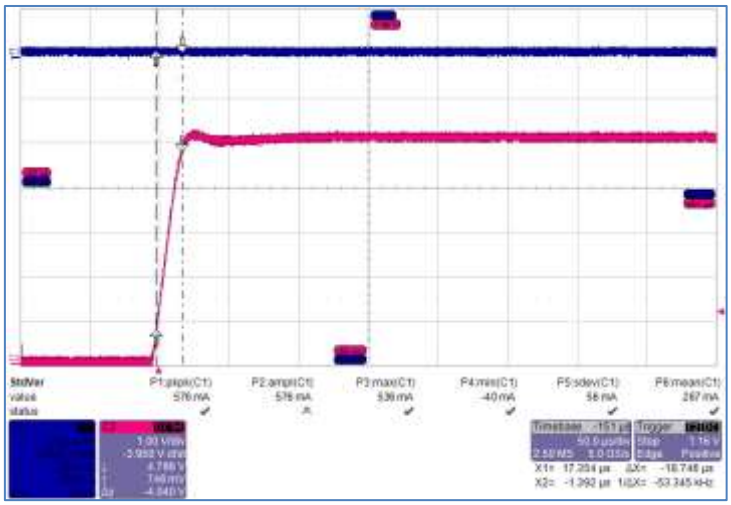


Figure 23: Step response of VBUS with 0.39 Ω and 10 µF for a 1.5 m USB cable.

5.8 Hibernation Mode and wakeup

For shipment purposes, applications with the DA1468x SoC can be put into hibernation mode, which is also called “shipping mode”. In this ultra-low power mode, there is no RAM retained, no clocks running (so no RTC), and all domains are off to minimize power consumption and to avoid discharging the onboard battery. The V33 and the V12 power rails are supplied from low power clamps which are programmable and can be lowered during hibernation to reduce power dissipation as much as possible.

The system can wake up from hibernation by HW Reset, Power-On Reset (POR) or Wake-Up controller (GPIO trigger).

- **HW Reset:** it is triggered by making the RST pin high.
- **Power-On Reset (POR).**
- **Using the Wake-Up Controller (GPIO Trigger):** the Wake-Up Controller can be programmed to wake up the DA1468x from extended-sleep (clocked) mode as well as from clockless sleep modes (deep-sleep, hibernation mode).

The device wakes up from hibernation when a triggering event appears (rising or falling edge on GPIO) and starts execution as if a HW reset has occurred, since there is no retained memory. The GPIOs can be latched to any configurations (input, input pull-up, or input pull-down) and retains their states during hibernation. The wake-up can occur from different sources, such as buttons or an external controller.

The wake-up controller can also be used for waking up the DA1468x from hibernation-mode when a USB cable is plugged in to the device. In this case, a resistor divider from VBUS is used and the circuit schematic is shown in Figure 24**.** When the USB cable is plugged in to the device, the GPIO state changes (via the voltage divider) from Low to High and the device wakes up from Hibernation mode (Figure 25). The voltage divider (R1 = R2 = 620 kΩ) divides the USB voltage by two in hibernation mode where the GPIO is configured as input. Since this is intended to be a one-time wakeup, when the system exits hibernation mode the application must either disable the wakeup controller on that GPIO or configure the GPIO as input pull-down (adding the internal 25 kΩ resistor in parallel to R2). This reduces the voltage divider output (below 0.2 V) and prevents the device from waking up every time a USB cable is plugged in.

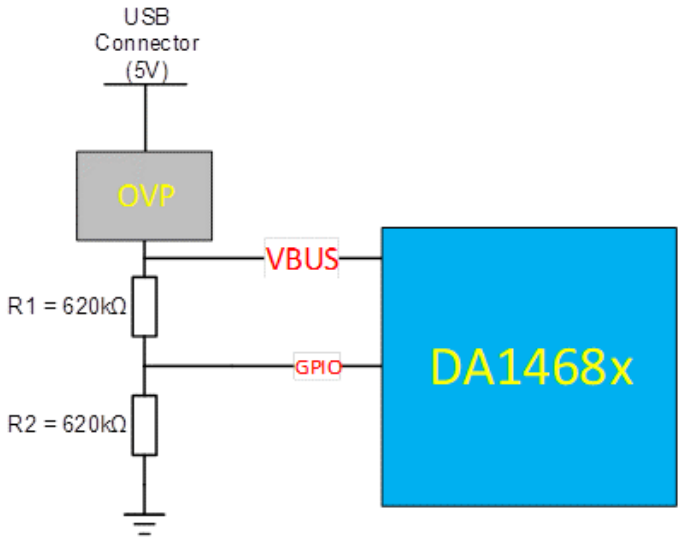


Figure 24: Wakeup from Hibernation by VBUS voltage using GPIO trigger

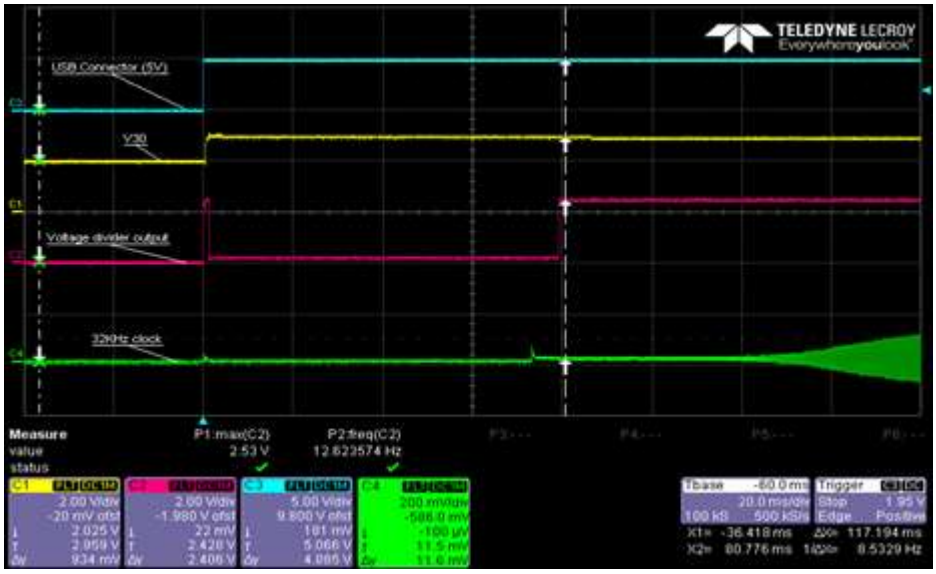


Figure 25: GPIO set as Input (no pull)

Note: since the DA14680-01 and the DA14681-01 SoCs are not clockless when in ‘shipping mode’, these SoCs can be woken up directly by applying a voltage to the VBUS input of the SoC by means of plugging in the USB cable. These SoCs use the LDO_VBAT_RET instead of the ~2V Clamp).

The above method (Figure 24) needs to be applied to the DA14682-00 and the DA14683-00 only. These SoCs are clockless when in ‘shipping’ or hibernation mode and need the Wake-Up Controller to wake up from this clockless mode (using the ~2V LDO_Ret Low Power Clamp).

5.9 RFIO port

The DA1468x provides a single ended RFIO port, matched to 50 Ω. The RFIO port consists of the RFIOp and RFIOm pins, where RFIOm is connected to ground.
A copper trace with a characteristic impedance of 50 Ω interconnects the RF port and the antenna.
A pi-network (Z1, Z2, Z3) close to the antenna feedpoint is added for antenna matching purposes.

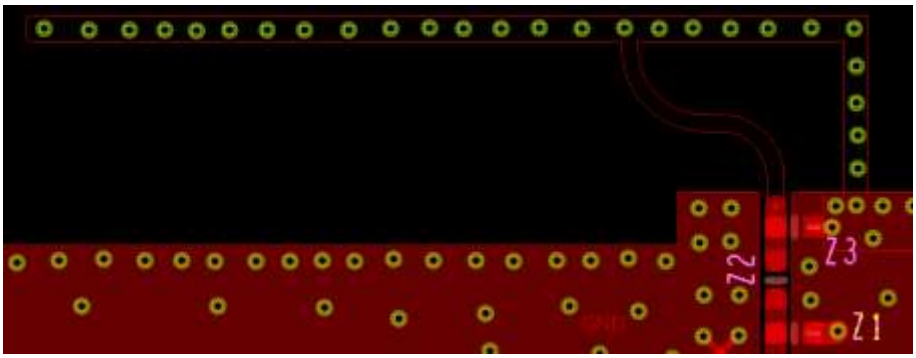


Figure 26: RF matching circuit must be placed as close as possible to the antenna

Minimize the transmission line length between radio IC and antenna in the PCB layout.

- The characteristic impedance of the transmission line should match the required radio impedance: 50 Ohm.
- Place the antenna matching components (Z1, Z2, Z3) as close as possible to the feeding point of the antenna.
- Make sure that the component's GND are connected on the same GND plane (left-hand side of the transmission line in Figure 28 and right-hand side in Figure 33).

5.10 PCB layout

The DA1468x PCB layout is mainly dependent on the chip's package. The fine pitch of WLCSP package is suitable for microvias approach whereas for AQFN package, a PTH-vias approach can be implemented.

Microvias or PTH vias: Microvias and especially microvias on chip pads, make board design easier because of their small size. Copper filled vias offer low dc resistance. The thickness of the dielectric layer depends on microvias aspect ratio (hole diameter to microvias depth), a pcb manufacturer capability. Assuming that microvias diameter is 100 μm, then for an aspect ratio 1:0.8, the dielectric layer can't be higher than 80 μm.
The cost of producing a PCB with microvias is higher in comparison to a PCB with PTH vias. For copper filled vias, cost and production time are significantly higher.

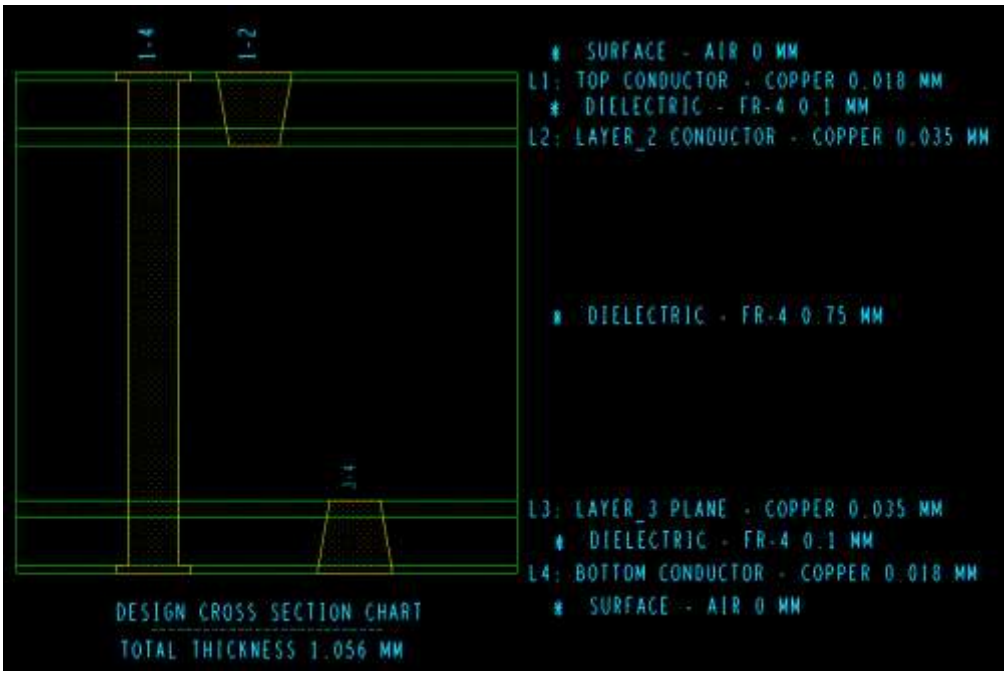


Figure 27: WLCSP53 PCB stackup

ESD considerations: Please consider these measures for a good ESD performance of your application. See also the USB section 5.7.1 for ESD measures on the USB connector.

- If charger contact pins are used, place an ESD protection device directly between the two charger connections: VBUS and ground. ESD testing according IEC 61000-4-2 means that ESD shooting at the charger contact pins will be done. At least upto 6KV level according the Human Body Model.
- Isolate the 16MHz Xtal ground connections from the ground used by the ESD protection devices.
- It's strongly advised to connect the battery ground terminal to the same ground point or ground plane as the Vbus ground connection.
- If any GPIO or the antenna can be touched by the user, provide an ESD protection device at these.
- Please read also AN-B-056 - DA14680_681 Recovery from System Level ESD Events [3].

5.10.1 PCB layout for WLCSP53 package

An example pcb layout, where all signals are extracted, is presented below (Figure 28). This is a 4 layers pcb, in 1-2-1 configuration. Microvias, 100 µm - 250 µm were used between layers Top (L1) – L2 and L3- Bottom (L4). No buried vias have been used. Finally the PTH vias are 200 µm - 450 µm (drill diameter - pad diameter).

On the top layer, the signals of the external row are routed. Layer 2, is used for routing the pins of the internal row.
Layer 3 is the reference GND plane (normal ground vias connect to this layer directly; 50 ohms microstrip line uses this layer as a ground reference).

Generic guidelines for the WLCSP53 PCB layout are:

- Active components operating at high frequency should have their layout made as compact as possible. This will prevent the cross-coupling between lines and also minimizes the parasitic effects which will have a negative impact on the operating parameters.
- Always provide a solid grounding to the radio IC. Use as many vias as possible to create a solid GND under the IC itself and connect it to inner and bottom GND layers.
- Place the 16 MHz or 32 MHz crystal used as reference for the BLE radio as close as possible to the IC. This will minimize any additional capacitive load on the input pins and reduces the chance of crosstalk and interference with other signals on the board. For the same reason, please provide openings in the nearest ground layer under the 'hot' pads of the 16 MHz or 32 MHz crystal. Please refer to Figure 28.

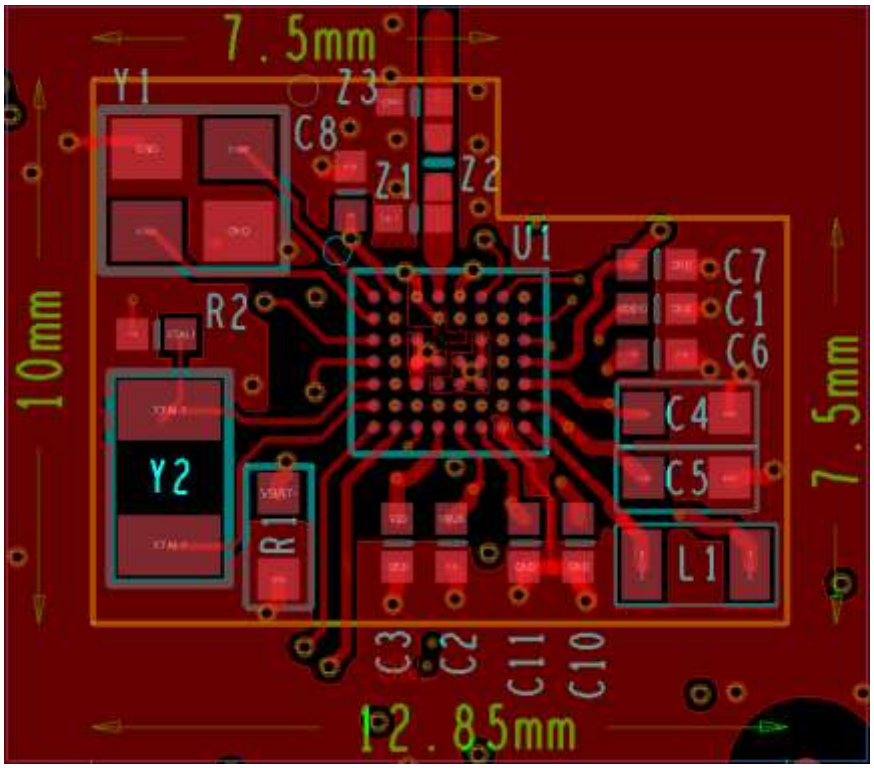


Figure 28: WLCSP53 PCB layout, top side

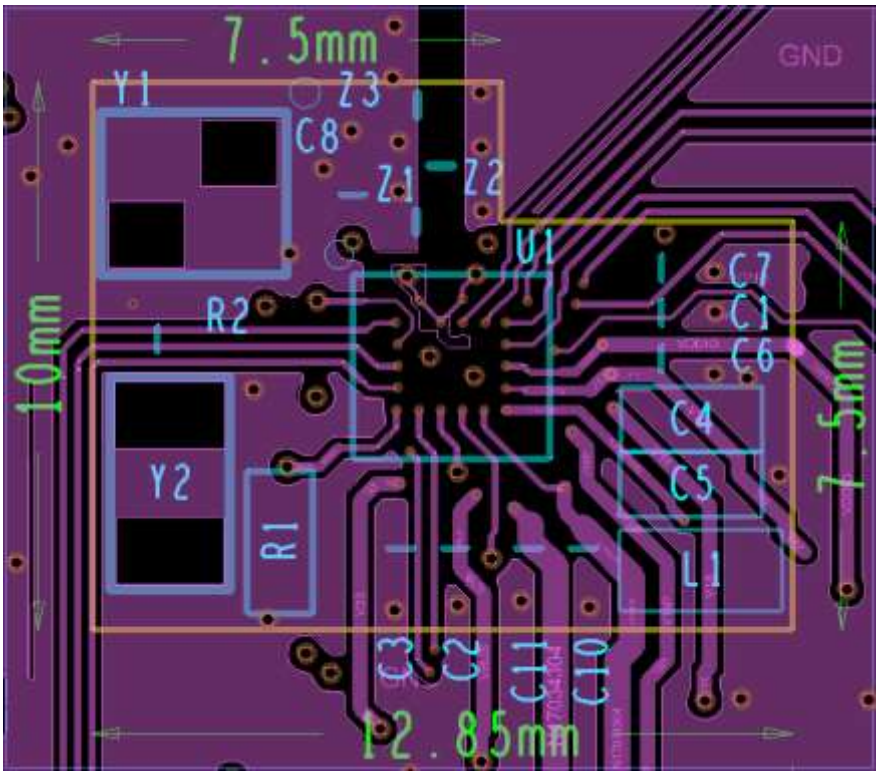


Figure 29: WLCSP53 PCB layout, layer 2

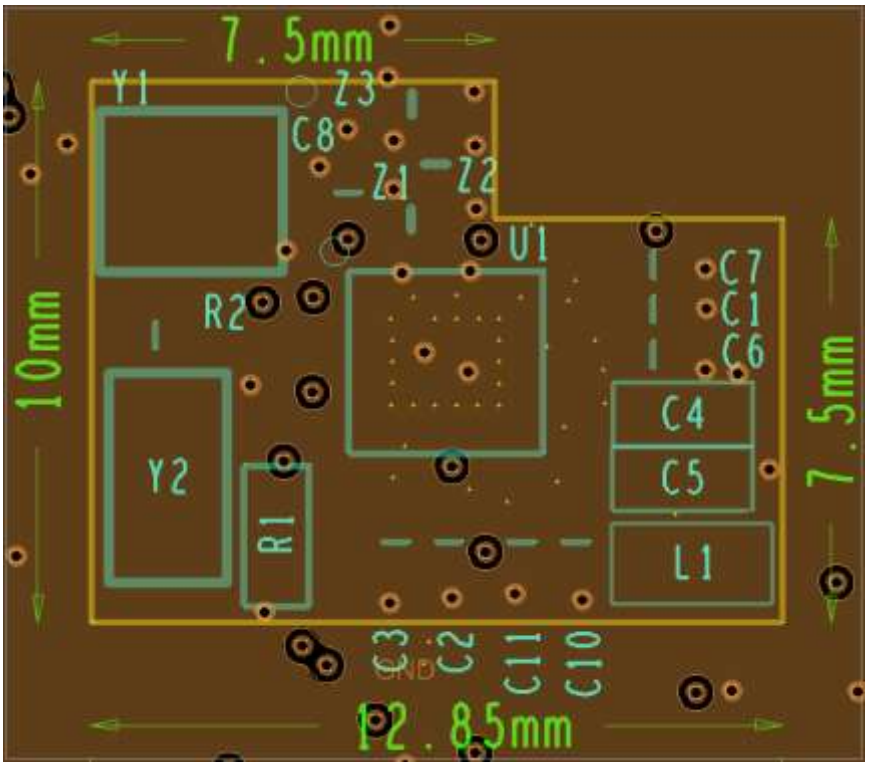


Figure 30: WLCSP53 PCB layout, layer 3, reference GND

Special attention must be given to the routing of the GND pins at the center of the package. PTH vias are used whereas the RFIOm and PSUB_RF signals are separated from the rest of the VSS pins on top layer:

1. RFIOM (A3), PSUB_RF (B4) and ESDN (A5)
   - Create a GND island on TOP layer, as it is illustrated on Figure 31.
   - Use 2 traces (as short as possible) to connect to 2 PTH vias (not microvias). The PTH vias are connected to layer 2 (ground plane used for 50 Ohms microstrip line).

2. GND_RF2 (C3), GND_RF1 (D3), AVS1 (D4) and SOCN (E3):
   - Create the GND island on TOP layer as shown on Figure 31
   - Connect this island with a PTH via (not microvia) to the layer 2

3. VSS1 (C6) , VSS2 (D5), VSS3 (D6), VSSIO1 (E6), VSSIO2 (E5) and AVS2 (E4):
   - Create the GND island on TOP layer as shown on the draft PCB below
   - Connect this island with a PTH via (not microvia) to the layer 2.

4. GND_BUCK (G7)
   - Connect to GND as presented on Figure 31
   - A decoupling cap should be placed very close to GND_BUCK and VBAT1, as is presented on Figure 28.

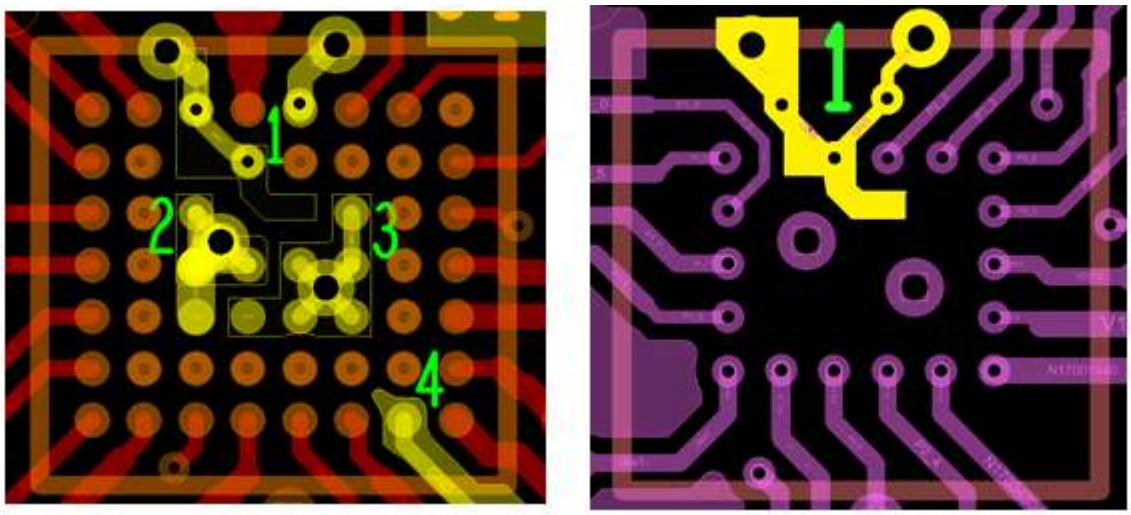


Figure 31: Ground connectivity Top (left) and layer 2 (right)

5.10.2 PCB layout for AQFN60 package

The PCB layout for the AQFN60 package, is implemented in a 4 layers PCB. No microvias required. The PTH vias are 200 µm - 450 µm (drill diameter – pad diameter). The PCB layer 2 is the reference ground: the ground vias connect to this layer, and the 50 Ohm microstrip line uses this layer as a ground reference.

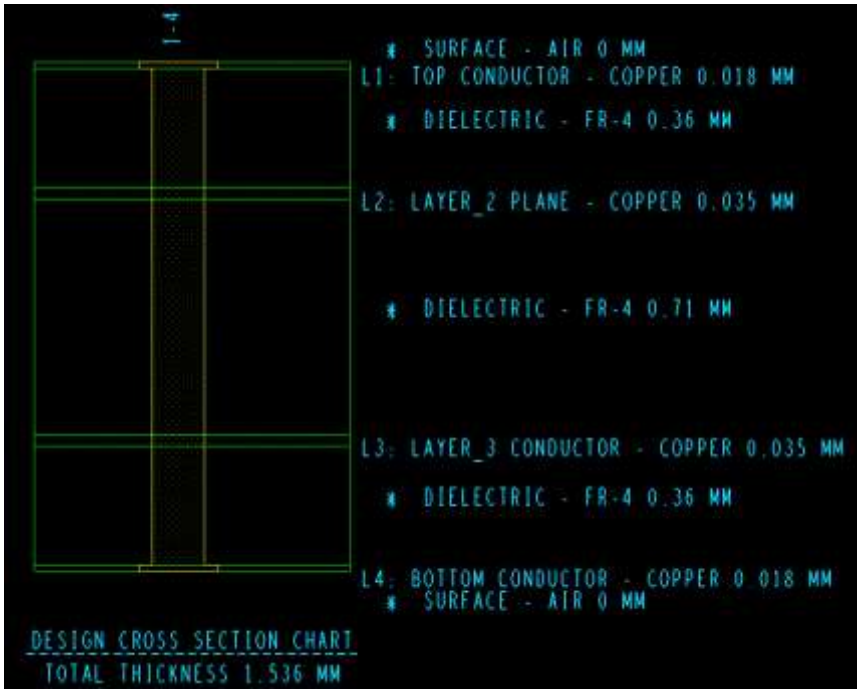


Figure 32: AQFN60 PCB stackup

General guidelines are:

- Active components operating at high frequency should have their layout made as compact as possible. This will prevent the cross-coupling between lines and also minimize the parasitic effects which will have a negative impact on the operating parameters.
- Always provide a solid ground to the chip's ground pins. In particular the DCDC_BUCK ground is a critical ground connection.
  Apply multiple vias to create a solid GND under the IC itself and connect it to the inner and the bottom GND layers. A 3x3 via matrix in the chip's ground is considered good.
- Place the 16 MHz or 32 MHz crystal as close as possible to the IC. This will minimize any additional capacitive load on the input pins and reduces the chance of crosstalk and interference with other signals on the board.
  For the same reason, please provide openings in the nearest ground layer under the 'hot' pads of the 16 MHz or 32 MHz crystal. Please refer to Figure 33.

Special care must be given to the grounding of the following pins:

- RFIOM (pin 51): Route using a minimum length line to an independent normal ground via (do not connect with the ground paddle to prevent noise to be coupled into the RF circuits). This normal ground via connects to the ground plane (2nd layer).
- ESDN: (pin 53): Route using a minimum in length line to an independent standard ground via (do not connect with the ground paddle). This standard ground via connects to the ground plane (2nd layer).
- The ground paddle (at the bottom of the aQFN package): use a matrix of 3x3 or 4x4 normal vias to the ground-plane (2nd layer). This paddle measures about 3.5 mm x 3.5 mm.
  Please make sure the ground-pad shape follows the shape of the paddle, including the exposed paddle parts.
  In order to avoid potential BOD problems when the SIMO BUCK DCDC is active (lifting of the internal BOD reference voltage caused by large DCDC peak currents), a ground via connected to a solid ground-plane near the DCDC_BUCK exposed ground stub must be present. In Figure 33 it's the most bottom-left placed via in the ground under the chip.
  This Buck DCDC_Ground is located between the VBAT2, VBAT1 and VBUS pins: between pins B6 and B7.

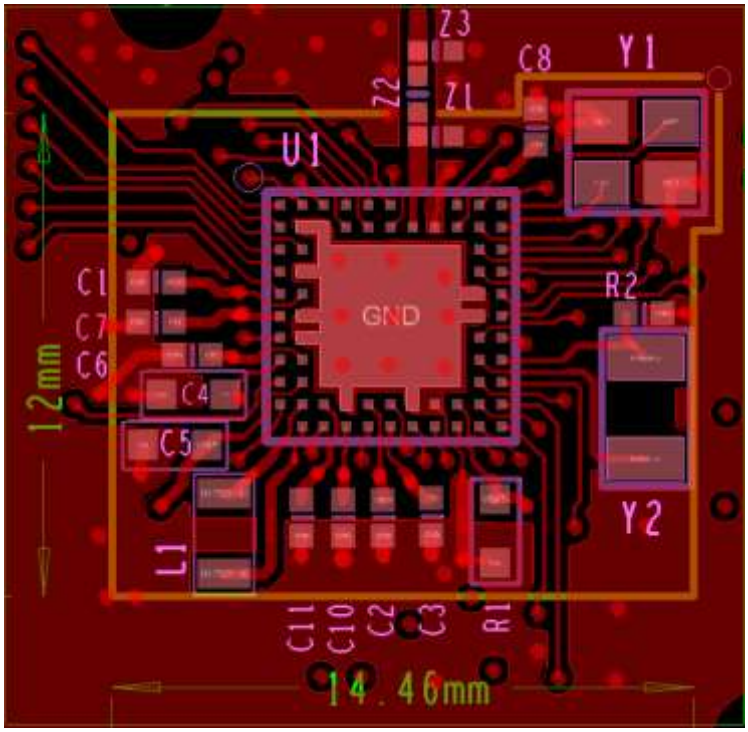


Figure 33: AQFN60 PCB layout, top layer

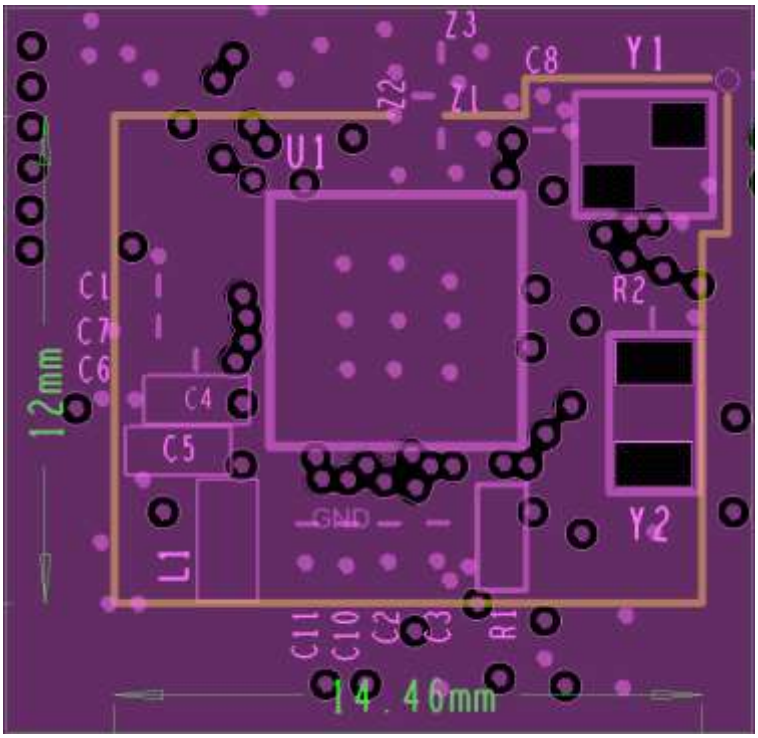


Figure 34: AQFN60 PCB layout, layer2, reference ground

5.11 AQFN60 - Package Outline (POD) Information

Please refer to Section 39 of the DA14680-01, DA14681-01 and DA14682-00, DA14683-00 datasheets for information on the AQFN60 package outline. [1]

5.12 WLCSP53 - Package Outline (POD) Information

Please refer to Section 39 of the DA14680-01, DA14681-01 and DA14682-00, DA14683-00 datasheets for information on the WLCSP53 package outline. [1]

Appendix: AQFN60 assembly and soldering guidelines

A.1 PCB

There are two types of land patterns are chosen for user PCB design, one is Solder Mask Defined (SMD), solder mask openings smaller than metal pads. The other is Non-Solder Mask Defined (NSMD), solder mask openings larger than metal pads. Better control of the copper etching process as compared to the solder masking process makes NSMD preferable.
Also, the SMD pad definition can introduce stress concentrations near the solder mask overlap region that can result in solder joints cracking under extreme fatigue conditions.
Using NSMD instead improves the reliability of solder joints as solder is allowed to “wrap around” the sides of the metal pads on the board.
NSMD is recommended to use on SMT assembly, the pad size used on the Dialog boards as showing below:

Terminal pad: 0.25 x 0.25 mm ; Terminal solder mask: 0.4 x 0.4 mm

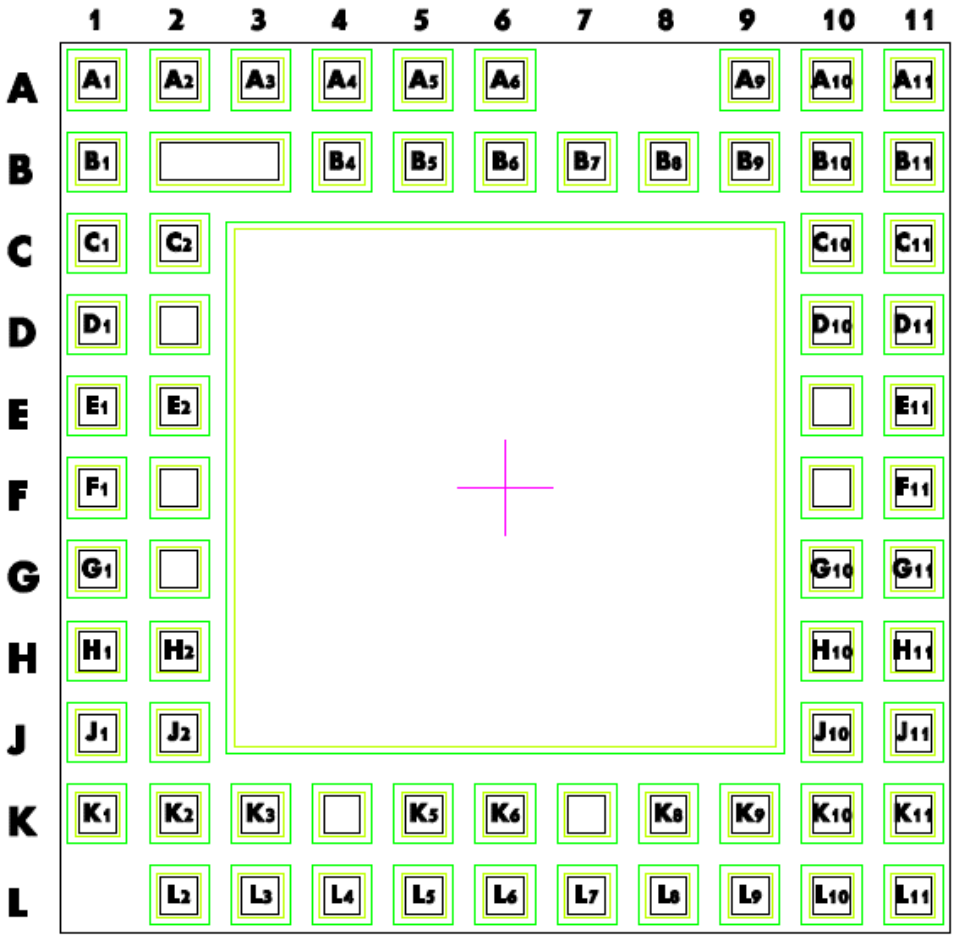
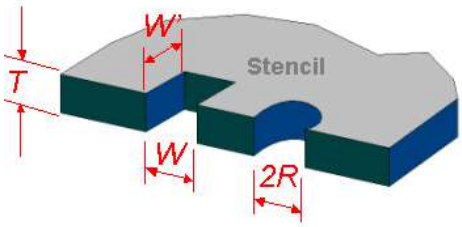


Figure 35: PCB footprint data

A.2 Stencil Design

- Basic concept: Aspect Ratio (W/T, 2R/T) > 1.5, Area Ratio (W/4T, R/2T) > 66%



- Trapezoidal Aperture: Bottom Opening 25~50 microns larger than the Top, Well design for paste release

- Use laser cutting followed by electro-polishing for stencil fabrication.
- The recommended stencil apertures are the same as the PCB land pattern, thickness is 0.1mm
- Use Type 4 solder paste (25 to 45 micron particle size range) or finer for solder printing, and SAC305 is a common used solder paste. Senju M705-S101-S4 is recommended solder paste.
- For the thermal paddle stencil opening, **using array of 2x2 opening and 20% opening of PCB thermal paddle area is recommended** to avoid void resident inside thermal paddle and can get better solderability.

Stencil Thickness: 0.1 mm

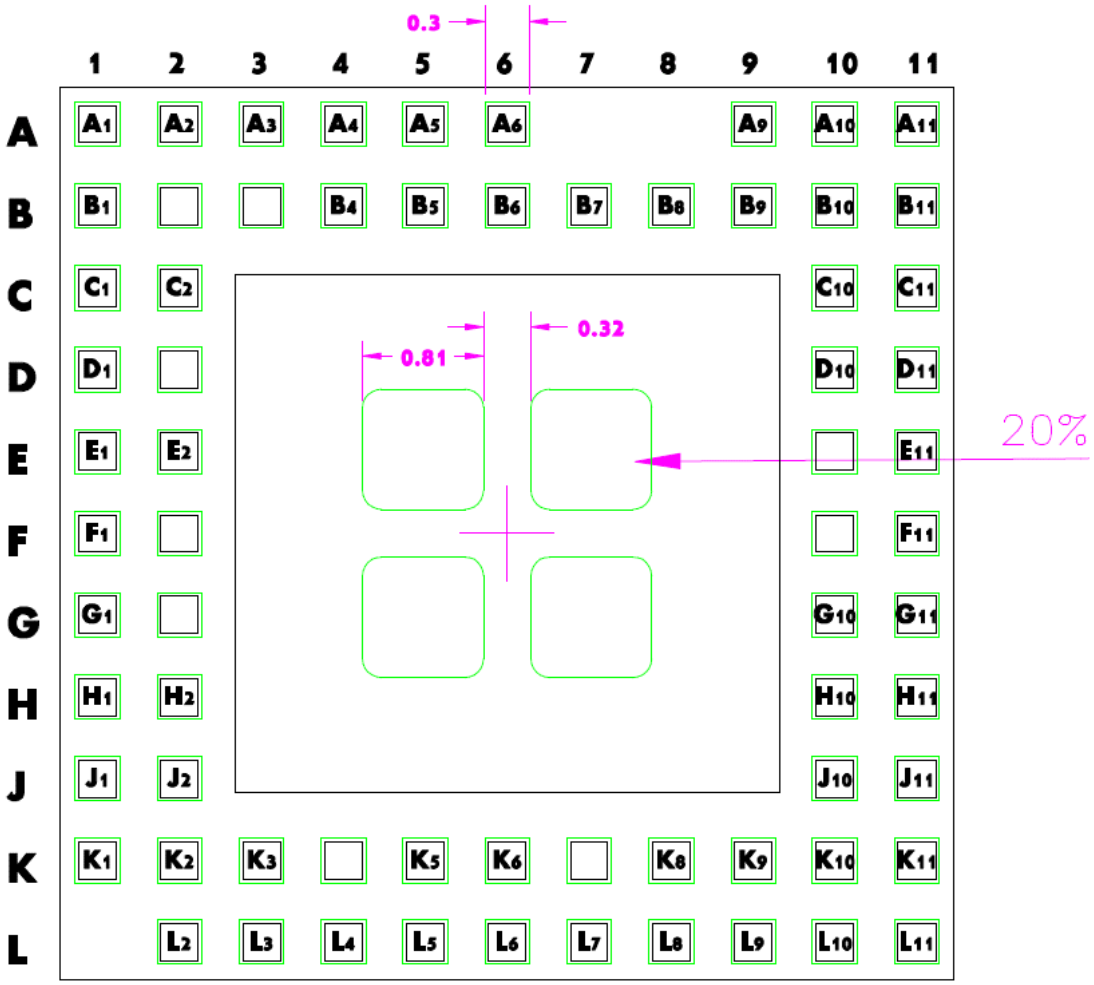


Figure 36: Recommend of stencil opening of thermal

A.3 Component Placement

For placing the AQFN, following methods can be used for recognition and positioning:

- Vision system to locate package outline.
- Vision system to locate individual bumps. It is recommended that the side-lighting option on the pick and place machine's vision system be used when attempting to use an individual bump recognition approach to ensure better contrast for bump recognition
- It is preferred to use a machine with fine-pitch placement for better accuracy.

A.4 Reflow Profile

Below reflow-profile, based on using solder paste SAC305

	A.Ramp Up Rate (25~150C)	B.Pre-HeatTime (155~165C)	C.Ramp Up (200C~ peak)	D.Reflow Time (Above 220C)	E.Peak Temp	G.Cooling Rate (peak ~25C)
SPEC.	<1.2C/s	60~90 sec	<1C/s	60~90 sec	230~255C	<6C/s

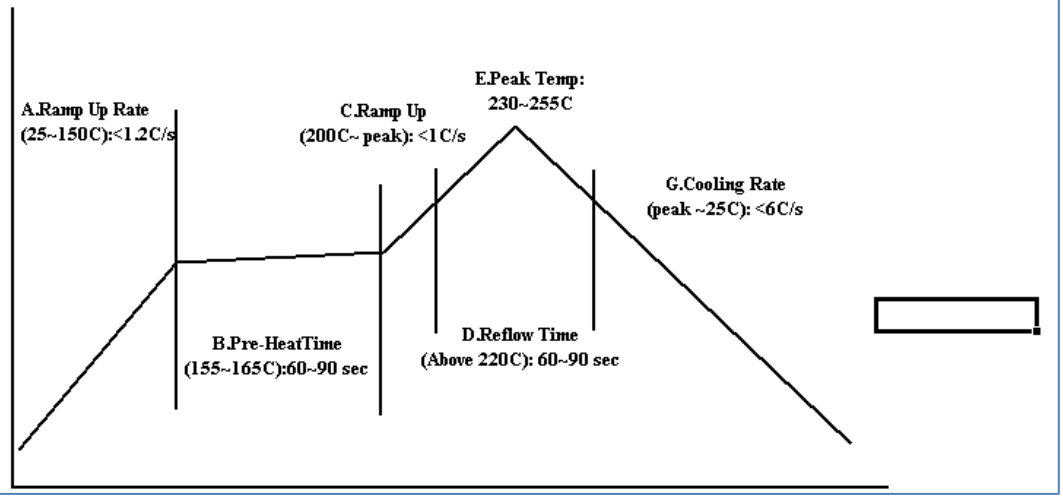


Figure 37: Reflow profile for solder paste SAC305

Revision history

Revision	Date	Description
1.0	22-Feb-2016	Initial version.
1.1	20-Apr-2016	Change details: ● Table 1 adapted: DA14680 available in AQFN package only. ● ESD measures in section 5.9. ● Additional PCB layout guidelines in section 5.9.2.
1.2	02-Jun-2016	Change details: ● Corrections in section 5.1 for VDD1V8 (V18) and VDD1V8P (V18P) usage. ● Section A.1: PCB terminal pad size changed from 0.3 mm to 0.25 mm.
1.3	22-Jul-2016	Updated section 4, 5.8 and 5.9.
1.4	26-Aug-2016	Added information on USB signal integrity in section 5.7.
1.5	24-Jun-2017	● Adding SIMO DCDC inductor examples in Table 6.16 MHz crystal examples in Table 7 and 32.768 KHz crystal examples in Table 8. ● Table 5: the rated voltage of capacitors C6, C7 and C8 have been corrected to 10V. And rated voltage of C2, C10 and C11 changed to 10V in order to have larger effective capacitance. ● 32 MHz crystal references removed in section 5.3.1
1.6	24-Jan-2018	Added information on the DA1468x SIMO Buck DCDC in section 5.1.
1.7	14-Feb-2018	Change details: ● Removing DA14681-00, adding the DA14682-00 and DA14683-00 ● Added a table with 32 MHz crystal examples (DA14682/683 support 32 MHz crystal operation)
1.8	23-Jul-2018	Added ‘Feature Available?’ checkboxes on top of relevant sections
1.9	28-Mar-2019	Removed the POD drawings, instead referring to the datasheets Added the Hibernation Mode and Wakeup section 5.8.
2.0	19-Jan-2022	Updated logo, disclaimer, copyright.

Status definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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