Application Note

DA14585/DA14586 Application Hardware Design Guideline

AN-B-054

Abstract

This document serves as a guideline for preparing schematics and PCB layouts for your application using DA14585/DA14586.

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1 Terms and Definitions

QFN	Quad Flat No-Leads
WLCSP	Wafer Level Chip Scale Package
PCB	Printed Circuit Board
GPIO	General Purpose In/Out
ADC	Analog to Digital Converter
SPI	Serial Peripheral Interface
ESR	Equivalent Serial Resistance

2 References

[1] DA14585, Datasheet, Dialog Semiconductor.

[2] DA14586, Datasheet, Dialog Semiconductor.

[3] UM-B-079, DA14585/586 SDK 6 Software Platform Reference, User Manual, Dialog Semiconductor.

[4] AN-B-027, Designing printed antennas for Bluetooth® Smart, Application Note, Dialog Semiconductor.

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3 Introduction

The DA14585/DA14586 offers designers great flexibility to create more advanced applications from the smallest footprints and power budgets. It supports all Bluetooth developments up to and including Bluetooth 5 and Bluetooth low energy Mesh. Besides, with 96 kB of RAM and a wide supply voltage range (0.9-3.6 V), it covers a larger choice of application possibilities with various energy sources.

For DA14586, a flash of 2 MB is embedded in the package, whereas the DA14585 has the possibility to execute code from an external flash. The available package options for both devices are summarized in Table 1.

Table 1: DA14585 and DA14586 Chip Options

Chip	Package	Numbers of Pins
DA14585	QFN (5 mm × 5 mm)	40
	QFN (6 mm × 6 mm)	48
	WLCSP (2.40 mm × 2.66 mm)	34
DA14586	QFN (5 mm × 5 mm × 0.9 mm)	40

The purpose of this document is to provide a set of guidelines which will help users prepare schematics and PCB layouts for products with the DA14585/DA14586. Recommended schematic, chip interfaces and surrounding components as well as PCB layout guidelines of both devices are provided.

4 Possible Configurations of DA14585/DA14586

There are two modes of operation possible for both of these devices depending on the configuration of the synchronous DC-DC convertor. They are:

- Boost (step-up) mode, starting from 0.9 V, when running from an Alkaline/NiMH cell.
- Buck (step-down) mode for increased efficiency when running from a Lithium coin-cell or two Alkaline batteries down to 1.8 V.

The system diagrams for these two modes for both DA14585 and DA14586 are given in Figure 1 and Figure 2, respectively.

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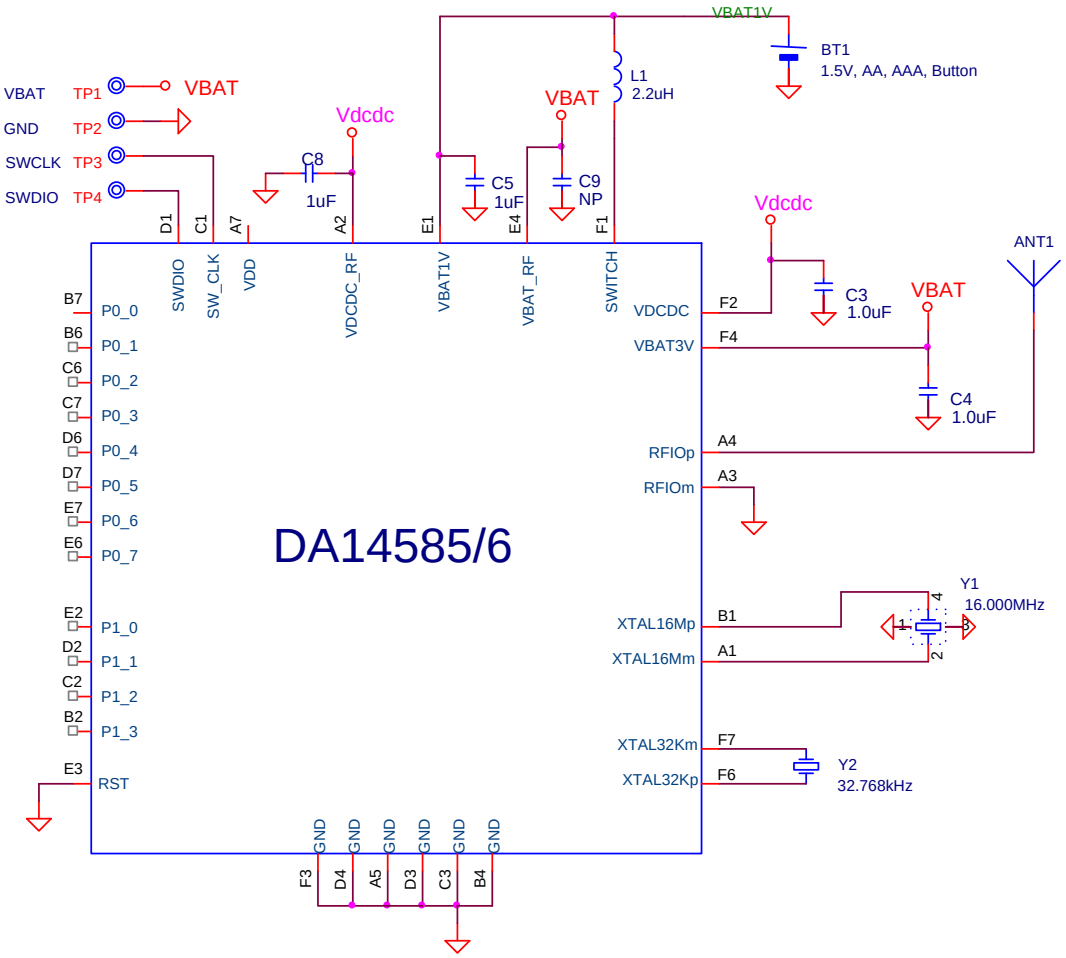


Figure 1: System diagram of DA14585/14586 powered by alkaline battery cells (boost mode)

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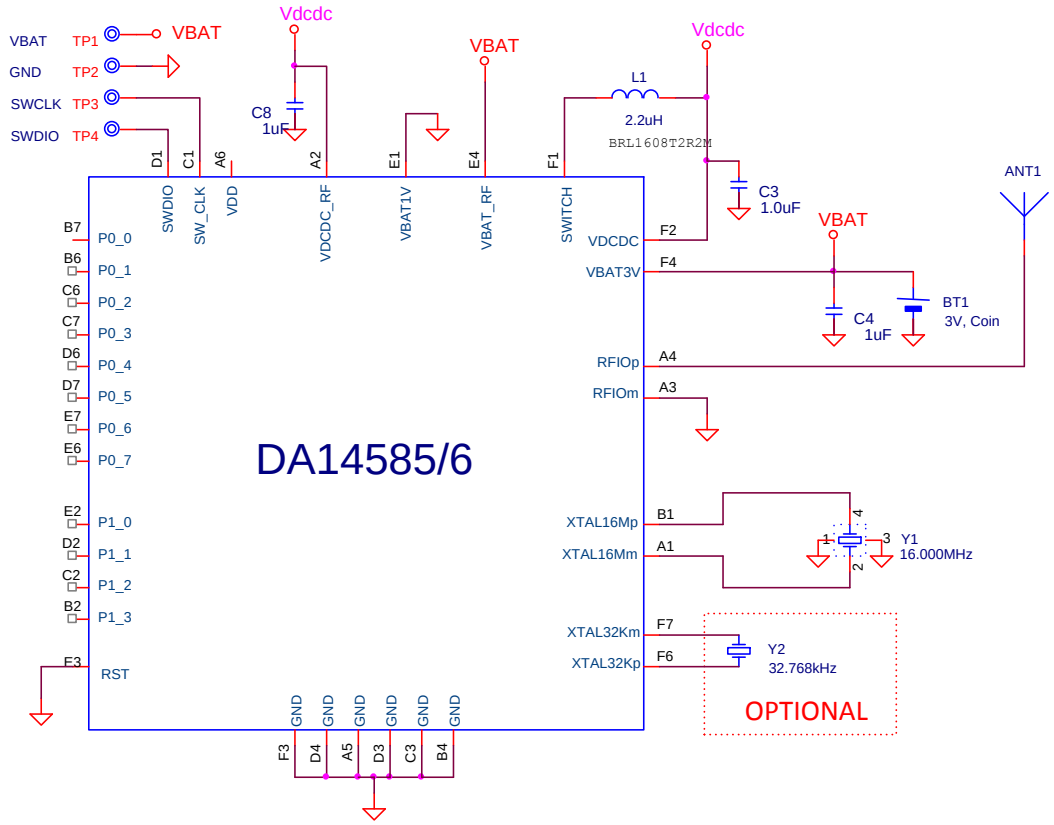


Figure 2: System diagram of DA14585/14586 powered by lithium coin cell (buck mode)

5 Schematic Guidelines

5.1 GPIO ports

- For UART communication, please notice that preferably the UART ports P0_4 and P0_5 are used. These are the default ports and are part of the Boot-Sequence. If not available, please use other UART pairs, that is, P0_0/P0_1 or P0_2/P0_3.
- When not using the external ADC measurement feature, make sure the voltage levels at the ports from P0_0 to P0_3 are not higher than Vbat3V in order to prevent that these signals are interfering with internal ADC measurements. In case the external ADC measurement feature is being used, check that the voltages at the ADC input ports, P0_0 through P0_3, are not higher than Vbat3V + 0.2V and never exceed the maximum level of 3.45 V.
- When booting from an external SPI slave device, make sure to use the following ports: P0_0, P0_3, P0_5, and P0_6 for serial clock (SCK), chip select (CS), master input slave output (MISO), and master output slave input (MOSI), respectively. For details, see *Table 20: Development Mode Peripheral Pin Mapping* in the datasheets [1] [2]. Refer also to [3].

5.2 16 MHz Crystal Oscillator

- Select a crystal having a maximum ESR lower than 100 Ω. Higher ESR values will increase the start-up time of the 16 MHz crystal oscillator. For crystals having ESR values of 50 to 80 Ω, start-

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up time is about 2 to 2.5 ms. For crystals having an ESR of 100 Ω or higher, it can be as long as 4 or 5 ms. Smaller packages of 16 MHz crystal (for example, size 2016) tend to have higher ESR values than larger packages (for example, size 3225).

- No additional load capacitors are required. Please don't put capacitor pads on the PCB as they will increase the capacity. The required crystal load capacitors are provided internally. The stray capacitance to the 16 MHz crystal must be minimized to avoid crosstalk to the 16 MHz oscillator.
- Keep the connections to the 16 MHz crystal as short as possible to minimize picking up interference or noise.
- Keep UART lines, debug lines and other clock lines away from the 16 MHz crystal oscillator. This applies for traces at the underlying layer, which may be a ground plane too. The oscillator is very sensitive and is easily disturbed, which may lead to an unstable BLE.
- The 16 MHz crystal oscillator is quite sensitive to signals on port P1_2 and P1_3. These ports will generate much crosstalk to the 16 MHz oscillator when toggled fast. Make sure these ports are not toggling when the 16 MHz oscillator is active. It is safe to use them for static purposes. Refer also to 6.1 for more details.

5.3 32 KHz Crystal Oscillator

- The 32 KHz crystal should have a load capacitance in the range of 6-9 pF. No additional load capacitors should be placed. Please do not place capacitor pads on the PCB neither.
- Although less critical than the 16 MHz crystal oscillator, keep its connections short.
- Do not let traces run close or parallel to the Xtal32Kp side of the Xtal32K oscillator.

5.4 DCDC Converter

- Good filtering and decoupling of the VDCDC_RF supply pin is important for a good radio frequency (RF) performance. The 1 µF decoupling capacitors should be placed as close as possible to the supply pins.

  This is of special importance in a boost mode system, where VBAT1V might be close to VDCDC. In this case the noise at VDCDC is high and RF performance is affected. In this case a higher decoupling capacitor (for example, 2 µF) might be needed.

  In rare cases, where VBAT1V is close to VBAT3V, doubling the decoupling by placing a 1µF capacitor at C9 is recommended.
- The SWITCH trace to the inductor should be as short as possible. Please prevent any coupling to other signals. Use a thin trace with a length of more than 7 mm between the VDCDC inductor and the VDCDC_RF pin. The inductivity of this trace together with the decoupling capacitor at VDCDC_RF builds a low-pass-filter, reducing the HF-noise at VDCDC_RF.
- Inductor: choose a type with a high resonance frequency, preferably higher than 75 MHz. This guarantees a low stray capacitance and minimizes the HF noise at VDCDC_RF. Its maximum rated current should be at least 100 mA for a buck-mode application and at least 200mA for a boost mode application. The DC resistance should be below 1 Ω for good efficiency.

  When the inductor is in saturation, it cannot operate well anymore, resulting in high HF-noise and HF-ripple and worse BLE performance. An inductor value of 2.2 µH is recommended.
- Capacitors: use 1 µF for both filtering caps at VDCDC and VDCDC_RF, preferably low inductance types. Please be aware that the voltage rating and the size of a capacitor has influence on the effective capacity at certain DC level. A 1 µF 4V 0402 capacitor might only have half of its capacitance at 2.7V than a 10V, 0603 type.
- For grounding, try to minimize the via inductance. Provide either a ground plane with enough ground vias or use double vias.

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5.5 Debugging Interface

Check for availability of the following signals on test-points, pins, or a header in order to have easy accesses to them for programming and for debugging: JTAG SW_CLK and SWDIO, UART RX, UART TX, VPP, Vbat3V, GND, and Reset.

5.6 RF Input and Output Matching

- For an optimal matching of the DA14585 to 50 Ω, make sure to place a shunt inductor as close as possible to the RFIO pin. The value of this shunt inductor depends on the package:
  - WLCSP package: 3.3nH inductor
  - Both QFN packages: 3.9nH inductor
  - This shunt inductor is L1 in Figure 3. It shall be placed as close as possible to DA14585/14586. This matching ensures best RF sensitivity and highest RF output power. Additionally it gives a 50 Ω point as a reference for the antenna matching.
- Z1, Z3, and Z2 in Figure 3 are components for antenna matching. These parts should be placed close to the antenna. Most universal is a PI matching network, having two shunt components and one series component. Type and value fully depend on the antenna type, but typically small pF caps and low nH inductor values are expected here. To guarantee a constant matching over production, good tolerance components are recommended. In most cases, not all three parts are required to have a good matching.
- The connecting PCB trace should have a characteristic impedance of 50 Ω. The free Agilent tool 'AppCad' can calculate the characteristic trace impedances, when substrate and trace dimensions are known. Also online RF calculators are available.

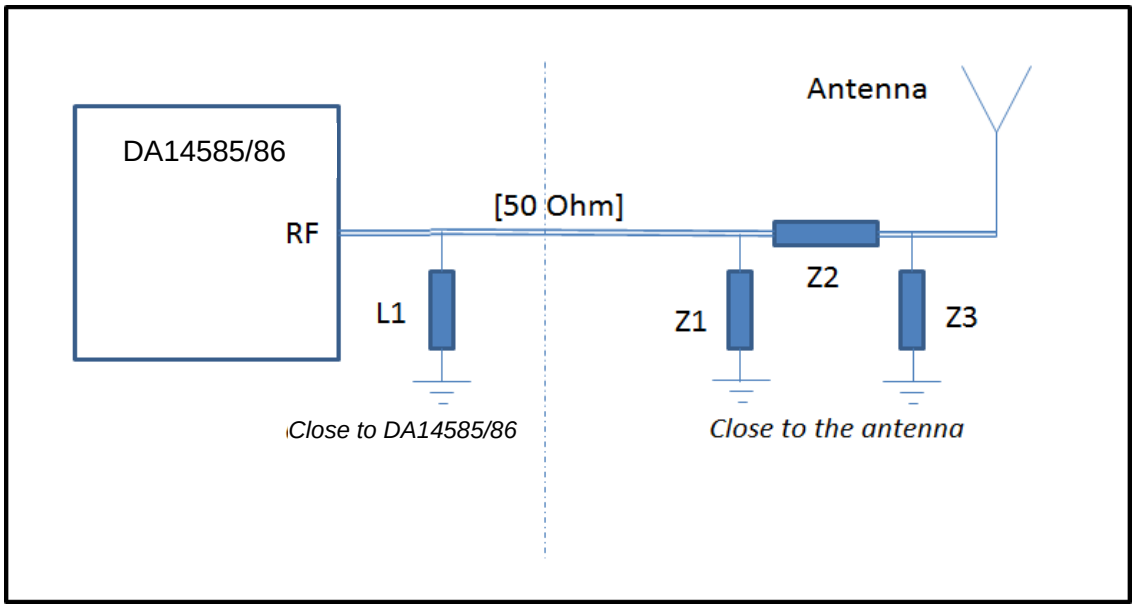


Figure 3: Antenna matching network

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5.6.1 Antenna Placement

When a PCB printed antenna is being used for a ceramic chip antenna, make sure no copper is under the antenna and no traces are running under the antenna area. The antenna must be able to radiate freely. The ceramic chip antenna mostly requires some copper-free area around it.

5.6.2 Printed Antenna Example

Figure 4 shows the PCB-printed antenna used in the Dialog's keyboard reference design. The design is a so-called inverted F-antenna. One can copy and paste this design on any PCB material. Gerber files and design files can be provided.

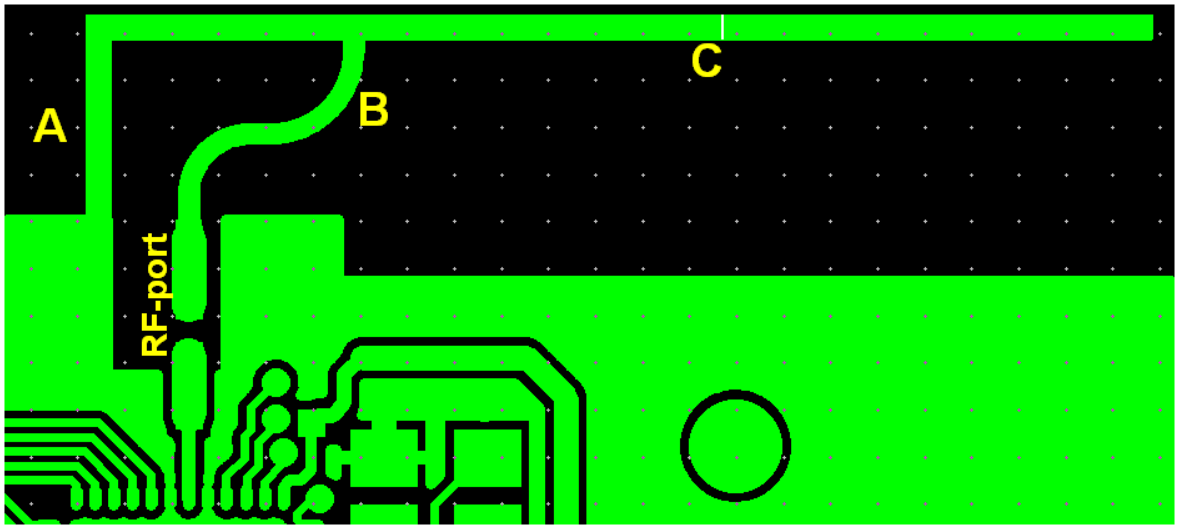


Figure 4: PCB Antenna in Keyboard Reference Design

Measures of the shown printed antenna:

A 4 mm long, 0.53 mm wide: this is for the vertical part only;

B 5 mm long, 0.40 mm wide: the antenna feed trace;

C 23 mm long in total, 0.53 mm wide: the section between A and B is 5.5 mm long.

The grid size in Figure 4 is 1 mm.

A PI-network for antenna matching components is provided too. Please make sure this matching circuit is present in your design. The antenna free space area should be 25 mm × 6 mm. Under and in this area there should be no ground planes, no traces and no components.

A very similar printed antenna is used on Dialog's new evaluation kits.

For more antenna examples please refer to [4].

5.7 Battery Bouncing

When the DA14585/DA14586 application is powered by a replaceable battery, battery bouncing might occur when the battery is fitted into its holder or the application falls on the floor. This short interruption of the supply voltage can cause, in very rare cases, the device to hang. A hardware reset is necessary to restart the application. To prevent the need for user interaction, a 1 µF capacitor can be placed between VBAT3V and RST. In this case RST shouldn't be connected to ground. In case of

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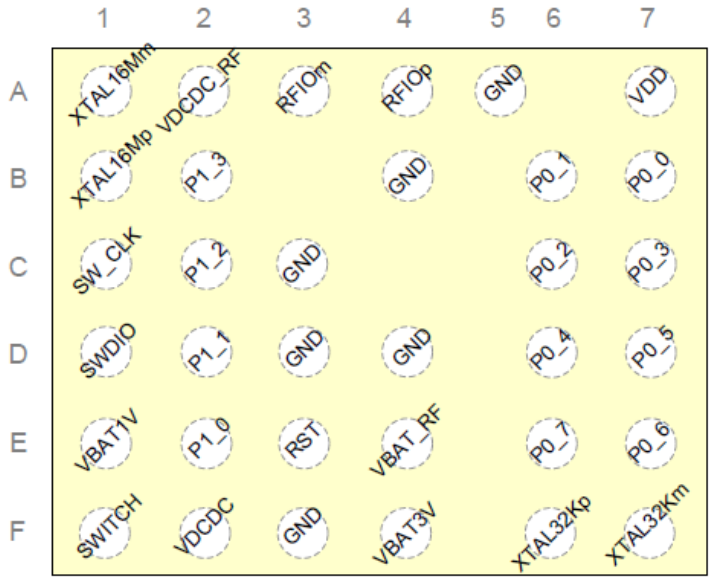
a voltage drop on VBAT3V and the following rise of the voltage, the capacitor will transfer this rising voltage to the RST pin and trigger a reset.

6 PCB Layout Examples

6.1 WLCSP Package: PCB Design Examples for 16 MHz Crystal

The following paragraphs show some design examples for the DA14585 WLCSP package with different PCB structures. For the WLCSP package the inner ring connections (P1_0, P1_1, P1_2, and P1_3; P0_1, P0_2, P0_4, and P0_7) can only be used with a multilayer PCB with micro vias. When micro vias are used, it is recommended to place them in the middle of the balls/connections of the device.

6.1.1 DA14585 WLCSP Ball Pattern



Top View

Figure 5: WLCSP ball pattern

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6.1.2 Single-Layer PCB

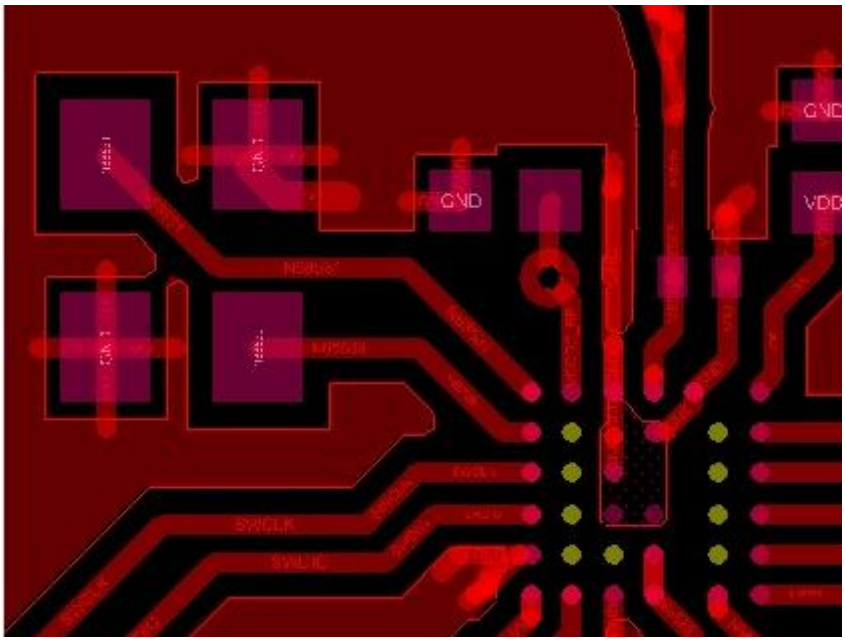


Figure 6: Single layer PCB

The crystal is surrounded by a guard ring. This guard ring is connected to ground. Both crystal case ground connections are connected to ground. The inner ring of the DA14585 is not used since there is not enough space to route to these pins.

6.1.3 Multi-Layer PCB with Regular Vias

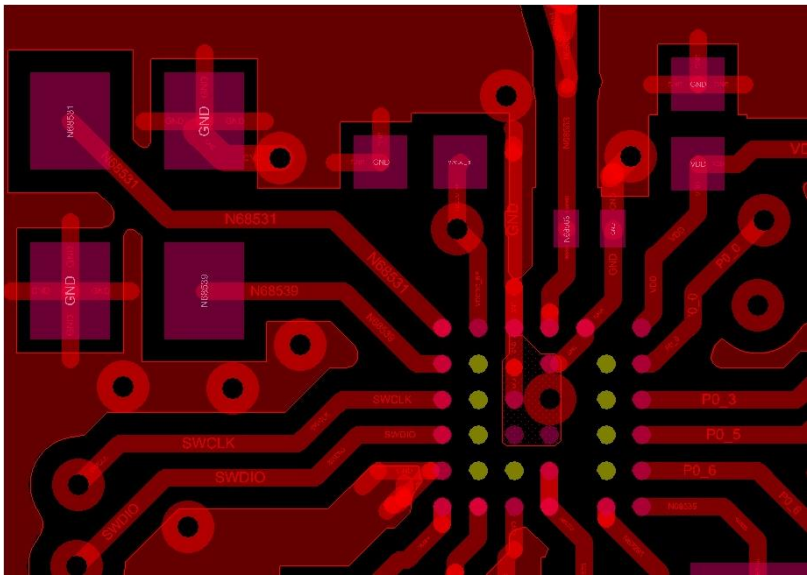


Figure 7: Multi-layer PCB with regular vias

The oscillator circuit is shielded by a ground plane. The crystal is surrounded by a guard ring. This guard ring is connected to the ground plane using vias. Both crystal case ground connections are

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connected to ground. There should be no wires between the oscillator circuit and the ground plane. The inner ring of the DA14585 is not used since there is not enough space to route to these pins when using regular vias.

6.1.4 Multi-Layer PCB with Micro Vias

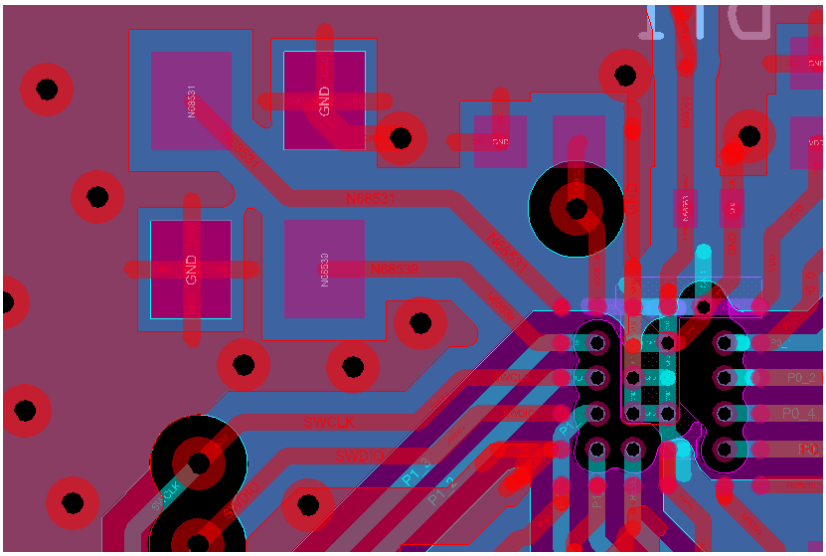


Figure 8: Multi-layer PCB with micro vias

The oscillator circuit is shielded by a ground plane. The crystal is surrounded by a guard ring. This guard ring is connected to the ground plane using vias. Both crystal case ground connections are connected to ground. There should be no wires between the oscillator circuit and the ground plane. The micro vias used to connect the inner pins of the DA14585 are located directly under the pads. This makes it possible to route the GPIO lines and the JTAG lines directly away from the oscillator circuit.

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6.2 Single-Layer PCB with Access to a Ball on an Inner Ring:

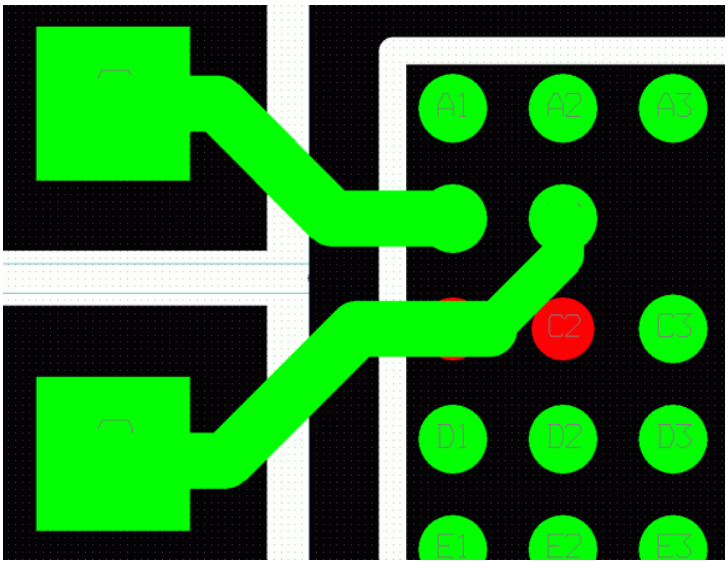


Figure 9: Access to the inner ring

Figure 9 shows an illustration example of getting access to ball B2 and the example is not related to the DA14585/14586 pinning. Two pins have to be sacrificed for the access. In Figure 9, pins C1 and C2 are sacrificed.

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Revision History

Revision	Date	Description
1.0	17-MAR-2017	Initial version.
1.1	25-APR-2018	Small additions. See details below.
1.2	18-MAY-2018	Graphical and textual improvements
Change details: ● C8 changed to 1 µF in Figure 1 and Figure 2. ● Added some description texts regarding noise in section 5.4.		
1.3	22-FEB-2022	Updated logo, disclaimer, copyright.

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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