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## Application Note

# Avalanche Guarantee for Power MOS FET

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## INTRODUCTION

In recent years, power MOS FETs have shown a dramatic improvement in their performance and their usage has been increasingly diversified and expanded. Market needs for power MOS FETs have been growing, especially in fields where high current and high switching speed are required, because power MOS FETs, as compared with bipolar power transistors, have high switching speed, low dissipation, and large SOA (Safe Operating Area). Recent progress in electronic control in the automotive electric component field is one of the factors that diversify the market needs for power MOS FETs. The growth of the market needs has led to the diversification of operating conditions and environmental conditions of power MOS FETs, and it is now very important to select a product optimal for circuit constants and mounting conditions of the circuit in which the product is to be used.

One of the most important criteria for selecting a power MOS FET is capability performance. In other words, a sufficient margin must be secured for the capability performance with respect to the operating voltage. However, recent demands for power MOS FETs with high performance and, at the same time, being light-weight and compact have made it increasingly difficult to select a high-performance power MOS FET while securing a sufficient margin.

The specifications of avalanche capability specify (guarantee) that a power MOS FET can be operated safely under specific conditions even if the surge voltage, which is generated when (immediately after) the switching operation under an inductive load is turned off, exceeds the rated breakdown voltage (voltage between the drain and source), assuming that the surge voltage exceeds the rated breakdown voltage of the power MOS FET, reaches its breakdown region, and breaks down the FET. Products with guaranteed avalanche capability have the avalanche current ( $I_{AS}$  or  $I_{AR}$ ) and avalanche energy ( $E_{AS}$  or  $E_{AR}$ ) values specified as absolute maximum ratings on the Data Sheet of each product.

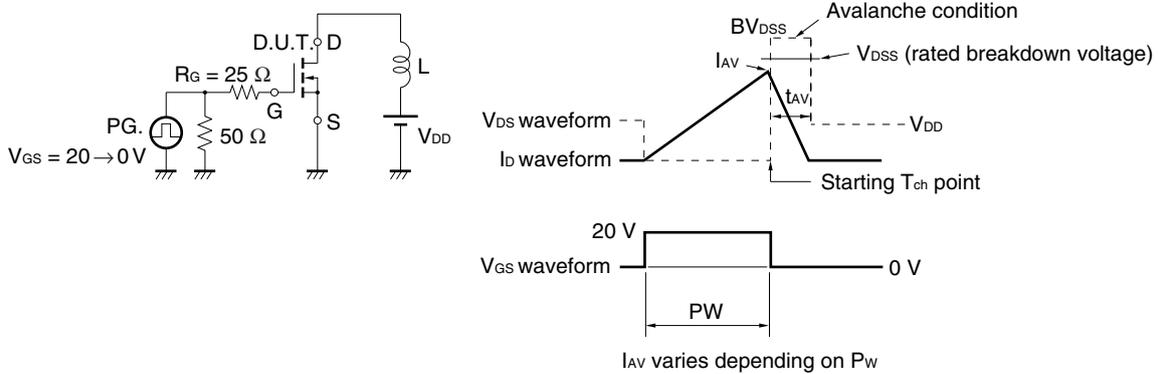
This Application Note focuses on power MOS FET avalanche capability, and explains the application method of avalanche operation and avalanche capability rating, and how to apply ratings to an actual circuit. Please use this Application Note for your reference when selecting a product.

- Remarks**
1. In this document, power MOS FETs are simply referred to as “FETs”.
  2. Inductance is expressed as an “L load” or “L”.
  3. In this Application Note, the avalanche capability specification parameters used in the Data Sheet of each product, which are expressed as “ $I_{AS}$  and  $I_{AR}$ ” or “ $E_{AS}$  and  $E_{AR}$ ”, are referred to as “ $I_{AV}$ ” or “ $E_{AV}$ ”, respectively.  $I_{AV}$  may be taken as  $I_{AS}$  and  $I_{AR}$ , and  $E_{AV}$ , as  $E_{AS}$  and  $E_{AR}$ .

## 1. Avalanche Operation

**Figure 1** shows the operation waveforms of  $V_{GS}$ ,  $V_{DS}$ , and  $I_D$  (avalanche operation waveforms) of an FET in a circuit equivalent to a switching circuit that turns on or off an L load by applying a pulse of  $V_{GS} = 20 \rightarrow 0$  V between the gate and source of the FET.

**Figure 1. L Load Switching Circuit and Avalanche Operation Waveform of FET**



The avalanche operation (avalanche condition) of an FET is the FET operation during the  $t_{AV}$  period in **Figure 1**. Note that, in this figure, the avalanche voltage is expressed as  $BV_{DSS}$ , the avalanche current as  $I_{AV}$ , and the channel temperature of the FET immediately before the avalanche operation as starting  $T_{ch}$ .

The operation of the FET in **Figure 1** is explained in detail below.

1. When the FET is turned on by applying a voltage of 20 V to  $V_{GS}$ ,  $V_{DS}$  falls toward  $V_{DS(on)}$ . At the same time,  $I_D$  starts flowing and linearly increases as time passes (energy is built up on the L load).
2. If the FET is turned on for the duration of  $P_w$  and then off with  $V_{GS}$  at 0 V, the energy built up on the L load is discharged, causing  $V_{DS}$  to rise rapidly.  $V_{DS}$  exceeds the voltage between the drain and source (rated breakdown voltage:  $V_{DSS}$ ) and stabilizes at the effective breakdown voltage ( $BV_{DSS}$ ). (The energy that has been built up is absorbed by the FET as avalanche energy).
3. The status of  $BV_{DSS}$  lasts until the energy built up on the L load is completely discharged ( $t_{AV}$ ). After that, it decreases to the  $V_{DD}$  level.
4.  $I_D$  peaks at  $I_{AV}$  immediately before the FET is switched off, and then linearly decreases toward zero within the duration of  $t_{AV}$ .

$I_{AV}$  changes depending on the L value of the L load and the ON time ( $P_w$ ) of the FET. Therefore, it tends to increase if the L value decreases or if the ON time ( $P_w$ ) of the FET is extended.

$t_{AV}$  is determined by the relationship between the L value and  $I_{AV}$ . However,  $t_{AV}$  is prolonged if the L value increases while  $I_{AV}$  remains the same or if  $I_{AV}$  increases while the L value remains the same.

**Caution** A breakdown status of the FET caused by a surge voltage generated from the power supply circuit at a timing other than that shown above (timing not immediately after the FET has been switched off) is not defined as the avalanche operation described in this Application Note. Note that, generally, a breakdown of the FET at such a timing is not guaranteed.

## 2. Avalanche Failure Mechanism

Avalanche failure is a mode in which an FET breaks down (is destroyed) due to a surge voltage, which is generated when (immediately after) the switching operation under an inductive load, exceeds the rated breakdown voltage of the FET. The FET breaks down in the following two modes during an avalanche operation.

1. Current failure mode
2. Energy failure mode

Each of these failure modes is explained below.

### 2.1 Avalanche Failure Mode I <<Current Failure>>

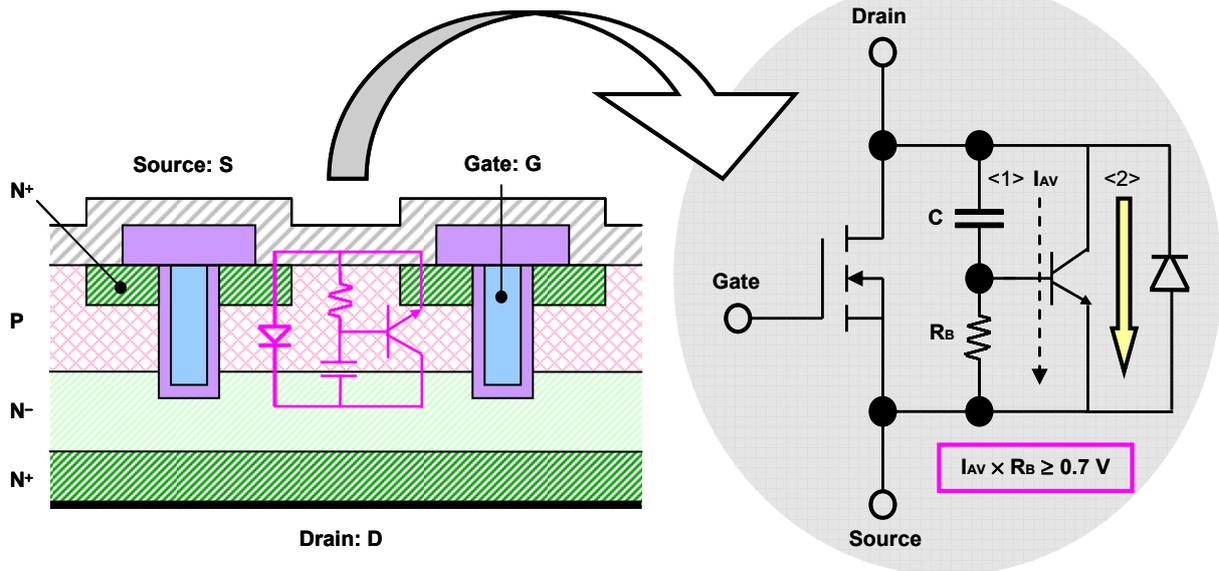
An FET consists of an assembly of many small FET cells (that are connected in parallel). In particular, products operating at low voltage of 250 V or less employ a structure in which each FET cell is miniaturized to lower the ON resistance of the element and a trench is formed on the surface into which a gate is embedded (to reduce the FET cell area) (NEC Electronics calls this a UMOS structure), in order to improve the performance. **Figure 2** shows the cross-sectional view of an FET cell and equivalent circuit of a trench structure FET chip. The cross-sectional view in this figure shows an NPN parasitic transistor comprised among the  $N^+$  layer connected to the source electrode, P layer that forms a channel, and the  $N^-$  layer on the drain side.

How a current failure occurs with an FET structure as mentioned above is described next.

- (1) If a voltage exceeding the rated value is applied between the drain and source, a breakdown current (avalanche current:  $I_{AV}$ ) flows.
- (2) This current ( $I_{AV<1>}$ ) flows from the drain, through the resistance component ( $R_B$ ) of the P layer, to the source via the parasitic capacitance (C).
- (3) If  $I_{AV}$  increases and the voltage on both ends of  $R_B$  rises above the  $V_{BE}$  ON voltage of the parasitic NPN transistor, the NPN transistor is turned on.
- (4) As a result, an excessive current ( $I_{AV<2>}$ ) which has been amplified by the parasitic transistor flows to the collector side, generating heat due to high current that eventually destroys the parasitic transistor (= FET).

To avoid such a current failure, the parasitic capacitance (C) and resistance component ( $R_B$ ) must be lowered as much as possible when designing the cell structure. A current failure is also influenced by temperature. The higher the temperature, the smaller the current by which the FET is destroyed. Generally, however, the influence of temperature is smaller than that with the energy limit region to be explained next.

Figure 2. FET Cell Cross-Sectional Structure and Equivalent Circuit of Trench Structure FET Chip



- <1> A voltage exceeding the rated breakdown voltage ( $V_{DSS}$ ) of the element is applied and the parasitic transistor is biased by  $R_B$ .
- <2> The parasitic transistor is turned off, causing a high current to flow and destroy the cell.

## 2.2 Avalanche Failure Mode II <<Energy Failure>>

**Figure 3** shows the avalanche operation waveform in an L load switching circuit. In this figure, the channel temperature ( $T_{ch}$ ) of the FET rises during avalanche operation ( $t_{AV}$ ), because the FET consumes the energy of the avalanche voltage ( $BV_{DSS}$ ) and avalanche current ( $I_{AV}$ ).

Generally, if the absolute temperature reaches 608 K (= 335°C), a PN junction can no longer play its role, cannot be controlled by current, and breaks down, because the energy structure of the N and P semiconductors changes to the state of an intrinsic semiconductor.

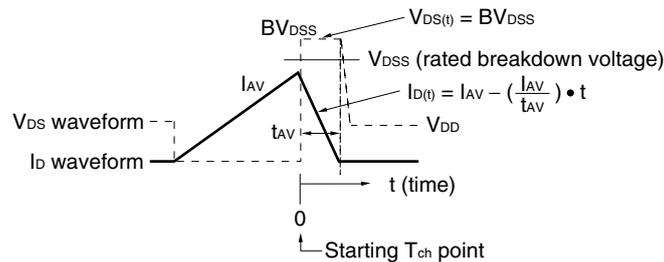
The energy failure mode indicates that energy is applied to the FET causing the PN junction to exceed the above-mentioned temperature limit and break down. The breakdown energy amount ( $E_{AV}$ ) at this time is determined by the following requirements.

- L value (in proportion to  $t_{AV}$ )
- Peak current  $I_{AV}$  flowing into the L load (in proportion to the ON time of the L load)
- Avalanche voltage  $BV_{DSS}$  of the FET

Since an energy failure is caused by a temperature rise, it is directly influenced by the channel temperature (starting  $T_{ch}$ ) immediately before an avalanche operation is started.

**Remark** The avalanche energy capability ( $E_{AS}$ ) guaranteed on the Data Sheet of each NEC Electronics product is generally that when starting  $T_{ch} = 25^\circ\text{C}$ .

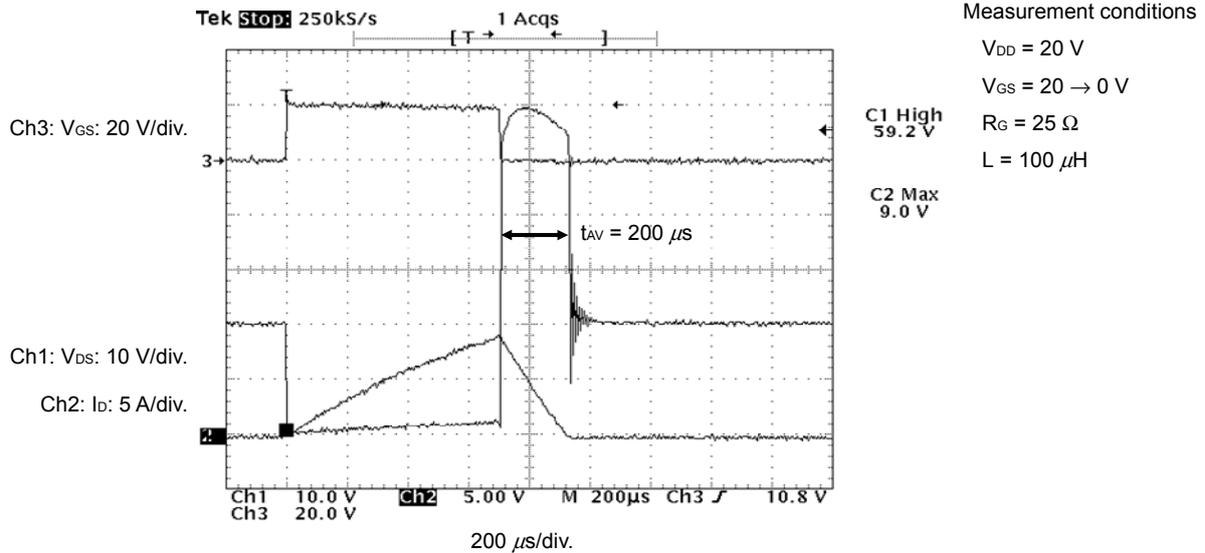
**Figure 3. Avalanche Operation Waveform in L Load Switching Circuit**



### 3. Waveform Actually Measured During Avalanche Operation (Example of Waveform Actually Measured at Breakdown Point)

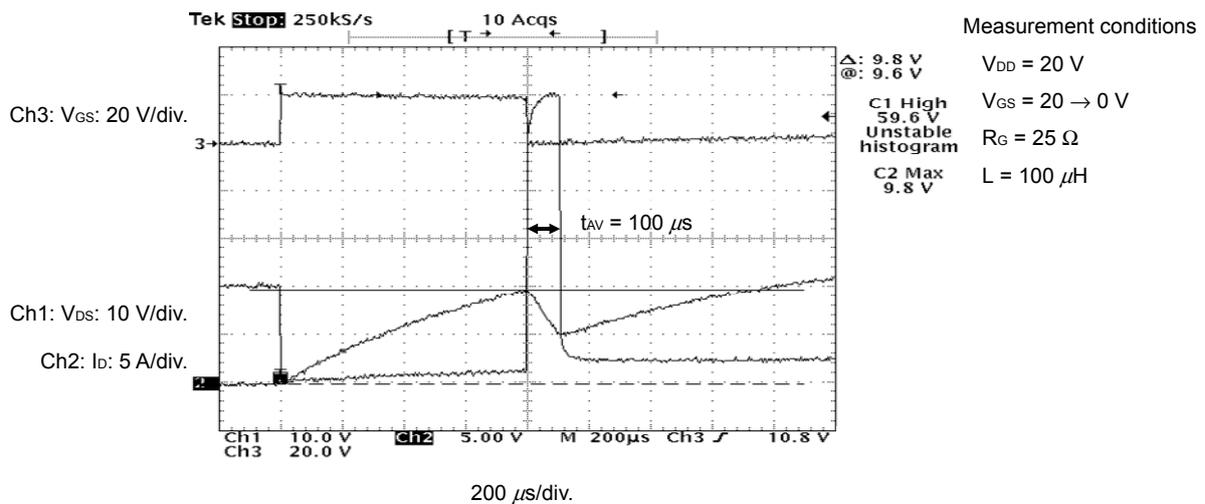
Figures 4 and 5 show examples of  $V_{DS}$  and  $I_D$  operation waveforms when an avalanche operation is actually measured. Figure 4 shows the waveforms of a normal product, and Figure 5 shows those of a defective product.

Figure 4. Example of FET Avalanche Operation (Actually Measured) Waveforms (Normal Product)



**Remark** The normal product operates normally with  $t_{AV}$  equal to about 200  $\mu s$ . No phenomenon where the current rises again (indicating FET breakdown) after the FET is turned off is observed.

Figure 5. Example of FET Avalanche Operation (Actually Measured) Waveforms (Defective Product)

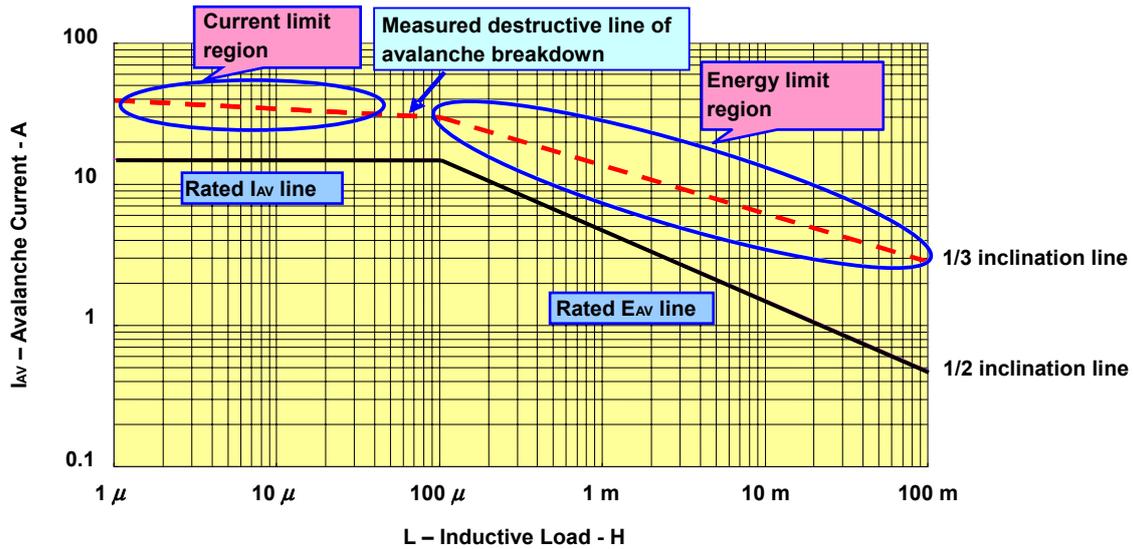


**Remark** With the defective product,  $t_{AV}$  is equal to about 100  $\mu s$ , which is much shorter than that of the normal product. In addition, a waveform such that the current increases again after the FET is turned off, indicating that the FET is broken down, is observed. In other words, the avalanche energy capability ( $E_{AS}$ ) of the defective product is less than half that of the normal product.

#### 4. Application Method of Measured Destructive Value and Rated Value of Avalanche Breakdown Capability

Figure 6 shows the relationship among the measured destructive and rated lines of the avalanche breakdown capability, and the measurement constant L value of an FET.

Figure 6. Relationship among Measured Destructive and Rated Lines of Avalanche Breakdown Capability and L Value



**Caution** The condition for the measured destructive and rated lines is starting  $T_{ch} = 25^{\circ}\text{C}$ . Derating due to starting  $T_{ch}$  must be considered for the measured destructive and rated lines.

Details of Figure 6 are described below.

The dotted line indicates the measured destructive line of avalanche breakdown of an FET. This line was drawn by actually measuring and plotting the avalanche current ( $I_{AV}$ ) at breakdown points by varying the L value. On this measured destructive line, the region where the L value is small and  $I_{AV}$  is large is the avalanche current limit region. In this region, the current value level remains almost flat, because it is not affected much by the L value.

The rated  $I_{AV}$  line, which indicates the safe operation range, has a sufficient margin with respect to the measured destructive line, and has a constant current value (about 50% of the measured destructive breakdown value). This is called the rated avalanche current value (rated  $I_{AV}$  value).

On the other hand, the region where the L value is large is the energy limit region. This region is dominated by the avalanche energy ( $E_{AV}$ ) that raises the channel temperature of the FET. When the channel temperature rises to about  $335^{\circ}\text{C}$ , the breakdown point is reached.

The rated  $E_{AV}$  line slopes down to the right with a further margin secured from the line that is calculated to fall below the maximum rated value of the channel temperature. The energy calculated from  $I_{AV}$  and the L value on this rated line is constant, and this value is the rated avalanche energy value (rated  $E_{AV}$  value).

To check the avalanche operation as described above, therefore, both the avalanche current ( $I_{AV}$ ) and avalanche energy ( $E_{AV}$ ) must be specified. At the same time, derating due to temperature rise is also considered. This means that starting  $T_{ch}$  immediately before the actual avalanche operation must be calculated, that derating due to temperature rise must be considered, and that a judgment must be made as to whether the result is within the rated avalanche range.

Generally, the rated values of starting  $T_{ch} = 25^{\circ}\text{C}$  are specified as the absolute maximum ratings for  $I_{AV}$  and  $E_{AV}$  on the Data Sheet of each product. As parameters,  $I_{AS}$  or  $I_{AR}$  is equivalent to  $I_{AV}$ , and  $E_{AS}$  or  $E_{AR}$ , to  $E_{AV}$ . The relationship with the L value and derating characteristics due to starting  $T_{ch}$  are also described as characteristic curves on the Data Sheet.

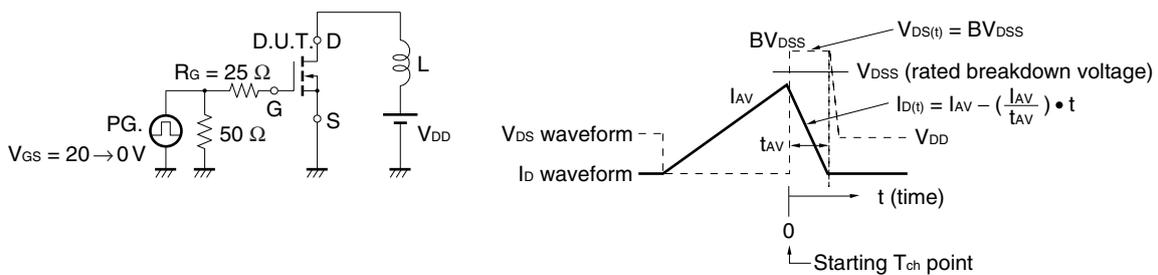
#### 4.1 Avalanche Capability Ratings: Relationship of $E_{AV}$ and $I_{AV}$ with Inductance Value

##### <<Example of Theoretical Calculation>>

This section verifies the relationship between  $E_{AV}$  and  $I_{AV}$  of the avalanche capability ratings, and the  $I_{AV}$  measurement constant (L value), by using a theoretical expression.

Figure 7 shows an example of an avalanche capability test circuit.

Figure 7. Avalanche Capability Test Circuit and Avalanche Operation Waveform of FET



The avalanche energy ( $E_{AV}$ ) in the above test circuit can be expressed as follows.

$$\begin{aligned}
 E_{AV} &= \int_0^{t_{AV}} V_{DS(t)} \cdot I_D(t) dt \\
 &= \int_0^{t_{AV}} BV_{DSS} \cdot \left( I_{AV} - \frac{I_{AV}}{t_{AV}} \cdot t \right) dt \\
 &= \int_0^{t_{AV}} BV_{DSS} \cdot I_{AV} \cdot \left( 1 - \frac{t}{t_{AV}} \right) dt \\
 &= \frac{1}{2} BV_{DSS} \cdot I_{AV} \cdot t_{AV} \quad \dots\dots <1>
 \end{aligned}$$

The time of energy discharge ( $t_{AV}$ ) is the L value multiplied by  $I_{AV}$ , divided by the voltage on both ends of L ( $BV_{DSS} - V_{DD}$ ).

$$t_{AV} = \frac{L \cdot I_{AV}}{BV_{DSS} - V_{DD}} \quad \dots\dots <2>$$

The  $t_{AV}$  values in expression <1> are substituted by <2>.

$$E_{AV} = \frac{1}{2} \cdot L \cdot I_{AV}^2 \cdot \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \quad \dots\dots <3>$$

Next, the channel temperature is verified by a theoretical expression.

$$\Delta T_{ch} = P_{AV} \cdot r_{th(t_{AV})} = \frac{1}{2} \cdot BV_{DSS} \cdot I_{AV} \cdot r_{th(t_{AV})} \dots\dots\dots <4>$$

The transient thermal resistance ( $r_{th(t_{AV})}$ ) of pulse width  $t_{AV}$  can be expressed as follows, if the transient thermal resistance of any pulse width  $P_W$  is  $r_{th(P_W)}$ .

$$r_{th(t_{AV})} = r_{th(P_W)} \cdot \sqrt{\frac{t_{AV}}{P_W}} \dots\dots\dots <5>$$

The following expression is derived by substituting values in expression <4> by expressions <5> and <2> and expressing  $\Delta T_{ch}$  as a function of  $I_{AV}$ .

$$\begin{aligned} \Delta T_{ch} &= \frac{1}{2} \cdot BV_{DSS} \cdot I_{AV} \cdot r_{th(t_{AV})} = \frac{1}{2} \cdot BV_{DSS} \cdot I_{AV} \cdot r_{th(P_W)} \cdot \sqrt{\frac{t_{AV}}{P_W}} \\ &= \frac{1}{2} \cdot BV_{DSS} \cdot I_{AV} \cdot r_{th(P_W)} \cdot \sqrt{\frac{L \cdot I_{AV}}{BV_{DSS} - V_{DD}}} \\ &= \frac{1}{2} \cdot r_{th(P_W)} \cdot \sqrt{\frac{BV_{DSS}^2 \cdot I_{AV}^2 \cdot L \cdot I_{AV}}{BV_{DSS} - V_{DD}}} \\ &= \frac{1}{2} \cdot r_{th(P_W)} \cdot \sqrt{\frac{BV_{DSS}^2 \cdot I_{AV}^3 \cdot L}{P_W \cdot (BV_{DSS} - V_{DD})}} \\ &= \frac{1}{2} \cdot r_{th(P_W)} \cdot \sqrt{\frac{BV_{DSS}^2}{P_W \cdot (BV_{DSS} - V_{DD})}} \cdot L^{\frac{1}{2}} \cdot I_{AV}^{\frac{2}{3}} \dots\dots\dots <6> \end{aligned}$$

From expression <3>, the rated line where  $E_{AV}$  is constant is as follows.

$$I_{AV} \propto L^{-\frac{1}{2}} \dots\dots\dots <7>$$

From expression <6>, the rated line where  $T_{ch} = T_{ch(max.)}$  is as follows.

$$I_{AV} \propto L^{-\frac{1}{2} \cdot \frac{2}{3}} = I_{AV} \propto L^{-\frac{1}{3}} \dots\dots\dots <8>$$

The 1/2 and 1/3 inclination lines in **Figure 6** are graphical representations of expressions <7> and <8>.

## 5. Application Method of Derating of Avalanche Capability Rating by Channel Temperature

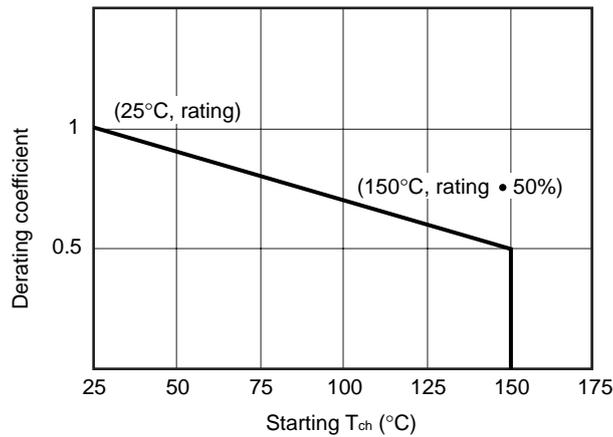
The avalanche current value ( $I_{AV}$ ) and avalanche energy value ( $E_{AV}$ ) of the avalanche capability ratings show different tendencies in starting  $T_{ch}$  derating. This chapter explains this difference.

Generally, derating due to temperature is expressed by a derating coefficient (dT) (%), and specifies the rate of avalanche capability derated by temperature rise, with starting  $T_{ch} = 25^{\circ}\text{C}$  as 100%.

### 5.1 Derating of $I_{AV}$ in Current Limit Region

**Figure 8** shows an example of derating of the rated  $I_{AV}$  value in the current limit region. If the channel temperature ( $T_{ch}$ ) of the product is  $150^{\circ}\text{C}$  maximum, the rated  $I_{AV}$  value of that product is derated to 50% with starting  $T_{ch} = 150^{\circ}\text{C}$ .

**Figure 8. Example of  $I_{AV}$  Derating Characteristics**

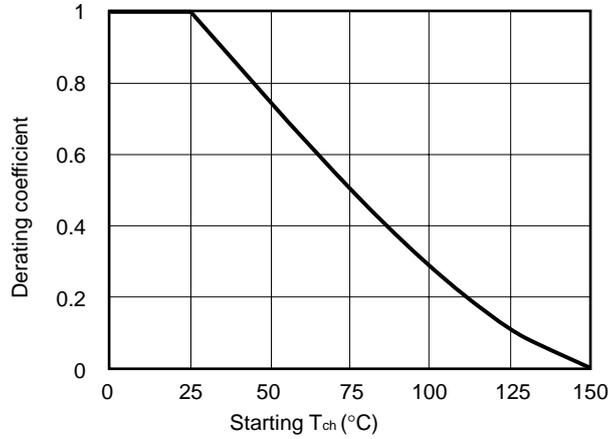


**Caution** Please be sure to check the Data Sheet when actually using the product.

## 5.2 Derating of E<sub>AV</sub> in Energy Limit Region

Figure 9 shows the derating of the rated E<sub>AV</sub> value in the energy limit region. If starting T<sub>ch</sub> is the maximum value of the channel temperature (T<sub>ch</sub>) of the product, the derating coefficient is 0%.

Figure 9. Example of E<sub>AV</sub> Derating Characteristics



Next, a theoretical expression is used to verify derating of the rated E<sub>AV</sub> value in the energy limit region. The following expression can be obtained from expression <6> shown in section 4.1.

$$I_{AV} = \left( \frac{\Delta T_{ch}}{\frac{1}{2} \cdot r_{th}(P_w) \cdot \sqrt{\frac{BV_{DSS}^2}{P_w \cdot BV_{DSS} - V_{DD}}} \cdot L^{\frac{1}{2}}} \right)^{\frac{2}{3}}$$

I<sub>AV</sub> in expression <3> shown in section 4.1 is substituted by this expression.

$$\begin{aligned} E_{AV} &= \frac{1}{2} \cdot L \cdot I_{AV}^2 \cdot \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \\ &= \frac{1}{2} \cdot L \cdot \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \cdot \left( \left( \frac{\Delta T_{ch}}{\frac{1}{2} \cdot r_{th}(P_w) \cdot \sqrt{\frac{BV_{DSS}^2}{P_w \cdot (BV_{DSS} - V_{DD})}}} \cdot L^{\frac{1}{2}}} \right)^{\frac{2}{3}} \right)^2 \\ &= \frac{\frac{1}{2} \cdot L \cdot \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}}{\left( \left( \frac{1}{2} \cdot r_{th}(P_w) \cdot \sqrt{\frac{BV_{DSS}^2}{P_w \cdot (BV_{DSS} - V_{DD})}}} \cdot L^{\frac{1}{2}} \right)^{\frac{2}{3}} \right)^2} \cdot (\Delta T_{ch}^{\frac{2}{3}})^2 \\ &= \frac{\frac{1}{2} \cdot L \cdot \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}}{\left( \left( \frac{1}{2} \cdot r_{th}(P_w) \cdot \sqrt{\frac{BV_{DSS}^2}{P_w \cdot (BV_{DSS} - V_{DD})}}} \cdot L^{\frac{1}{2}} \right)^{\frac{2}{3}} \right)^2} \cdot (\Delta T_{ch}^{\frac{4}{3}}) \end{aligned}$$

Accordingly, derating of the rated E<sub>AV</sub> value is proportional to ΔT<sub>ch</sub> to the power of 4/3.

### 5.3 Derating of I<sub>AV</sub> in Energy Limit Region

**Figure 10** shows the derating of the rated I<sub>AV</sub> value in the energy limit region. This figure shows a tendency different from the E<sub>AV</sub> derating characteristics above (in **Figure 9**).

The relationship between I<sub>AV</sub> and T<sub>ch</sub> is verified by using the following theoretical expression, with respect to derating of I<sub>AV</sub> due to the temperature in the energy limit region.

$$\Delta T_{ch} = \frac{1}{2} \cdot r_{th(P_w)} \cdot \sqrt{\frac{L}{P_w} \cdot \frac{BV_{DSS}^2}{BV_{DSS} - V_{DD}}} \cdot I_{AV}^{\frac{3}{2}}$$

is converted from expression <6> to derive the following equation.

$$\frac{\Delta T_{ch1}}{\Delta T_{ch2}} = \left( \frac{I_{AV1}}{I_{AV2}} \right)^{\frac{3}{2}}$$

If ΔT<sub>ch1</sub> is any temperature (0 ≤ ΔT<sub>ch1</sub> ≤ T<sub>ch(max.)</sub> – 25°C), ΔT<sub>ch2</sub> = T<sub>ch(max.)</sub> – 25°C, I<sub>AV1</sub> the value at ΔT<sub>ch1</sub>, and I<sub>AV2</sub> the standard of the product, the following equation results.

$$\frac{\Delta T_{ch1}}{T_{ch(max.)} - 25^\circ C} = \left( \frac{I_{AV1}}{I_{AV2}} \right)^{\frac{3}{2}}$$

Therefore, the following equation results.

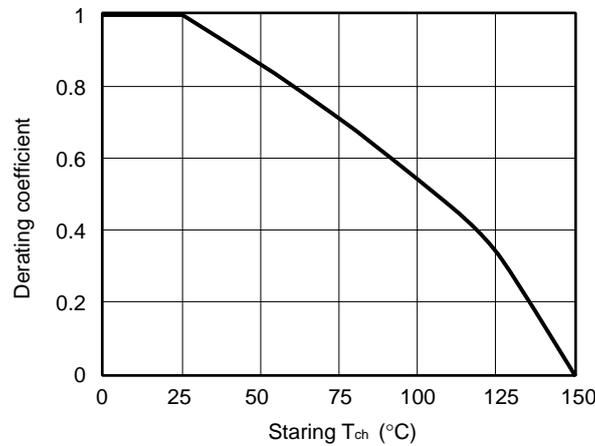
$$\frac{I_{AV1}}{I_{AV2}} = \left( \frac{\Delta T_{ch1}}{T_{ch(max.)} - 25^\circ C} \right)^{\frac{2}{3}}$$

Since  $\frac{I_{AV1}}{I_{AV2}}$  can be replaced by the derating coefficient (dT) and ΔT<sub>ch1</sub> = T<sub>ch(max.)</sub> – Starting T<sub>ch</sub>, the following expression can be derived.

$$dT = \left( \frac{T_{ch(max.)} - \text{Starting } T_{ch}}{T_{ch(max.)} - 25^\circ C} \right)^{\frac{2}{3}}$$

This expression is shown in **Figure 10**.

**Figure 10. Example of I<sub>AV</sub> Derating Characteristics**



**Caution** Whether E<sub>AV</sub> derating characteristics or I<sub>AV</sub> derating characteristics are employed as the derating characteristics due to starting T<sub>ch</sub> differs depending on the product. Please be sure to check the Data Sheet when actually using the product.

## 6. Concept of Avalanche Capability During Single Pulse Operation and Repetitive Pulse Operation

The definitions of avalanche capability rating of an actual product are broadly classified into the following two types.

1. Definition under the condition of single pulse avalanche operation
  - Single avalanche current ( $I_{AS}$ )
  - Single avalanche energy ( $E_{AS}$ )
2. Definition under the condition of repetitive pulse operations
  - Repetitive avalanche current ( $I_{AR}$ )
  - Repetitive avalanche energy ( $E_{AR}$ )

Depending on the product, some products permit only single operation while others permit repetitive operations. Generally, single operation and repetitive operation specification have the same rated value. However, the rated value differs depending on the products, so please be sure to check the Data Sheet of each product.

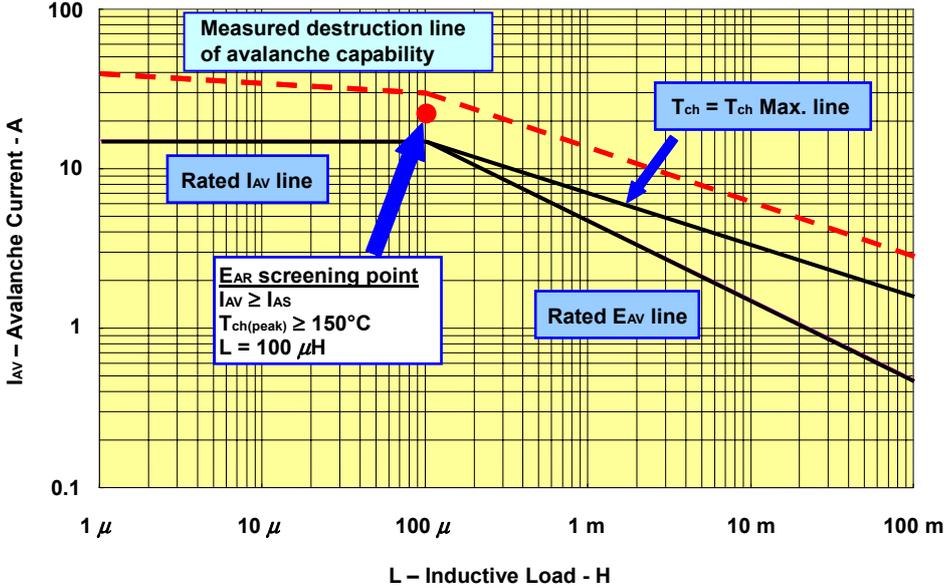
**Remark** Symbols  $I_{AV}$  and  $E_{AV}$  shown in this document may be taken as " $I_{AS}$  and  $I_{AR}$ " or " $E_{AS}$  and  $E_{AR}$ ".

## 7. Avalanche Testing

The test to measure avalanche capability is a destructive test, so the same sample cannot be repeatedly tested without being destroyed. Therefore, process design is performed for the high-avalanche-capability FET series of NEC Electronics, on the premise of guaranteeing avalanche operation. To incorporate the avalanche capability ratings for screening products in the production stage of FETs, a sufficient margin is secured from the avalanche failure line (measured destructive line) to prevent the degradation of normal products, and appropriate conditions are set for testing. Moreover, in consideration of variations in the production process, a test method is employed to perform avalanche test on all products and remove defective products.

Usually, effective screening conditions for the two failure modes, as shown in **Figure 11**, are determined in the production process. Because the two failure modes switch at a point where  $L$  is equal to about  $100 \mu\text{H}$  in many cases, it is effective to perform pinpoint screening of the products (which is performed at  $I_{AS}$  at the midpoint between the measured destructive line and rated line) at a point where  $L = 100 \mu\text{H}$ . The optimal screening point is specified for each product each time.

Figure 11. Example of Conditions for Screening Avalanche Capability Ratings in Production Process



## 8. Example of Safe Operation Judgment of Avalanche Capability in Actual Operation Waveform

This chapter describes an example of safe operation judgment related to the avalanche operation used in practice. As a prerequisite, the avalanche current ( $I_{AV} = I_{D2}$ ) used in practice must be less than the rated avalanche current value. If the avalanche current exceeds the rated value, the ratings are not satisfied at that point.

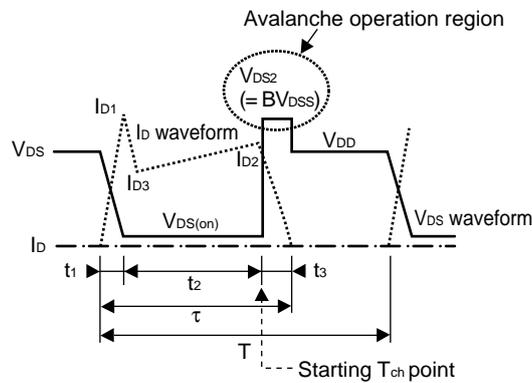
If a product has specification, safe operation judgment is required, taking derating of the avalanche current rating due to starting  $T_{ch}$  into consideration.

### 8.1 Calculating Starting $T_{ch}$

This section explains the method (procedure) for calculating starting  $T_{ch}$ , which is necessary for making a decision if a product can operate safely. The calculation method can also be applied to safe operation judgment, taking derating of the avalanche current rating due to starting  $T_{ch}$  described above into consideration.

First, the channel temperature immediately before the avalanche operation is started is calculated with an example of an actual operation waveform, such as that shown in **Figure 12**.

**Figure 12. Example of Actual Operation Waveform**



The power dissipation in this example of an actual operation waveform consists of the following three components, as shown in **Figure 13** (a).

- $P_{on}$  : Power dissipation by on resistance
- $P_{S(on)}$  : Switching power dissipation during turning on
- $P_{S(off)}$  : Switching power dissipation during turning off

Assuming that power dissipation consisting of these components continues indefinitely, the temperature rise is calculated by using the “principle of superposition”. It is easy, accurate, and effective to include into the calculation two to three waves that protrude from the average value of the entire period with respect to the power dissipation waveforms. Specifically, the following power dissipation averaged during period  $T$ , as shown in the approximation **Figure 13** (b) of power dissipation waveforms, is applied.

$$P_{av} = \frac{1}{T} \int_0^T P_T dt = \frac{\tau}{T} \cdot P_\tau$$

The average power dissipation during period  $\tau$  is then calculated by integrating the average value of  $P_{on}$ ,  $P_{S(on)}$ , and  $P_{S(off)}$  during period  $\tau$ .

$$P_\tau = \frac{1}{\tau} \int_0^\tau P_T dt$$

Power dissipation of the difference between  $P_\tau$  and  $P_{av}$  is applied for the duration  $T + \tau - t_3$ . Next, negative power dissipation,  $-P_\tau$ , is applied for  $T - t_3$ . Similarly,  $P_{on}$  and  $-(P_{S(on)} - P_{on})$  is applied for  $\tau - t_3$  and  $\tau - t_1 - t_3$ , respectively, to calculate the rise in channel temperature.

The channel temperature (starting  $T_{ch}$ ) immediately before the avalanche operation is considered to be at a point immediately before  $P_{S(off)}$  is applied, so the peak channel temperature value on completion of applying  $P_{on}$  is calculated by the following expression.

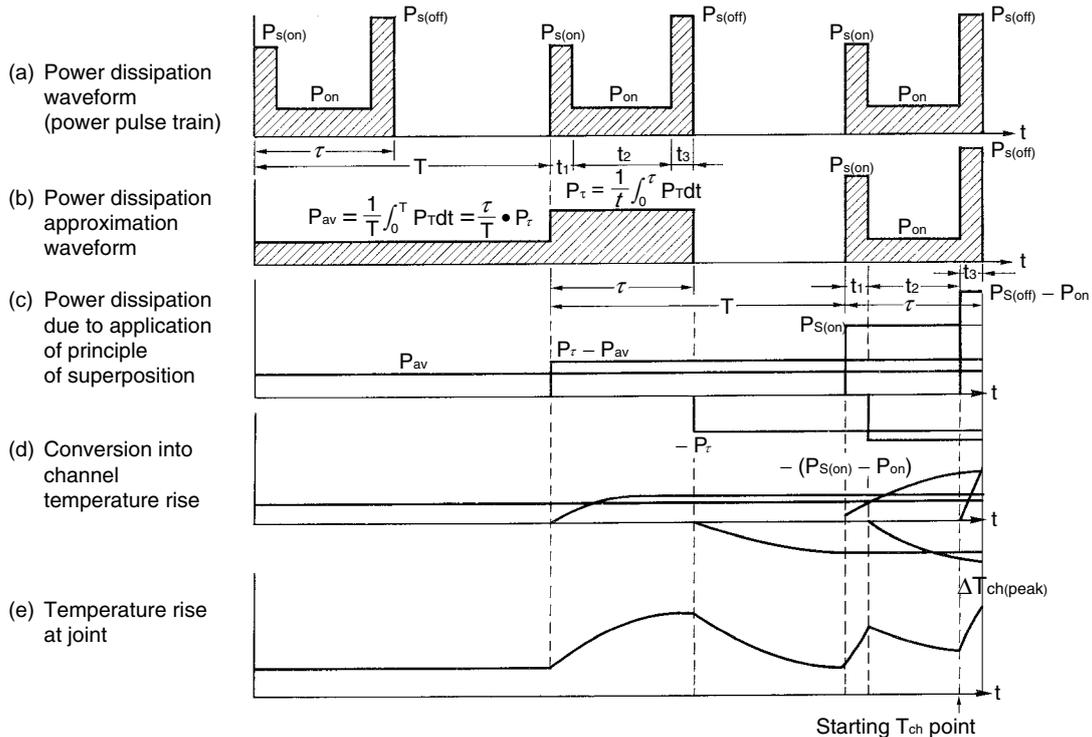
$$\begin{aligned} \Delta T_{ch(peak)} = & P_{av} \cdot R_{th(ch-c)} + (P_\tau - P_{av}) \cdot r_{th(ch-c)}(T + \tau - t_3) \\ & - P_\tau \cdot r_{th(ch-c)}(T - t_3) + P_{S(on)} \cdot r_{th(ch-c)}(\tau - t_3) \\ & - (P_{S(on)} - P_{on}) \cdot r_{th(ch-c)}(t_2) \end{aligned}$$

The sum of the result of this expression and the case temperature of the FET is starting  $T_{ch}$ . In other words, starting  $T_{ch} = T_c + \Delta T_{ch(peak)}$ .

**Remark** The meanings of the symbols are described below.

- $\tau$ : Pulse width of power dissipation (=  $t_1 + t_2 + t_3$ ) (s)
- $T$ : Cycle( $1/f$ ) (s)
- $P_\tau$ : Average power dissipation during pulse width  $\tau$  (W)
- $P_{av}$ : Average power dissipation in one cycle (W)
- $t_1$ : Switching time when turned off (s)
- $t_2$ : On time (s)
- $t_3$ : Switching time when turned on (s)
- $R_{th(ch-c)}$ : Steady state thermal resistance between FET channel and cases
- $r_{th(ch-c)}(t)$ : Transient thermal resistance between FET channel and cases at pulse width (t) ( $^{\circ}C/W$ )
- $T_c$ : FET case temperature ( $^{\circ}C$ )
- $\Delta T_{ch(peak)}$ : Maximum channel temperature rise from case temperature ( $^{\circ}C$ )

**Figure 13. Calculating Power Dissipation Waveform and Channel Temperature During Steady State Period**



## 8.2 Calculating Avalanche Energy and Example of Safe Operation Judgment

This section explains how to calculate the avalanche energy of the actual operation waveform in **Figure 12**.

In **Figure 12**, the status of  $V_{DS} = BV_{DSS}$  is the avalanche operation. Its energy can be calculated by the following expression.

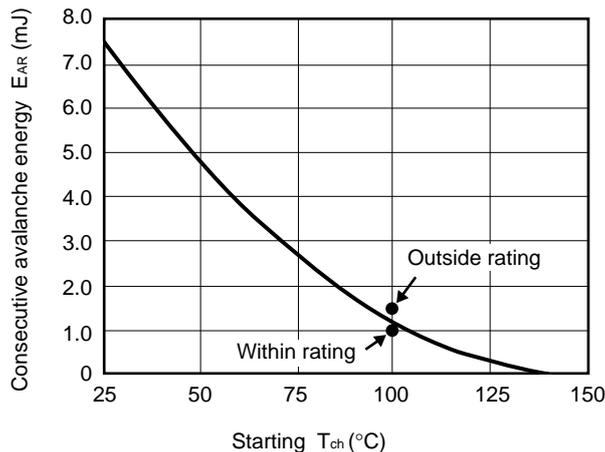
$$E_{AV} = P_{S(off)} \times t_3 \text{ (J)}$$

Usually, the rated avalanche energy value at room temperature ( $T_A = 25^\circ\text{C}$ ) is specified in the Data Sheet of avalanche-guaranteed products. This rated value is derated by the starting  $T_{ch}$  in actual operation, and is compared with the  $E_{AV}$  calculated above. If  $E_{AV}$  is within the range of the derating characteristics (derating curve), the product operates safely. To be more specific, if the  $E_{AV}$  and starting  $T_{ch}$  point in actual operation are plotted on the derating characteristic graph, and the plotted points are below the derating curve, the product operates safely within the rated value. If the points are above the derating curve, the rating is not satisfied.

The Data Sheet also shows derating characteristics due to starting  $T_{ch}$ , such as that shown in **Figure 14**. Use that characteristic graph to make a judgment taking derating into consideration, as described above.

- Remarks**
1. The above judgment is made on the assumption that the starting  $T_{ch}$  point in the avalanche operation region is clear. In other words,  $T_{ch}$  immediately before the avalanche operation is assumed to be starting  $T_{ch}$ . If the waveforms when the FET is turned off cannot be clearly separated because the switching operation of the FET overlaps with the avalanche operation and the starting  $T_{ch}$  point is unclear, calculate  $T_{ch}$  when the FET has been completely turned off (the point of completion, including the avalanche operation). If that value does not exceed  $150^\circ\text{C}$ , it can be judged that the product operates safely.
  2. To secure a wide margin for safer designing,  $T_{ch}$  on completion of  $PS(off)$  may be used as starting  $T_{ch}$  and the derating characteristics of the avalanche energy may be considered in making a judgment.

**Figure 14. Example of Judgment by Derating Characteristics**

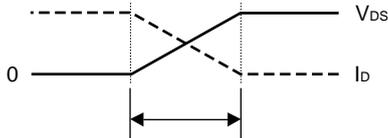


### 8.3 Calculating Average Power Dissipation within Period during which Voltage Waveform and Current Waveform Linearly Change within the Same Time

This section gives a representative example of a simple expression to calculate the average power dissipation within time where the switching waveforms of the voltage and current linearly change within the same time.

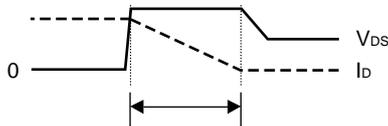
If the actual waveforms show complicated changes, the period is divided appropriately so that the changes approximate to linear changes, and the expressions for each period are used in combination for calculation.

(1) If switching waveforms cross within the same time, on a zero basis



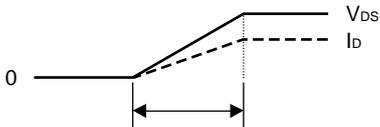
$$P = \frac{V_{DS(\text{peak})} \cdot I_{D(\text{peak})}}{6}$$

(2) If the current switching waveform is delayed, on a zero basis (L load)



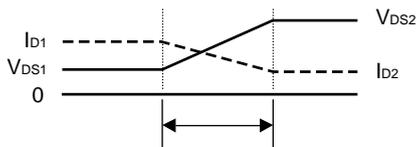
$$P = \frac{V_{DS(\text{peak})} \cdot I_{D(\text{peak})}}{2}$$

(3) If switching waveforms rise simultaneously, on a zero basis



$$P = \frac{V_{DS(\text{peak})} \cdot I_{D(\text{peak})}}{3}$$

(4) If waveforms are not on a zero basis



$$P = \frac{1}{3} \cdot (V_{DS1} - V_{DS2}) \cdot (I_{D1} - I_{D2})$$

$$- \frac{1}{2} \cdot V_{DS1} \cdot (I_{D1} - I_{D2})$$

$$- \frac{1}{2} \cdot (V_{DS1} - V_{DS2}) \cdot I_{D1} + V_{DS1} \cdot I_{D1}$$

### 8.4 Example of Judging Safe Operation from Verification Results (Summary)

This chapter 8 has explained the criteria of judging whether the actual avalanche operation is safe within the rating, including the process of verification. To sum up the above explanations, satisfying the following conditions are the prerequisites for safe operation of an FET.

- Prerequisite for safe operation 1

$$I_{AV} \leq I_{AS}, I_{AR}$$

The current value ( $I_{AV}$ ) immediately before the avalanche operation must be less than the rated values of  $I_{AS}$  or  $I_{AR}$ . If derating due to a temperature rise must be taken into consideration, the value after derating must be within the rated values.

- Prerequisite for safe operation 2

$$E_{AV} \leq E_{AS}, E_{AR}$$

The value after derating due to the temperature (starting  $T_{ch}$ ) immediately before the avalanche operation must be within the rated values.

### 8.5 Calculating Peak $T_{ch}$ Value Including Avalanche Operation Period

The methods explained up to this section have focused on how to calculate  $T_{ch}$  (starting  $T_{ch}$ ) immediately before the avalanche operation, so that a judgment can be made as to whether  $T_{ch}$  is within the rated values, by taking derating of the rated avalanche values into consideration.

If the avalanche operation time ( $t_{AV}$ ) is about 100  $\mu$ s or shorter, however, a technique that calculates the  $T_{ch(peak)}$  value, including that during the avalanche operation, by using a simple expression and, if that value does not exceed 150°C, judges that the product operates safely within the rated values may also be used. To calculate  $T_{ch}$ , including that during the avalanche operation, the temperature rise of  $T_{ch}$  immediately after completion of the avalanche operation can be calculated by using the calculation method described in 8.1 Calculating Starting  $T_{ch}$ . Generally, derating of the rated values due to the temperature rise does not have to be taken into consideration if this technique is used.

The channel temperature immediately after completion of the avalanche operation is considered to be at the point of completion of applying  $P_{S(off)}$ , so the peak channel temperature value on completion of applying  $P_{S(off)}$  is calculated by the following expression.

$$\begin{aligned} \Delta T_{ch(peak)} = & P_{av} \cdot R_{th(ch-c)} + (P_{\tau} - P_{av}) \cdot r_{th(ch-c)(T+\tau)} \\ & - P_{\tau} \cdot r_{th(ch-c)(T)} + P_{S(on)} \cdot r_{th(ch-c)(\tau)} \\ & - (P_{S(on)} - P_{on}) \cdot r_{th(ch-c)(\tau-t_1)} \\ & + (P_{S(off)} - P_{S(on)}) \cdot r_{th(ch-c)(t_3)} \end{aligned}$$

The sum of the result of this calculation and the case temperature of the FET is the channel temperature ( $T_{ch}$ ). Therefore,  $T_{ch} = T_c + \Delta T_{ch(peak)}$ . If  $T_{ch}$  in this case is less than 150°C, it can be judged that the product operates safely within the rated values.

Figure 15. Approximation Waveform of Average Power Dissipation

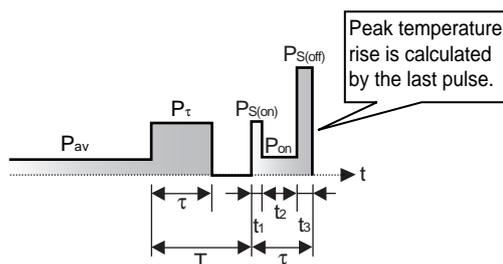
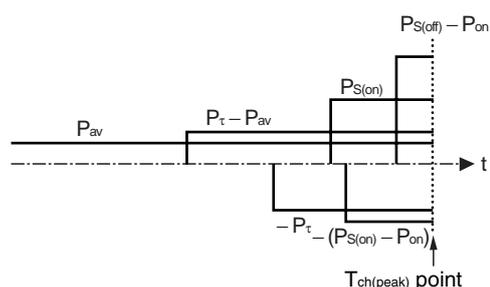


Figure 16. Limit of Power Dissipation Waveform by Principle of Superposition



## Conclusion

The avalanche capability of an FET may change depending on the circuit constants of the circuit to be used, operating conditions, and environmental conditions. It is also assumed that there are subtle differences between the specified conditions of the avalanche operation and the conditions of the circuit actually used. A judgment whether the avalanche operation can be positively performed on an application circuit must therefore evaluate the actual operation circuit thoroughly and secure a sufficient margin.

The avalanche capability specifications of an FET product on the Data Sheet of each product should be given priority. Before using the product, therefore, be sure to check the specifications on the Data Sheet.

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