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Renesas Electronics Corporation

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APPLICATION OF N-ch POWER MOS FET 2SK278 TO 200 kHz SWITCHING REGULATOR

APPLICATION NOTE

APPLICATION OF N-ch POWER MOS FET 2SK278
TO 200 KHz SWITCHING REGULATOR

1. INTRODUCTION

The switching regulators are miniaturized very rapidly in order to satisfy the increasingly rigid requirements of equipment designers. Technical improvements on their elements and applications are introduced so quickly one after another.

The most significant trend of all is that the operating frequency of typical switching regulators has been successively raised from the previous level of 20 kHz to 50 kHz or even 100 kHz today. This realizes corresponding improvements of frequency characteristics of various devices and their applicability in elevated frequency environments.

It is against such background that Nippon Electric Company (NEC) is proud to offer on production basis N-ch power MOS FET 2SK278, a switching device designed to be compatible with 200 kHz which is the operating frequency level any next-generation switching regulators will naturally be required to attain.

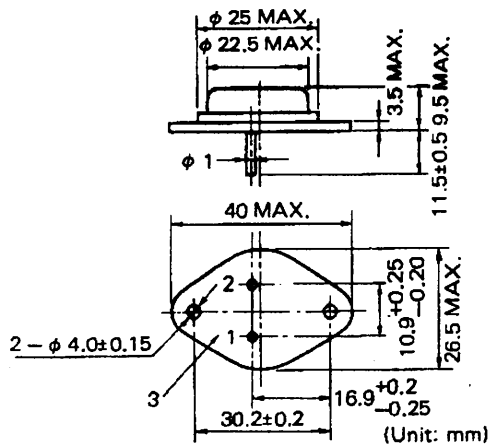
In order to show an example of promising application potentials of 2SK278, this brochure describes a 200 kHz, 5 V, 10 A output forward type switching regulator where 2SK278 is used as the main switching device in combination with other elements capable of operating in 200 kHz environments.

2. GENERAL DESCRIPTION OF 2SK278

The absolute maximum ratings, electrical characteristics and external dimensions of 2SK278 are shown in Tables 1 and 2 and Fig. 1 respectively.

Table 1. Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

ITEM	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Drain to Source Voltage	V_{DS}	$V_{GS} = 0$	400	V
Gate to Source Voltage	V_{GS}	$V_{DS} = 0$	± 20	V
Continuous Drain Current	$I_D(\text{DC})$		7.0	A
Peak Drain Current	$I_D(\text{pulse})$	$PW \leq 10 \text{ ms}$ duty cycle $\leq 50 \%$	10	A
Total Power Dissipation	P_T	$T_C = 25^\circ\text{C}$	100	W
Maximum Channel Temperature	T_{ch}		150	$^\circ\text{C}$
Storage Temperature	T_{stg}		$-65 \sim +150$	$^\circ\text{C}$



1. Gate
2. Source
3. Drain
EIAJ : TC-3, TB-3
JEDEC : TO-3
IEC : C14A, B18

Schematic Diagram

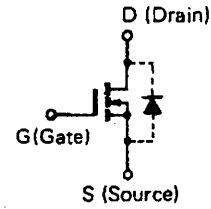


Fig.1 2SK278 Package Dimensions

Table 2. Electrical Characteristics (Ta = 25 °C unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source Breakdown Voltage	BV_{DSS}	400			V	$V_{GS} = 0$ $I_D = 10 \text{ mA}$
Gate Cutoff Current	I_{GSS}			±100	nA	$V_{DS} = 0, V_{GS} = \pm 20 \text{ V}$
Drain Cutoff Current	I_{DSS}			10	mA	$V_{DS} = 400 \text{ V}, V_{GS} = 0$
Gate to Source Cutoff Voltage	$V_{GS}(\text{off})$	0.4	1	3	V	$V_{DS} = 10 \text{ V}, I_D = 50 \text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	0.6	1.0		S	$V_{DS} = 10 \text{ V}, I_D = 3 \text{ A}$
Drain to Source On Resistance	$R_{DS}(\text{ON})$		1.0	1.5	Ω	$V_{GS} = 15 \text{ V}, I_D = 4 \text{ A}$
Input Capacitance	C_{iss}		950	1500	pF	$V_{DS} = 10 \text{ V}, V_{GS} = -5 \text{ V},$ $f = 1 \text{ MHz}$
Output Capacitance	C_{oss}		600		pF	
Reverse Transfer Capacitance	C_{rss}		10		pF	
Turn-on Delay Time	$t_d(\text{on})$		20	50	ns	$I_D = 2 \text{ A}, V_{GS(\text{on})} = 10 \text{ V},$ $V_{GS(\text{off})} = 0, R_L = 75 \Omega,$ $V_{CC} \approx 150 \text{ V}, PW = 1 \mu\text{s},$ duty cycle $\leq 1 \%$
Rise Time	t_r		20	50	ns	
Turn-off Delay Time	$t_d(\text{off})$		25	50	ns	
Fall Time	t_f		35	50	ns	

2SK278 is an N-channel MOS FET of vertical configuration, using the case as the drain. As it is also an enhancement type MOS FET, it is used in the same bias condition as the conventional bipolar NPN transistors as long as due attention is paid to the fact that its gate is voltage driven.

In addition its V_{DS} is rated at 400 V and its on-state resistance ($R_{DS(on)}$) is relatively small as the MOS FETs go while it attains a very high switching speed. These distinctive features join to justify the use of 2SK278 as an AC 100 V line operating type switching regulator in the frequency range of more than 100 kHz where the conventional bipolar transistors fail to respond quickly enough.

The structure of 2SK278 and external appearance of its element are shown in Figs. 2 and 3 respectively.

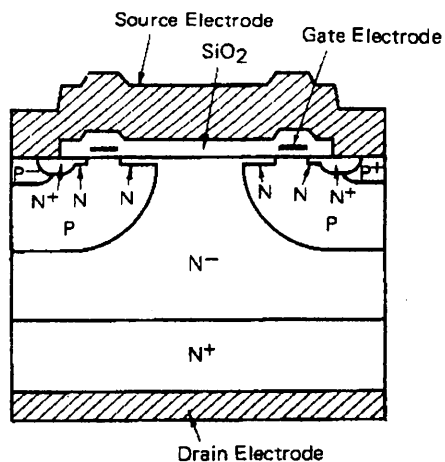


Fig.2 2SK278 Structure

Equivalent circuit of this device (see below) can be described as a cascading connection of three FETs. Junction FETs FET-3 and FET-2 have high breakdown voltage, and protect MOS FET stage FET-3 from high voltage exposure.

By this fact, 2SK278 can have high Drain to source breakdown voltage.

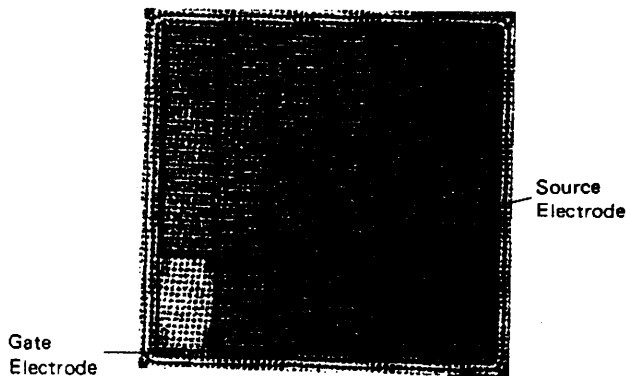
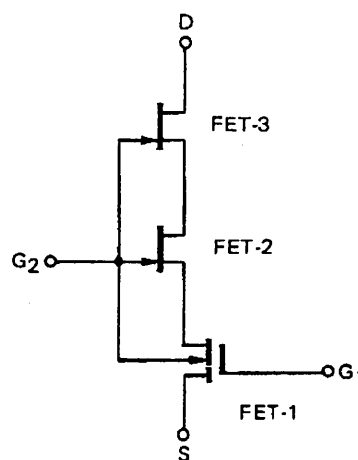


Fig. 3 Photograph of Die of 2SK278



Note:

G₁ : Gate Electrode of FET-1

G₂ : Gate Part of Equivalent
Junction FETs FET-2
and FET-3

Equivalent Circuit

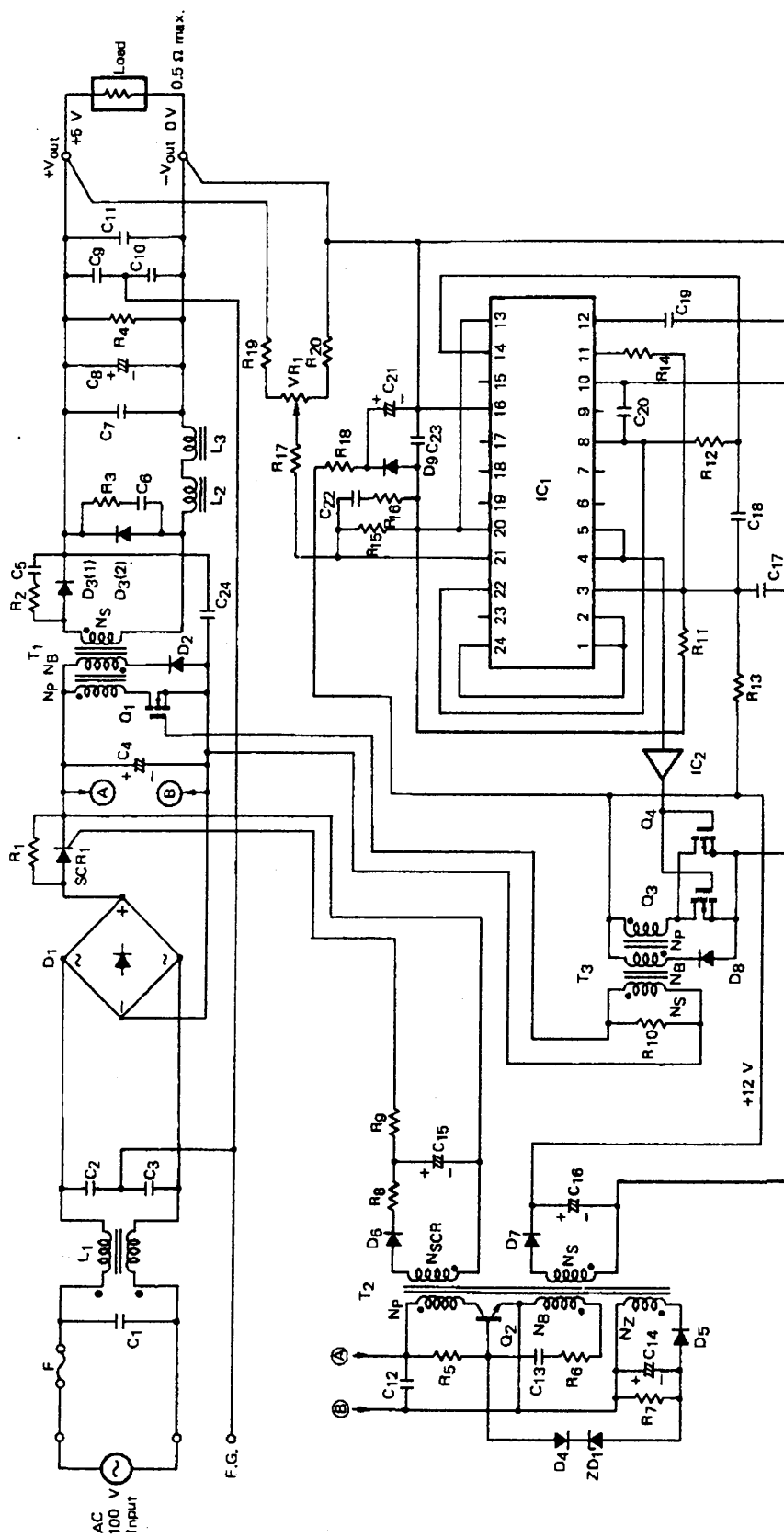


Fig.4 200 kHz Forward Type Switching Regulator Circuit

Table 3. Parts List

YMBOL	NAME	RATINGS	SYMBOL	NAME	RATINGS
C ₁ ~C ₃	Film Capacitors	0.22 μ F, 500 V	Q ₁	Power MOS FET	2SK278 (400 V, 7 A) NEC
C ₄	Al electrolytic capa.	470 μ F, 160 V	Q ₂	V MOS FET	2SC2752 400 V, 2 A TO-128 NEC
C _{5, 6}	mylar film capa.	1000 pF, 50 V	Q ₃ , Q ₄		VN66AF (60 V, 2 A) Siliconix
C ₇	film capa.	2.2 μ F, 50 V			
C ₈	Al electrolytic capa.	4700 μ F, 16 V			
C _{9, 10}	film capa.	0.22 μ F, 500 V			
C ₁₁	mylar film capa.	0.47 μ F, 50 V	R ₁	cement resistor	15 Ω , 5 W
C ₁₂	film capa.	0.068 μ F, 200 V	R _{2, 3}	carbon film resistor	4.7 Ω , 1/2 W
C ₁₃	mylar film capa.	1500 pF, 50 V	R ₄	solid resistor	50 Ω , 1 W
C ₁₄	Al electrolytic capa.	33 μ F, 16 V	R ₅	carbon film resistor	150 k Ω
C ₁₅	"	150 μ F, 10 V	R ₆	"	100 Ω
C ₁₆	"	330 μ F, 16 V	R ₇	"	4.7 k Ω
C ₁₇	mylar film capa.	0.22 μ F, 50 V	R ₈	"	220 Ω
C ₁₈	"	1500 pF, 50 V	R ₉	"	100 Ω
C ₁₉	ceramic capa.	470 pF, 50 V	R ₁₀	"	240 Ω , 1/2 W
C ₂₀	mylar film capa.	0.22 μ F, 50 V	R _{11, 12}	"	10 k Ω
C ₂₁	Al electrolytic capa.	33 μ F, 16 V	R ₁₂	"	4.7 k Ω
C ₂₂	—	—	R ₁₃	"	150 Ω , 1/2 W
C ₂₃	mylar film capa.	1000 pF, 50 V	R ₁₄	metal film resistor	6.9 k Ω
C ₂₄	film capa.	0.1 μ F, 650 V	R ₁₅	carbon film resistor	1.5 M Ω
D ₁	bridge rectifier	2B8M (400 V, 1.5 A) NEC	R ₁₆	"	—
D ₂	first recovery diode	F114D (400 V, 0.8 A) "	R ₁₈	"	6.8 k Ω
D ₃	Schottky barrier diodes (common cathode)	20CSO4M (40 V, 20 A) "	R _{19, 20}	metal film resistor	1 k Ω
D ₄ ~D ₆	diodes	1S953 "			
D _{7, 8}	"	1S954 "	SCR ₁	SCR	5P2M (5 A, 200 V) NEC
D ₉	diode	1S953 "			
F	fuse	3 A	T ₁	Output transformer	core: PQ20/20H7C ₁ TDK N _p =27Turns, D _p =0.4 mm ϕ 3 layers N _s =4 Turns, D _s =0.4 mm ϕ 6 parallel 3 layers N _B =27Turns, D _B =0.4 mm ϕ 1 layers
IC ₁	Sw. Reg. Controller	ZN1066E Ferranti	T ₂	transformer for auxiliary power supply	core: EP-13H ₇ C ₁ TDK N _p =95Turns, D _p =0.2 mm ϕ L _p =1.75 mH N _B =4Turns, D _B =0.25 mm ϕ N _s =14Turns, D _s =0.25 mm ϕ 2 parallel 2 layers N _z =14Turns, D _z =0.25 mm ϕ N _{SCR} =4Turns, D _{SCR} =0.25 mm ϕ
IC ₂	LSTTL (Inverter)	μ PB74LS00 NEC	T ₃	pulse transformer for gate driving	core: EP-10H ₅ A TDK N _p =N _s =N _B =18 Turns D _p =D _s =D _B =0.25 mm ϕ L _p =92 μ H
L ₁	Common mode choke coil for line filter	core: T12-125 (dastcore) N ₁ =N ₂ =10Turns D=0.6 mm ϕ 2 parallel	VR ₁	Variable resistor	PN822H102H (NEOPOT) NEC
L ₂	choke coil for smoothing circuit	core: EI-22H ₇ C ₁ TDK N=6Turns D=0.6 mm ϕ 2 parallel 3 layer L=50 μ H	ZD ₁	Zenner diode	RD13EB (13 V, 400 mW) NEC
L ₃	choke coil for smoothing circuit	core: T8-125 N=8Turns D=0.7 mm ϕ 4 parallel L=4.6 μ H			

3. APPLICATION TO 200 kHz SWITCHING REGULATOR

A trial model of the 5 V, 10 A output forward type switching regulator where 2SK278 is used in the output stage, is described in the following pages.

3.1 Specifications of Power Supply

Input voltage : AC 100 V \pm 15 % (50 or 60 Hz)

Output voltage, current: DC 5 V \pm 5 %, 10 A max.

Operating frequency : $f = 200$ kHz

3.2 Design Key Points

As the trial model switching regulator must operate at a definitely high frequency than conventional switching regulators, it is necessary to introduce many improvements in terms of transformer design, etc. The more important of them incorporated in the trial model switching regulator are listed in Table 4.

Table 4. 200 kHz Switching Regular Design Key Points

ITEM	IMPROVEMENT POLICY	CONCRETE MEASURE TAKEN
Prevention of rush current into line	Adoption of slow start circuit	SCR installed in parallel to limiting resistor on line side
Miniaturization of auxiliary power supply	Adoption of DC-DC convertor	Adoption of fly-back type DC-DC convertor (simple switching regulat circuit added, $f=150$ kHz, $P_o=1.5W$).
Prevention of rush current into inverter	Adoption of soft start circuit	Control IC amplifier output provided with time constant with addition of Capacitor and Resiste.
Reduced radiation noise of secondary rectifying diode	Fixed diode case potential	Secondary choke coil installed on GND line side so that diode case potential does not fluctuate..
Output transformer frequency band extension	Reduced primary to secondary leakage inductance	Improved coil winding.
Transient response/ regulation coexistence	Adoption of combined choke coil	Two choke coils serially connected, realizing two different L values by current value.

3.3 Circuit Designs

(1) Slow start circuit

As the primary smoothing circuit is designed to receive input from capacitor C₄, this slow start circuit is used to perform charging the capacitor gradually enough to prevent the occurrence of a rush current when the switch is turned on.

Concretely charging C₄ starts through R₁. As the auxiliary power supply circuit (DC-DC convertor) of Q₂, etc. is actuated, the N_{SCR} coil generates a voltage, which is used to charge C₁₅ at a certain time constant through the time constant circuit composed of R₈ and C₁₅. The charged C₁₅ triggers SCR₁ through R_g.

In this case the surge current to SCR₁ must be provided with a sufficiently large margin against the maximum rating of $I_{TSM} = 80$ A. (Usually below 20 A)

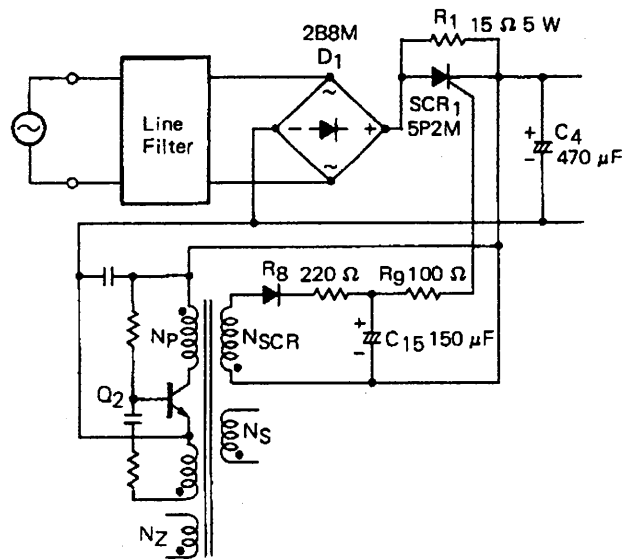


Fig.5 Slow Start Circuit

(2) Auxiliary power supply

Circuit diagram of auxiliary power supply DC-DC convertor is shown in Fig. 6. This convertor is of fly-back type, and operates as a simplified stabilizing circuit by providing the positive feedback from N_B to the base for self-excited oscillation and, at the same time, connecting output voltage of N_Z which has as many turns of winding as N_S , to the base of Q_2 through D_4 and ZD .

This convertor has NTC2752 as Q_2 and operates on the frequency of about 150 kHz. Its output profiles are roughly as follows.

- For driver control IC bias : $V_S = 14\text{ V}$
- For SCR₁ drive : $V_{SCR} = 5\text{ V}$
- For stabilization (N_Z coil output): $V_Z = 14\text{ V}$

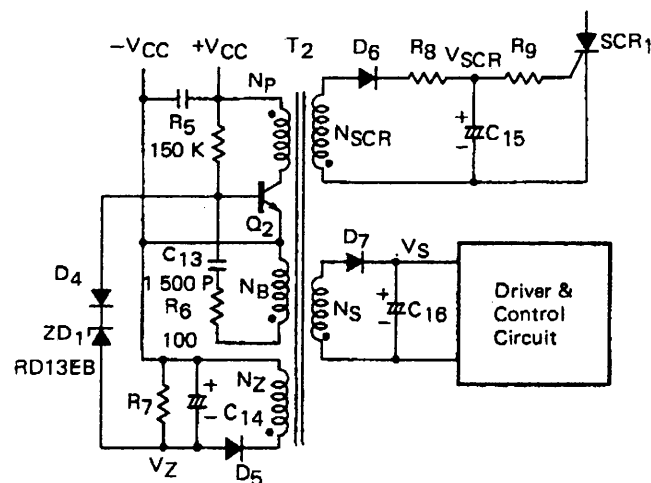


Fig.6 Auxiliary Power Supply Circuit

ABSOLUTE MAXIMUM RATINGS

Maximum Voltages and Currents ($T_a=25^\circ\text{C}$)

Collector to Emitter Voltage	V_{CEO}	400	V
Emitter to Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	$I_C(\text{DC})$	500	mA
Peak Collector Current	$I_C(\text{pulse})^*$	1000	mA
Continuous Base Current	$I_B(\text{DC})$	250	mA

Maximum Power Dissipations

Total Power Dissipation ($T_a=25^\circ\text{C}$)	P_T	1.0	W
Total Power Dissipation ($T_C=25^\circ\text{C}$)	P_T	20.8	W

Maximum Temperatures

Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$

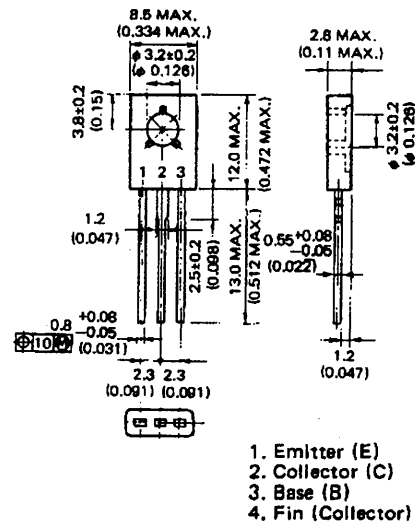
Thermal Resistance

Junction to Case	$R_{th(j-c)}$	6.0	$^\circ\text{C/W}$
------------------	---------------	-----	--------------------

* Pulsed $PW \leq 300 \mu\text{s}$, duty cycle $\leq 10\%$

PACKAGE DIMENSIONS

in millimeters (inches)



ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$)

Fig.7 Outlined Specifications of NTC2752

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector to Emitter Sustaining Voltage	$V_{CEO}(\text{SUS})$	400			V	$I_C=10 \text{ mA}$, $I_B=0$
Collector Cutoff Current	I_{CBO}			10	μA	$V_{CB}=400 \text{ V}$, $I_E=0$
Emitter Cutoff Current	I_{EBO}			10	μA	$V_{EB}=5.0 \text{ V}$, $I_C=0$
DC Current Gain	h_{FE1}	20		80		$V_{CE}=5 \text{ V}$, $I_C=50 \text{ mA}^*$
	h_{FE2}	10				$V_{CE}=5 \text{ V}$, $I_C=0.3 \text{ A}^*$
Collector Saturation Voltage	$V_{CE}(\text{sat})$			1.0	V	$I_C=300 \text{ mA}$, $I_B=60 \text{ mA}^*$
Base Saturation Voltage	$V_{BE}(\text{sat})$			1.2	V	
Turn On Time	t_{on}		0.5	1.0	μs	$I_C=0.3 \text{ A}$, $I_{VL}=I_{B2}=60 \text{ mA}$, $V_{CC}=150 \text{ V}$, $R_L=500 \Omega$, $PW=50 \mu\text{s}$, duty cycle $\leq 2\%$
Storage Time	t_{stg}		2.3	2.5	μs	
Fall Time	t_f		0.35	1.0	μs	

* Pulsed $PW \leq 350 \mu\text{s}$, duty cycle $\leq 2\%$

Caution: This transistor NTC2752 is underdevelopment device, and was production of this transistor will be started middle of 1981.

(3) Control circuit

With the conventional operating frequency of less than 100 kHz the control circuits may be built around standard ICs. The operating frequency of 200 kHz means, however, a shortened cycle of $5 \mu\text{s}$. So, standard ICs are not fully acceptable in such operating environment because their input/output delay runs almost 500 ns due to tpd characteristics of their comparators, and because the amplifiers' frequency characteristics are limited in high frequency range terms.

(The 200 kHz operation must be provided with $t_{pd} \leq 100$ ns and the amplifier frequency characteristics of more than 200 kHz for $A_V = 40$ dB.)

As a result, ZN1066E of Ferranti Electric Inc., is used for the trial model switching regulator.

(The frequency characteristics of the amplifier built in this IC is about 3 MHz for $A_V = 40$ dB.)

This IC contains two of these amplifiers, each of which is provided with the common mode input voltage range of 1 V to 2.8 V and designed to operate on a single power supply, not accepting 0 V. As a result, no excess current protection circuit is provided.

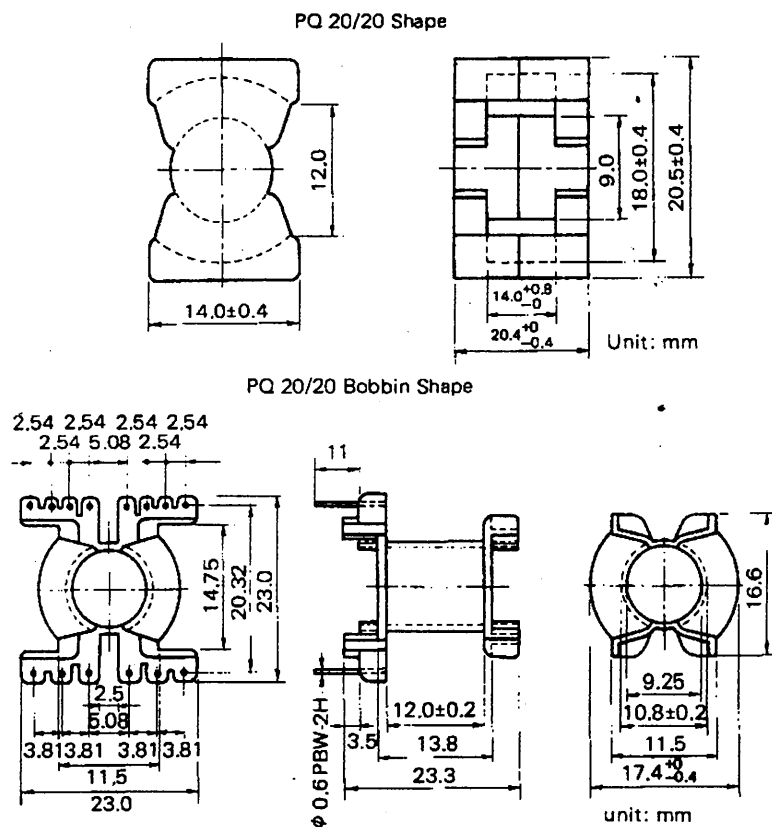
(4) Main transformer T_1 design

PQ core of TDK is adopted for main transformer T_1 . The following TDK document was referenced in drawing up T_1 design. Interested readers are advised to consult it.

Document title: PQ CORES FOR SWITCHING POWER SUPPLIES No. 79L-2

Core used: PQ 20/20 H7C1

The core and core bobbin shapes and core constant of PQ 20/20 H7C1 are shown in Fig. 8.



Parameter			
Core Constant	C_1	mm^{-1}	0.738
Effective Magnetic Path Length	ℓ_e	mm	45.4
Effective Cross Sectional Area	A_e	mm^2	62
Effective Volume	V_e	mm^3	2790
Central Leg Cross Sectional Area	A_{cp}	mm^2	61
Minimum Area of A_{cp}	$A_{cp}(\text{min})$	mm^2	58.1
Actual Window Area	A_{cw}	mm^2	65.8
Weight	g		15

Name	AL-value (nH/N ²)
H7C1PQ20/20 Z-12	≥ 4260
(50 kHz, 3T 100 °C)	

Fig.8 PQ20/20 Core, Core Bobbin Shapes and Core Constant

– Decision on Turns of Coil Winding –

Forward constant (K_{FC}) = 0.3 is assumed for 200 kHz operation. The minimum value ($V_{in} \text{ (min)}$) of the smoothing input voltage is found as follows.

Taking $V_{in} = 85 \text{ V (min)}$ and input = 10 A and consulting the O.H. Shade chart or calculating from the amount of electric charge from the smoothing capacitor due to inverter action,

$$V_{in} \text{ (min)} = 95 \text{ V}$$

Assuming core temperature increase T_{up} at 35°C , permissible power loss P_m is,

$$P_m = 1 \text{ W}$$

From the relationships $P_m = P_{LF} + P_{CU}$ and $P_{LF} = P_{CF}$ (minimal loss condition),

$$P_{LF} = P_{CU} = 0.5 \text{ W}$$

therefore total loss P_L is found as follows by $P_L = P_{LF}/K_{FC}$ which expresses the relationship between iron loss P_{LF} and K_{FC} in the forward converter circuit,

$$P_L = 1.67 \text{ W}$$

The relationship between flux density at operation and P_L is expressed as follows:

$$B_m^{2.4} = \frac{P_L}{(K_h + K_e \cdot f) \cdot V_e}$$

therefore

$$B_m = \left\{ \frac{1.67}{(4.9 \cdot 10^{-17} + 1.7 \cdot 10^{-22} \cdot 200 \cdot 10^3) \cdot 200 \cdot 10^3 \cdot 2310} \right\}^{\frac{1}{2.4}} \cdot 10^{-4}$$

$$= 0.1523 \text{ [T]}$$

As a result, from $\Delta B = 0.12 \text{ T (} 25^\circ\text{C)}$ and $A_{CP} = 61 \text{ mm}^2$ N_p , the number of primary winding turns, is expressed as follows.

$$N_p = \frac{V_{in} \text{ (min)} \cdot \tau_{O \max}}{\Delta B \cdot A_{CP}}$$

Assuming $\tau_{O \max} = 0.45 \text{ T}$ and $T = 5 \mu\text{s}$

$$N_p = \frac{95 \times 2.25 \times 10^{-6}}{0.12 \times 61 \times 10^{-6}} = 29.2 \approx 30. \text{ [Turns]}$$

– Decision on Secondary Winding –

$$N_s = \frac{N_p}{V_{in} \text{ (min)}} \cdot V_S \text{ and } V_S = \frac{V_O + V_F + V_\ell}{D_{\max}}$$

where V_ℓ = line drop voltage.

$$N_s = \frac{N_p (V_O + V_F + V_\ell)}{V_{in} \text{ (min)} \cdot D_{\max}}$$

where $V_F = 0.6 \text{ V}$, $V_O = 5 \text{ V}$, $V_\ell = 0.2 \text{ V}$ and $D_{\max} = 45\%$.

Therefore

$$N_s = \frac{30 \times 5.8}{95 \times 0.45} = 4.07 \text{ [Turns]}$$

– Winding –

Avoiding the formation of any air gap toward the bobbin edges is especially important to minimize leakage inductance. The sandwich method of winding the primary and secondary coils is also preferred for the purpose. The winding configuration shown in Fig. 9 is adopted, reflecting the outcome of a series of trials and errors.

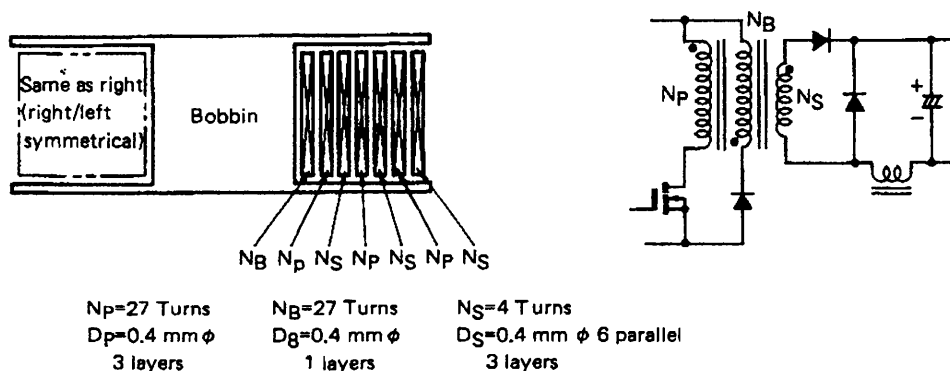


Fig. 9

Note: Against the design target of $N_p = 30$ [] $N_p = 27$ [] was the actual limit attainable with the 0.4 mm ϕ wire. Therefore $N_p = 27$ [] is used with the trial model switching regulator.
As a result, the constants above assume the following values.

$$\text{From } \Phi = \frac{V_{in(\min)} \cdot t_{on\max}}{N_p} = 7.92 \text{ [wb]}$$

$$\Delta B = 0.13 \text{ T, } B_m = 0.16 \text{ T, } P_L = 2.27 \text{ W and } P_{LF} = 0.681 \text{ W}$$

4. RESULTS

The switching regulator designed and manufactured as described in the following pages were tested and the results are shown in Table 5 and Fig. 10.

Table 5 Trial Model Switching Regulator Performance
Evaluation Results

Table 5.

Item	Conditions	Measured value
Line Regulation (%) $\Delta V_{out} (\Delta V_{out}/V_{out})$	$V_{in}=85\sim 115 \text{ V}$ $V_{out}=5 \text{ V, } I_{out}=10 \text{ A}$	16 mV(0.32 %)
Load Regulation (%) $\Delta V_{out} (\Delta V_{out}/V_{out})$	$I_{out}=0\sim 10 \text{ A}$ (0 to rated load) $V_{in}=100 \text{ V, } V_{out}=5 \text{ V}$	30 mV(0.60 %)
Output ripple voltage V_{ripple}	$V_{in}=100 \text{ V}$ $V_{out}=5 \text{ V, } I_{out}=10 \text{ A}$ (excluding output noise, p-p value)	50 mVp-p
Efficiency η	$V_{in}=100 \text{ V}$ $V_{out}=5 \text{ V, } I_{out}=10 \text{ A}$	78.4%
External shape	Without casing	34(W) X 170(D) X 110(H) (unit: mm)

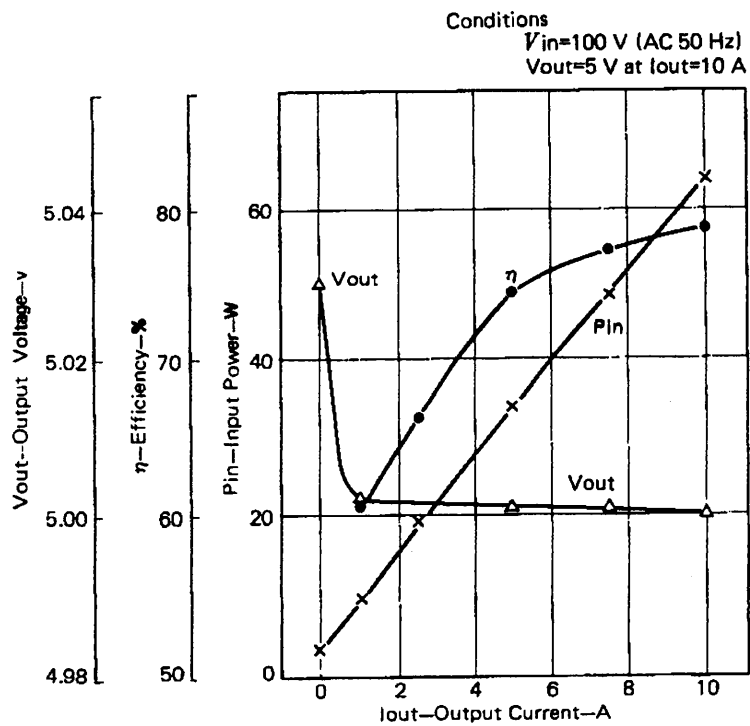


Fig.10a Input/Output Characteristics and Efficiency vs. Output Current Conditions

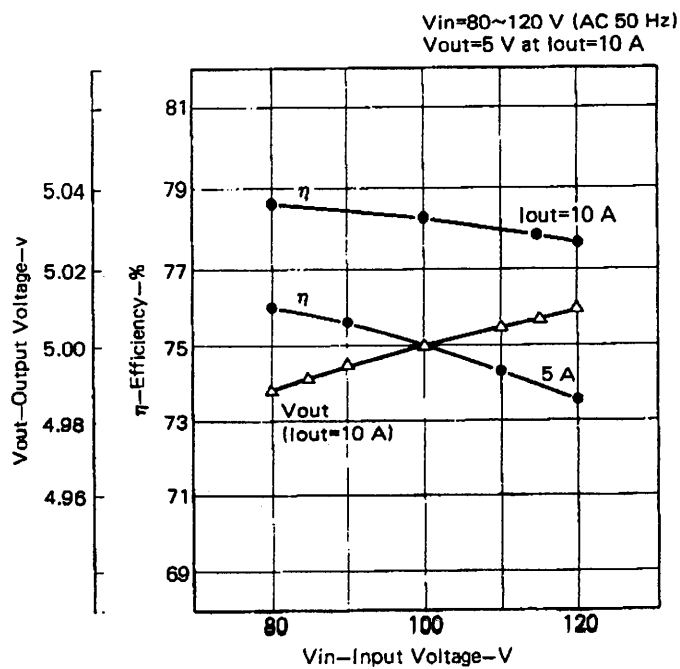


Fig.10b Output Voltage and Efficiency vs. Input Voltage



Fig.11 Operating Waveforms of Trial Mode 1 Switching Regulator

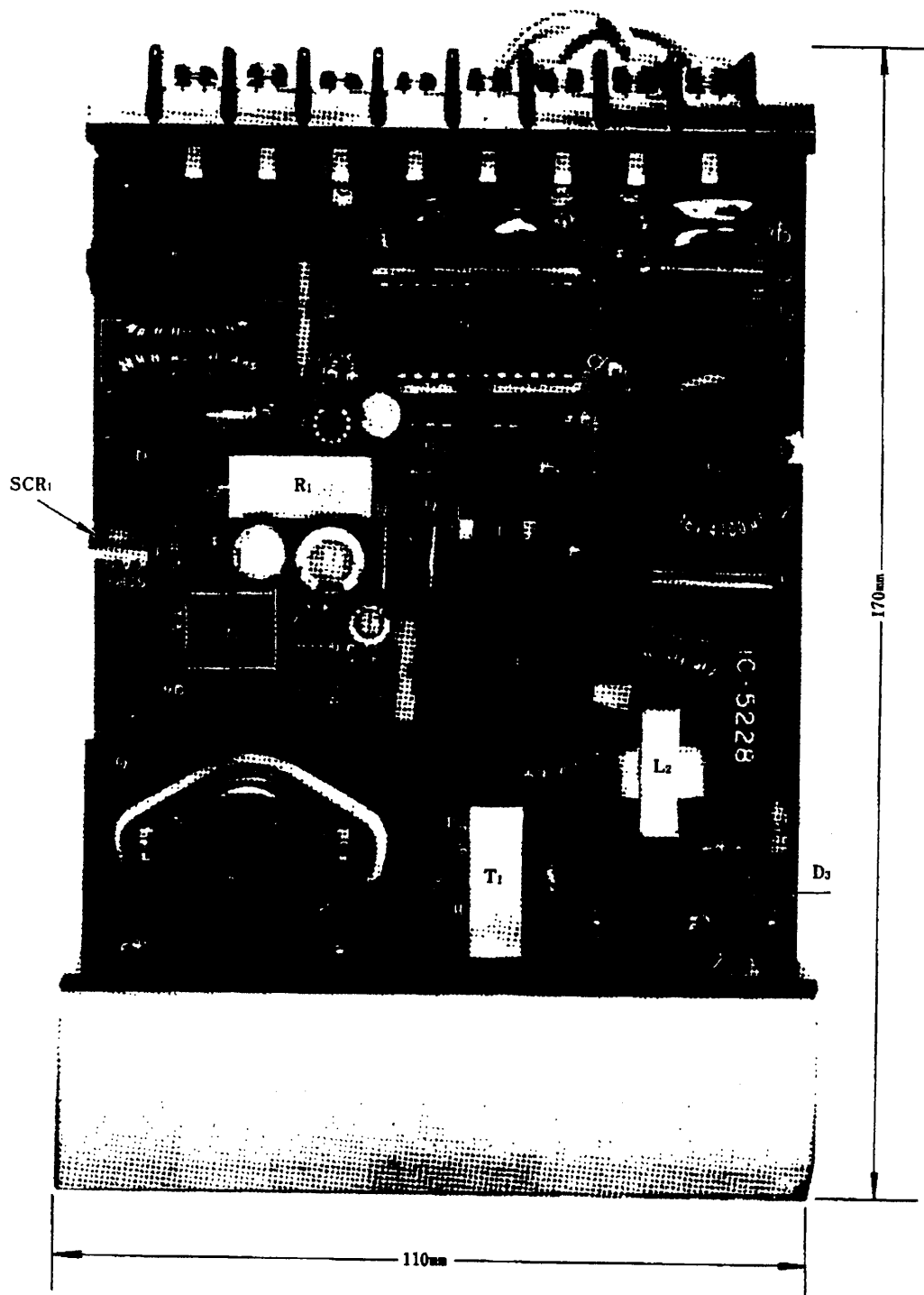


Fig. 12 Trial Model Switching Regulator External Appearance

5. SUMMARY

(1) Combined choke coil and its effect

In order to realize a faster response time making the most of the elevated operating frequency this switching regulator uses a pair of choke coils combined in such a way that, while one of them is saturated at prescribed amperage, the other of smaller L value remains unsaturated.

Fig. 14 shows an example of the advantage offered by such choke coil configuration at light load operation. Under this operating condition choke coil L_2 is not saturated. This causes I_D of inverter transistor Q_1 to incline less steeply, which in turn results in a reduced ripple current. The rewarding features of the combined choke coil are listed in Table 6.

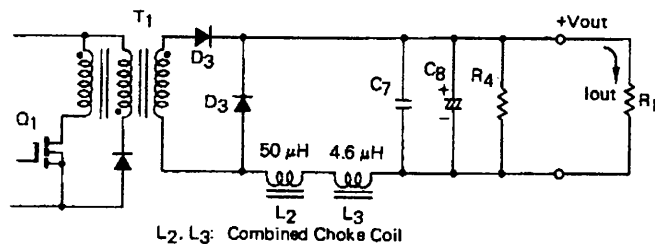


Fig.13a Secondary Side Rectifying Smoothing Circuit

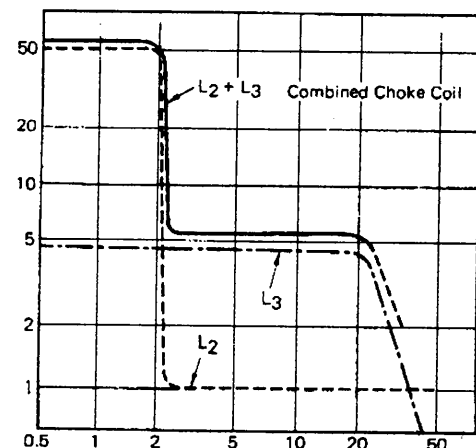


Fig.13b Combined Choke Coil Inductance Curves

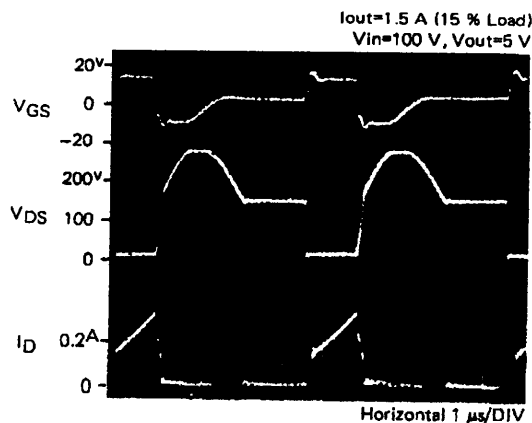


Fig.14 200 kHz Switching Regulator Operating Waveforms Under Light Load

Table 6. Rewarding Features of Combined Choke Coil

ITEM	CONTENTS
Reduced transient response time	As L_2 is saturated in the middle of operation, a faster output voltage transient response time is realized at load fluctuation than the case where a choke coil of same L value ($50 \mu\text{H}$) remains unsaturated.
Improved load regulation	Critical point moves farther toward the lighter end of load than the case where the saturating L_2 choke coil is absent. This improves load regulation almost to the same level as attained using a choke coil which has same L value as L_2 but does not saturate.
Improved stability	As critical point moves farther toward the lighter end of load than the case where L_2 is absent, the output ripple voltage does not rise in the load sweep test. This results in improved stability.
Reduced output ripple voltage under light load	The output ripple voltage is less pronounced than the case where L_2 is absent.
Improved efficiency under light load	L_2 works to reduce the ripple current of inverter transistor Q_1 under light load. This results in improved efficiency.

TABLE 6. REWARDING FEATURES OF COMBINED CHOKE COIL

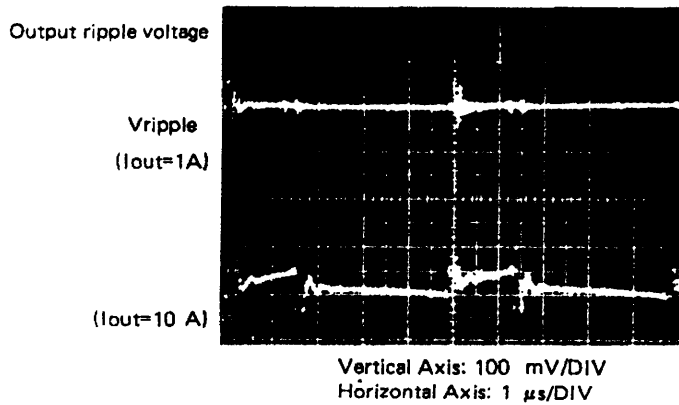


Fig. 15 Shows the Ripple Voltage Differences, Depending on the Amount of Output Current

– Transient Response Characteristics –

The transient response characteristics of output voltage when switching from light load to heavy load are discussed in the following pages.

Output Response

Suppose the switching regulator is put in operation as shown in Fig. 16 and load R_L is turned from OFF to ON by switching. Consider next how each part will behave.

As seen in Fig. 16-b, choke coil current I_L rises gradually after the switch is turned on. I_{D1} for $t = t_1$ is expressed as follows.

$$I_{D1} = \frac{V_S - V_{out} - V_F}{L} \cdot \tau_1 \quad \dots \dots \dots (1)$$

where V_S is the transformer secondary output voltage.

I_{D2} for $t = t_1 (= \tau_1 + \tau_2)$ is:

$$I_{D2} = I_1 = I_{D1} - \frac{V_{out} - V_F}{L} \cdot \tau_2 \quad \dots \dots \dots (2)$$

where V_F is the diode forward voltage.

Expressions (1) and (2) lead to:

$$I_1 = \frac{1}{L} \{ \tau_1 (V_S - V_{out} - V_F) - \tau_2 (V_{out} - V_F) \}$$

Assuming $\tau_1 = \tau_2 = \frac{T}{2}$,

$$I_1 = \frac{T}{2L} (V_S - 2V_{out}).$$

Therefore the value of I_L of choke coil in n -th cycle is:

$$I_{L(n)} = I_n = \frac{nT}{2L} (V_S - 2V_{out}).$$

Conversely, taking $nT = t_s$ for the above expression,

$$t_s = \frac{2L \cdot I_n}{V_S - 2V_{out}} \quad \dots \dots \dots (3)$$

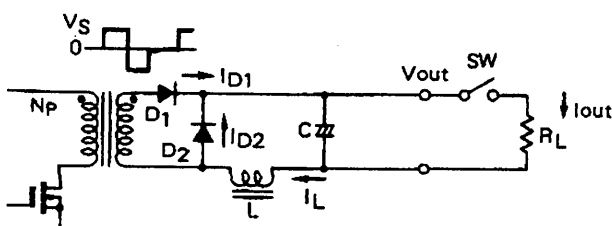


Fig.16a

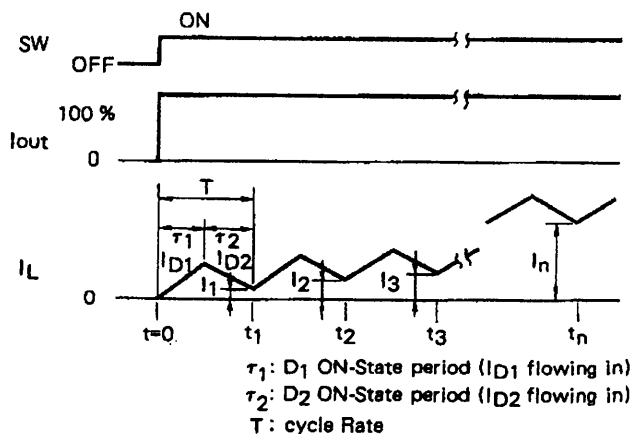


Fig.16b Step Response Waveform

The output voltage transient response to I_n in the circuit shown in the figure above is found next as shown in Fig. 17.

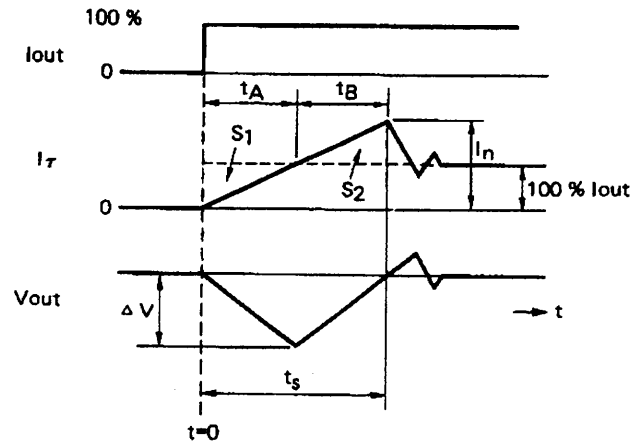


Fig.17 Output Voltage Transient Response Diagram

I_n rises linearly for $t = 0$ but an electric charge corresponding to area S_1 must be added in order to supply a certain amount of current (I_{out}) to the load. The electric charge corresponding to S_1 is to be obtained in the form of a discharge from capacitor C. This means, however, that the voltage across capacitor C suffers voltage drop ΔV corresponding to the discharge.

S_1 , the amount of electric charge to be added to make up for linear but gradual increase of I_n , is expressed:

$$S_1 = \frac{1}{2} I_{out} \cdot t_A \text{ while } S_1 = S_2, t_A = t_B = \frac{t_s}{2} \text{ and } I_n = 2I_{out}.$$

As voltage drop ΔV across capacitor C corresponds to the amount of discharge from the capacitor, which in turn equals S_1 ,

$Q_C = C \Delta V = S_1$ where Q_C is the discharge from capacitor C.

$$\text{Therefore } \Delta V = \frac{I_{out} \cdot t_A}{2C} = \frac{I_{out} \cdot t_s}{4C} \dots \dots \dots (4)$$

Putting Expression (3) in Expression (4),

$$\Delta V = - \frac{L \cdot I_{out}^2}{2C (V_S - 2V_{out})} \dots \dots \dots (5)$$

Rewriting Expression (3),

$$t_s = \frac{4L \cdot I_{out}}{V_S - 2V_{out}} \dots \dots \dots (6)$$

Therefore the relationship between transient response time constant t_s and choke coil inductance L and its counterpart between output voltage drop ΔV and choke coil inductance L are found as shown in Figs. 18-a and -b, using expressions (5) and (6).

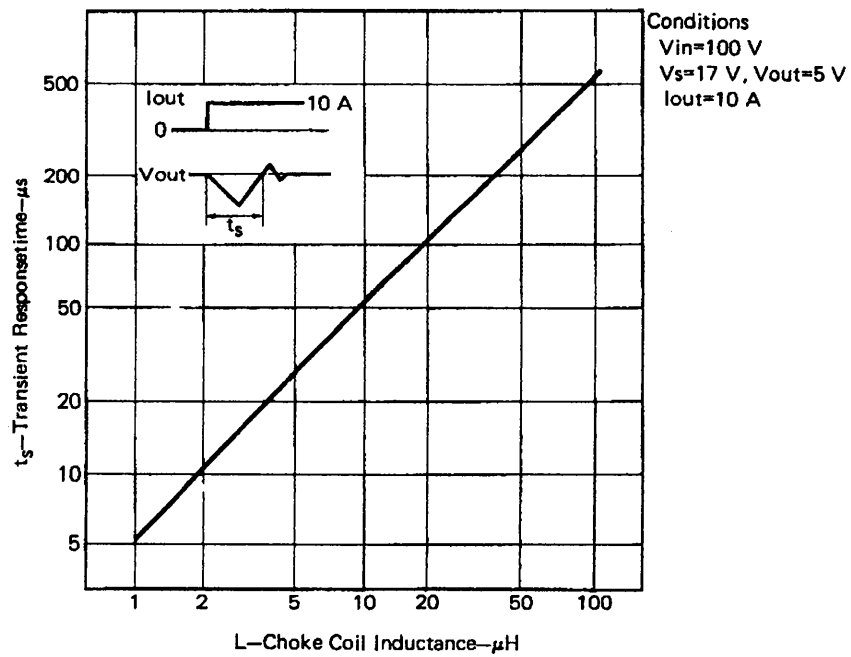


Fig. 18a L vs. t_s Characteristics

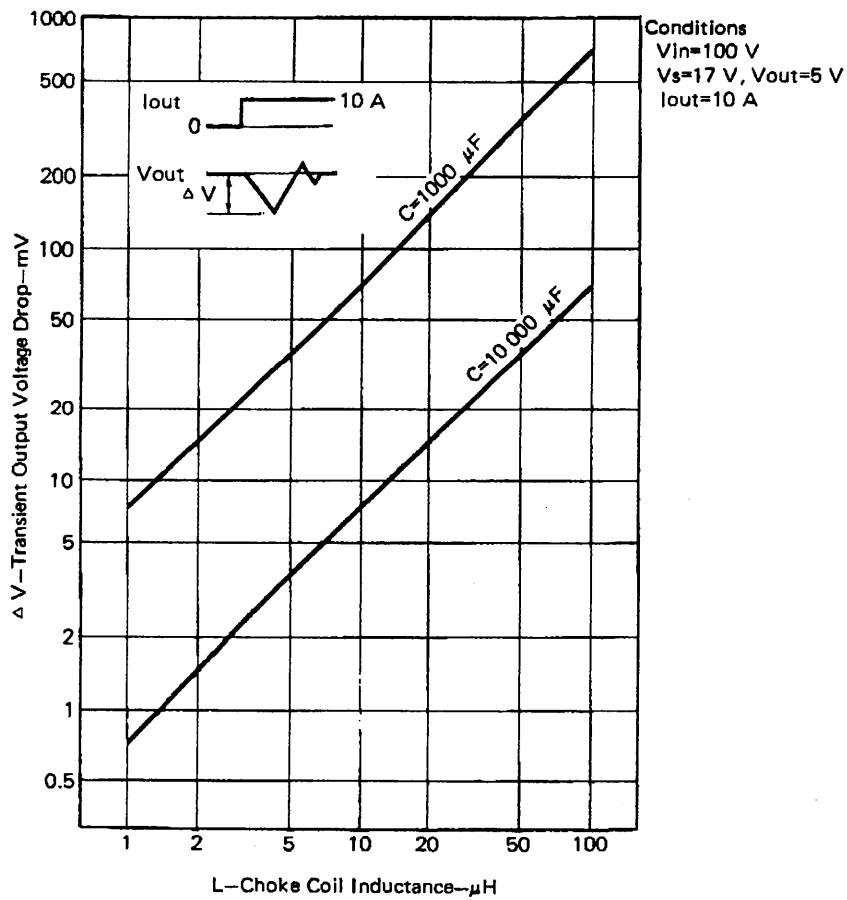


Fig. 18b L vs. ΔV Characteristics

Actual ΔV is subjected to the influence of line impedance up to the output terminal due to the presence of the smoothing capacitor as shown in the circuit of Fig. 19-a, and acts on the response waveform as shown in Fig. 19-b.

In order to abate this influence, it is necessary to reduce r_l as much as possible (less than 2–3 m Ω for 10 A application).

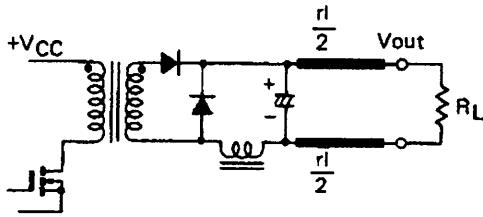


Fig.19a Circuit

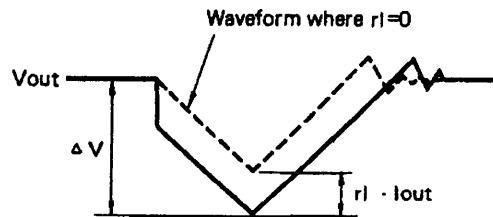


Fig.19b Response Waveform

Actual Example of Transient Response Characteristics

The output circuit configuration of this switching regulator is shown in Fig. 20. Response waveforms recorded for the load step from 0 to 100 % are shown in Fig. 21.

As seen in Fig. 21, this switching regulator realizes output response time $t_S \approx 50 \mu s$, which is much faster than that of previous switching regulators having the operating frequency of 20 kHz or so.

The output circuit of this switching regulator contains a combined choke coil which consists of choke coils L_2 and L_3 . Choke coil L_3 has a relatively large L value of 50 μH but is saturated at 2 A or thereabout. As a result, its influence on the transient response characteristics is extremely reduced.

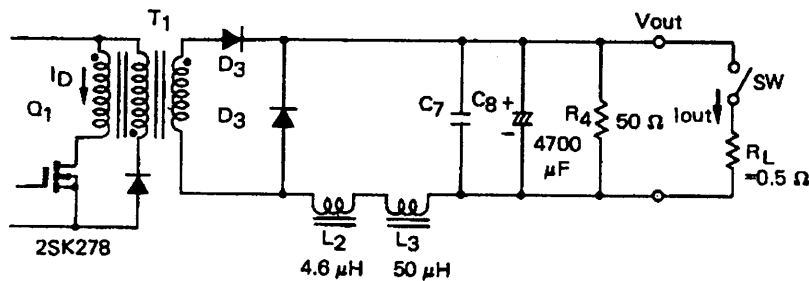


Fig.20 Forward Type Switching Regulator Circuit Configuration

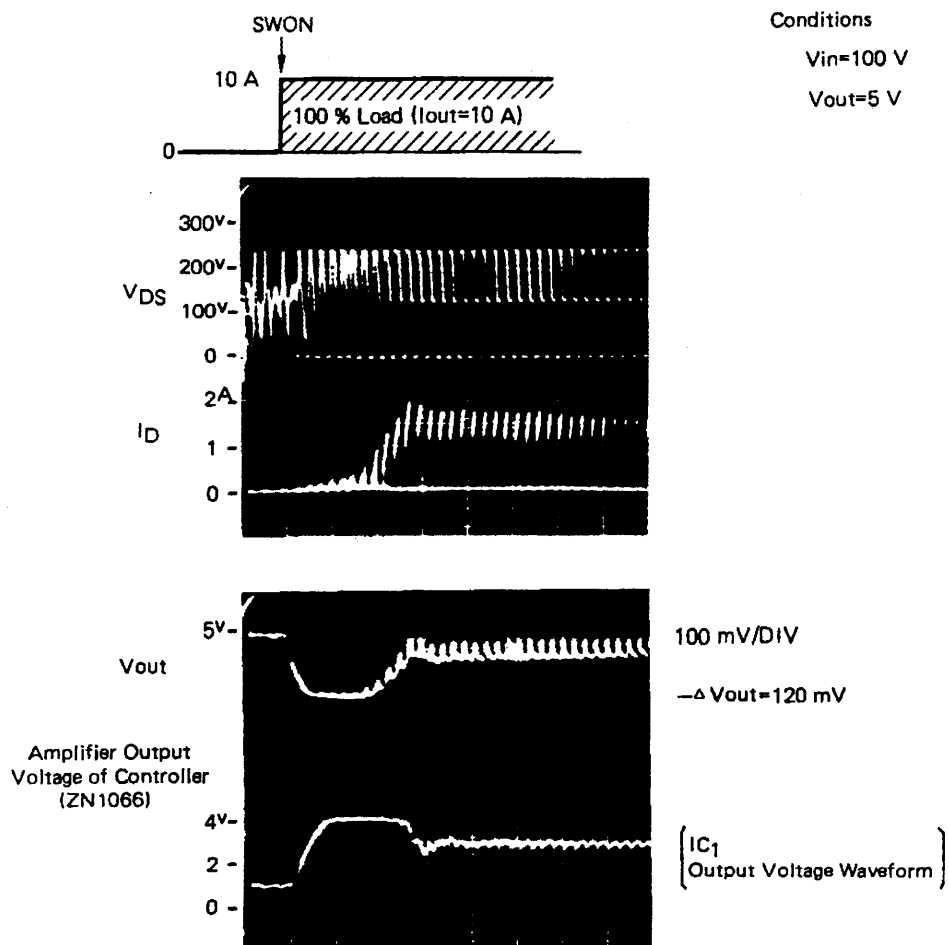


Fig.21 Output Voltage Transient Response Characteristics for 0 to 100 % Load Step Test

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