ISL5217 Cellular Applications

AN9911
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Introduction

The ISL5217 Quad Programmable Up-converter (QPUC) efficiently filters and upconverts baseband data to intermediate bandpass data utilizing from 1 to 4 programmable channels. Four channels can be independently used for narrowband applications such as IS-136, GSM, and EDGE, while 2, 3, or 4 channels can be combined in wideband application such as IS-95, CDMA-2000-1x, CDMA2000-3x MC and CDMA-2000-3x DS, TD-SCDMA, and UMTS. The design of the ISL5217 allows one device to implement four narrowband channels, two midwidth channels, or one wideband channel.

This application note describes the device configuration examples for several air interface standards with the information formatted for use with the ISL5217EVAL1 evaluation board and windows software.

For All Examples

Input Data Format

The ISL5217EVAL1 evaluation board was designed to utilize the QPUC serial data inputs as the primary input path. The board contains a 128Kx32 RAM to support driving the input data into the ISL5217 via the SDA-SDD serial data inputs. Data samples are input into the device serially in order, with sample n, followed by n+1....etc. The channel bit rate is the device symbol rate (f_S), which is the rate at which the I/Q samples are input into the device.

The I/Q sample pairs can be input in parallel through µP addressable registers or serially through 1 of 4 serial interfaces SDA-SDD, as shown in Figure 1. To provide increased flexibility for the user, many of the data input parameters are programmable, including word bit length, symbol rate, time slot values, and the data input flags. As only the device parameters required for the configurations in the examples are documented herein, please see the ISL5217 data sheet for complete device programming information.

The parallel mode allows the QPUC µP to write up to 16 bit I and Q samples directly into the FIFO holding registers through control words 0x1 and 0x0. The writing order is Q first, followed by I, with each channel having independent I and Q data control word locations. The µP can perform back-to-back write accesses, but must maintain four f_{CLK} periods between accesses to the same address. This limits the maximum µP write access rate for an I/ Q sample pair to CLK/4 or a maximum of 26MHz.

The serial channels provide for transfer of the input data at reduced rates, as each bit of serial data input requires a CLK for latching. This effectively limits 16 bit I and 16 bit Q samples to CLK/32 or 3.25MHz maximum. Lesser bit width data, like 4 bit I and 4 bit Q can be input at CLK/8, or 13MHz maximum.

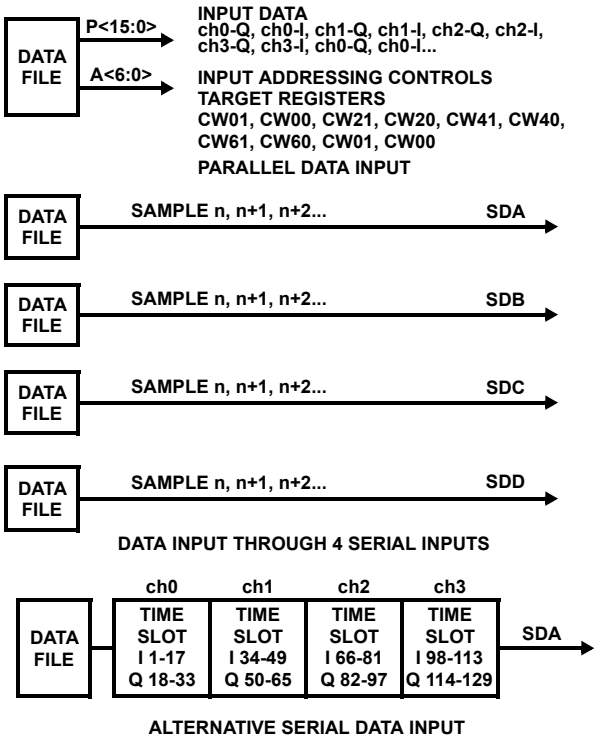


FIGURE 1. SINGLE CHANNEL INPUT DATA FORMAT

Shaping Filter Requirements

The required number of shaping filter coefficients is determined by the programmed Interpolation Phases (IP) and the Data Span (DS), where:

$$\#\ \text{Coefficients} = (DS)(IP) \quad \text{(EQ. 1)}$$

The interpolation phase determines the rate to compute a polyphase output by selecting the appropriate timing from the Sample Rate NCO to drive the shaping filter at 4x, 8x, or 16x the input sample rate. The Data Span selects the number of samples to convolve. Each convolution requires DS reference clocks for each phase of the filter. An output is calculated (IP) times for each input sample. To ensure sufficient processing time for each output, the clock must be:

$$CLK > (DS)(IP)(f_S) \quad \text{(EQ. 2)}$$

Conversely, the input sample rate requires:

$$f_S < (CLK)/[(IP)(DS)] \quad \text{(EQ. 3)}$$

Although the serial and parallel inputs can accommodate 3.25-13MHz and 26MHz data throughput, the shaping Finite Impulse Response (FIR) is programmable to x4, x8, or x16

interpolation phases with a selectable Data Span (DS) of 4-16. Selecting the minimum IP setting of 4 and DS setting of 4 yields a result from Equation 3 of a maximum data throughput limitation of 6.5MHz, per channel, for the device.

Shaping Filter Coefficients

The number of available FIR coefficients is 256 per channel per individual I and Q filter. These memory coefficients can be either 16-bit 2's complement or 24-bit floating point format, and can be segmented into two 128 location banks for switching between filters by setting a single bit in a control word.

Data Flow

Data flows through the device as shown in figure 2. Data enters the shaping FIR/FM modulator at f_S and exits at f_S* IP. The halfband filter interpolates by 2 to the f_S*IP*2 rate, or can be bypassed. Data enters the High Order Interpolation (HOI) filter and can be integer or non-integer interpolated, but always exits at the CLK rate. Please see the data sheet for the muxed at 2x clock output rates and additional output mode information.

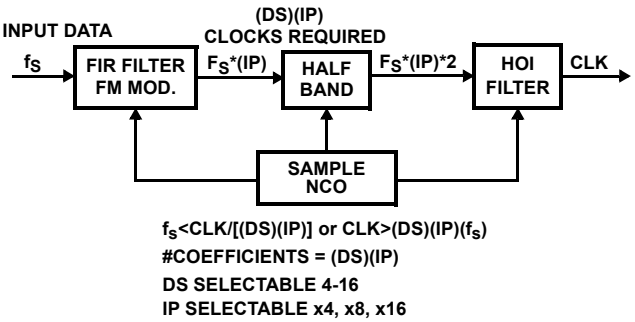


FIGURE 2. MULTIPLE CHANNEL INPUT DATA FORMAT

The shaping filter, halfband, and HOI filter combine to produce an overall interpolation through the device of CLK/f_S.

File Formats

The evaluation board windows application program requires several types of input files to configure and load data into the board. Scripts are used to configure the evaluation board and for programming sequential actions. Java scripts (*.js) and Visual Basic scripts (*.vbs), created with any text editor, are supported. Specific file formats are required for each type of file, with examples provided in the evaluation software.

*Configuration Files *.js or *.vbs*

Configuration files contain the evaluation board form contents in register command format. The header contains the set-up information required for the loader, followed by the reset commands and the software form registers output commands. Device commands are Puc.Poke, Puc.peek, setbits, clearbits, resetbits and modifybits. Evaluation board hardware commands which do not directly affect the device are Puc.Write and Puc.read. All ADDRESS, DATA, and MASK values are expressed in HEXADECIMAL. Additional insight on the command line window can be obtained by using the forms to change bit fields and observing the corresponding commands being echoed in the command line window. Please see the evaluation board users manual for detailed information.

*Coefficient Files *.coe or *.imp*

The coefficient files contain seven comment lines at the beginning, which are ignored by the loader, with each line thereafter containing one floating point coefficient per line. The magnitude of each coefficient must be less than one.

*Pattern Files *.pat or *.imp*

The pattern file contains seven comment lines at the beginning, which are ignored by the loader, with each line thereafter containing two floating point numbers with values that must be less than 1. The first number is for the I data, and the second is for the Q data.

*Dynamic Configuration Files *.cfg*

The dynamic configuration file contains seven comment lines at the beginning, which are ignored by the loader, with each line thereafter containing a device register address and value for the 15 device configuration registers. When the dynamic configuration is enabled, one of the eight sets of 15 registers is output during the TXENx low period.

Clock Rates

The CLK rates specified for the examples may vary from the oscillator installed in the evaluation board position U6. The evaluation boards are supplied with an 80MHz oscillator. Please ensure that you remove the U6 oscillator and utilize the J11 clock input SMA connector in order to support the specific examples shown herein. Please see the reference documents section of the AN9910 user's software users manual to obtain an evaluation board schematic and other applicable documents.

Example Configurations

GSM

The device is configured in pre-filtered FM mode for outputting four channels of GSM in continuous mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA input, and the symbol NCO is programmed to provide a sample rate of f_S = 270.833kHz. The shaping FIR is programmed to interpolate by x16 with a dataspan of 5. The filter frequency response is shown in Figure 3. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 4, 8,12, and 16MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 4, utilizing the on-board HI5828 dual DAC, and the vector analysis is shown in Figure 5. The stimulus file is 1022 samples of pseudo random gmsk data.

The digital data was collected utilizing a 32K FFT with the results shown in Figure 6. Enabling the halfband, the digital performance is improved as shown in Figure 7.

TABLE 1. GSM CONFIGURATION

Clock Rate CLK =	80MHz
Sample Frequency f_S =	270.833kHz
Configuration File:	GSM_only.js
Filter File:	gs5t16x.imp
Stimulus File:	gmskpnpc.imp
Dynamic Configuration File:	N/A

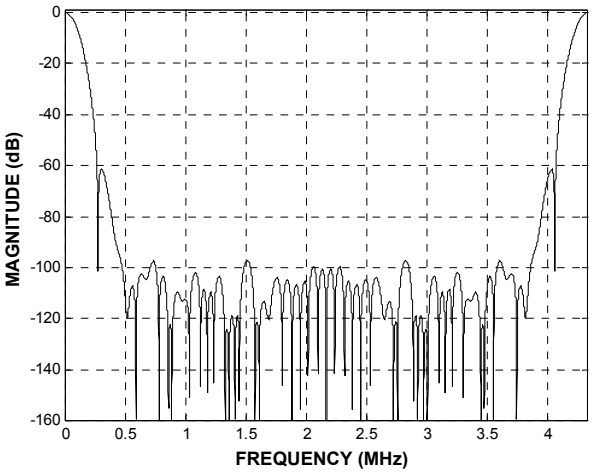


FIGURE 3. SHAPING FILTER FREQUENCY RESPONSE

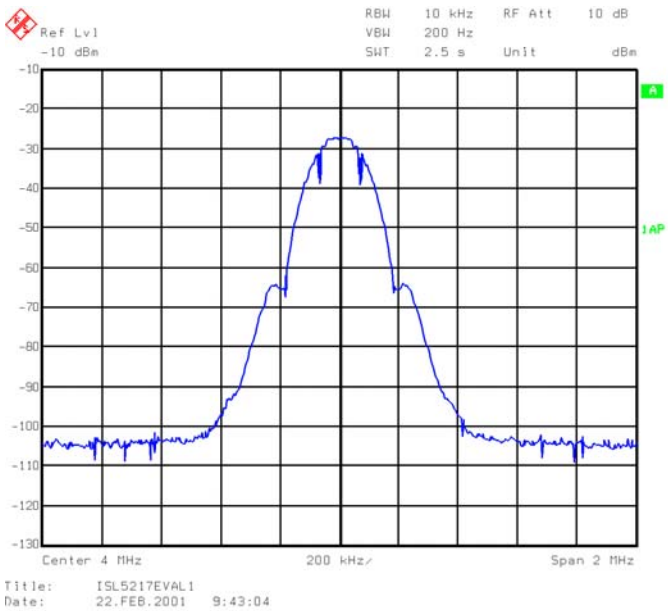


FIGURE 4. ANALOG SPECTRUM

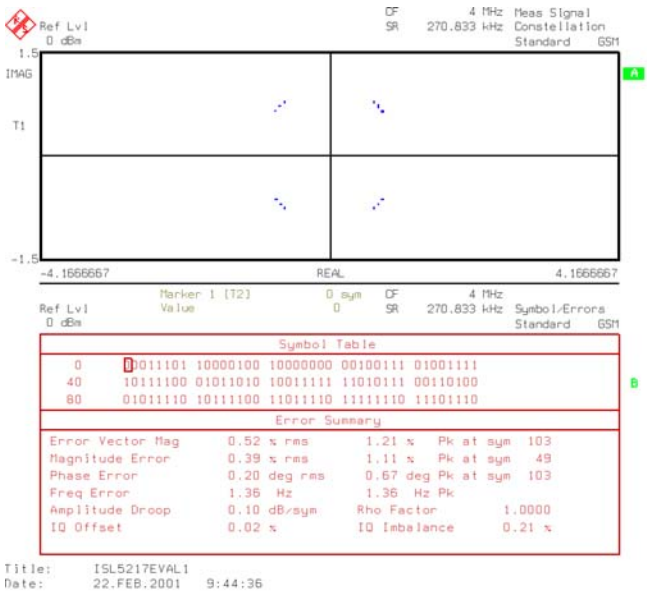


FIGURE 5. VECTOR ANALYZER OUTPUT

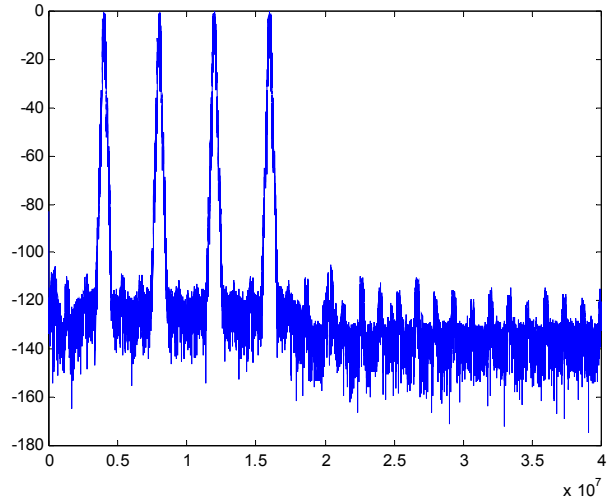


FIGURE 6. DIGITAL OUTPUT

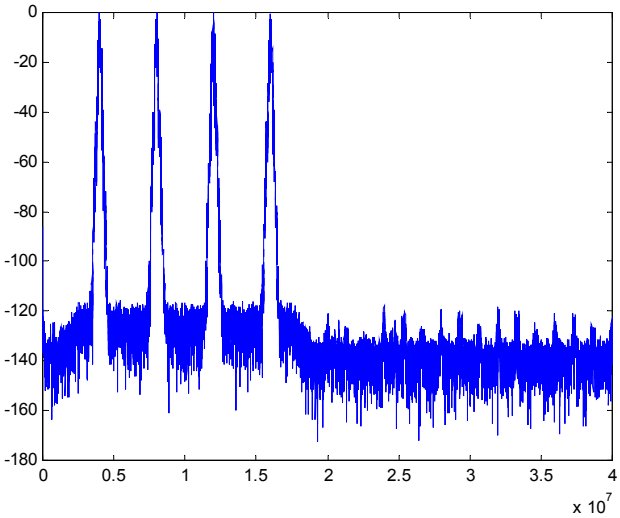


FIGURE 7. DIGITAL OUTPUT, HALFBAND ENABLED

GSM Burst Mode

The device is configured for outputting one channel of GSM in burst mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA input, and the fixed integer divider (FID) is enabled to provide an integer relationship of CLK/288 or f_S = 270.833kHz rate. The shaping FIR is programmed to interpolate by x16 with a dataspan of 6. The filter frequency response is shown in Figure 8. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequency is set to 4MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 9, utilizing the on-board HI5828 dual DAC, and the vector analysis is shown in Figure 10. The stimulus file is 148 samples of pseudo random data with a synchronization pattern included.

The dynamic configuration software mode is utilized with a programed value of TXEN on =148.5 bits or 42768 clocks on (148.5 * (1/270.8333e3) / (1/78e6)) and 8.25 bits or 2376 clocks off (8.25 * (1/270.8333e3) / (1/78e6)). These settings allow the device to transmit 148 bits in the required on normal burst period and to ramp up/down in the guard period. The gain profile is enabled in this example with 192 gain profile coefficients being utilized. The gain profile coefficients were derived from the EDGE transmit filter profile with trailing full scale bits added to extend the transmit on time.

TABLE 2. GSM Burst Configuration

Clock Rate CLK =	78MHz
Sample Frequency f_S =	270.833kHz
Configuration File:	GSM_Only.js
Filter File:	gs5t16xTest.imp
Stimulus File:	GSM_Only.imp
Dynamic Configuration File:	GSM_Only.imp

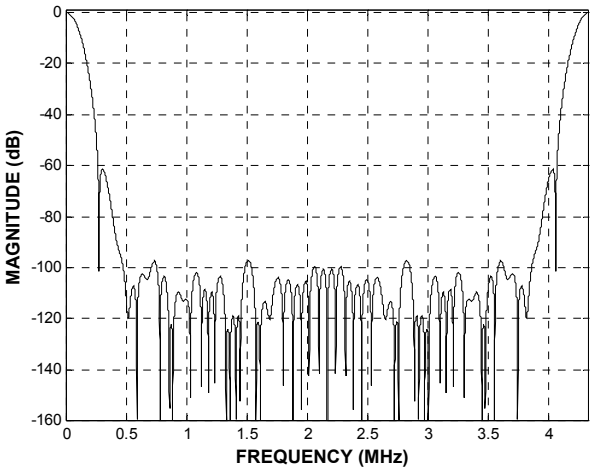


FIGURE 8. SHAPING FILTER FREQ. RESPONSE

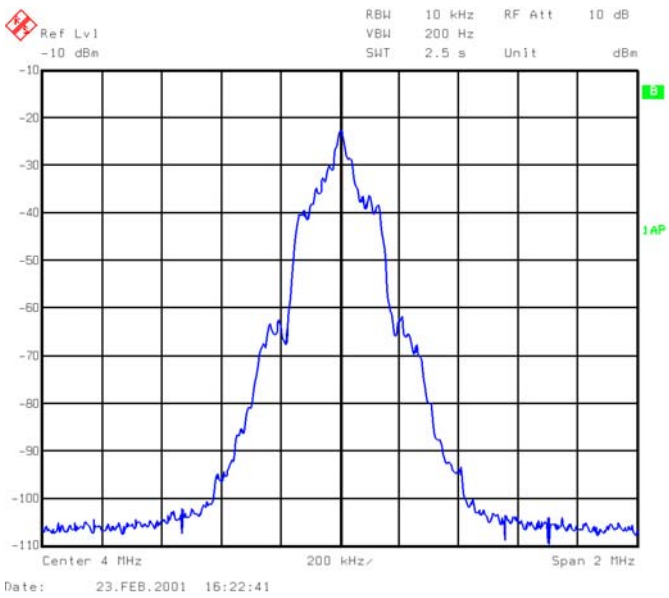


FIGURE 9. ANALOG SPECTRUM

The peak shown in the analog spectrum is due to the pattern loaded, the data does not present a pn spectral outline.

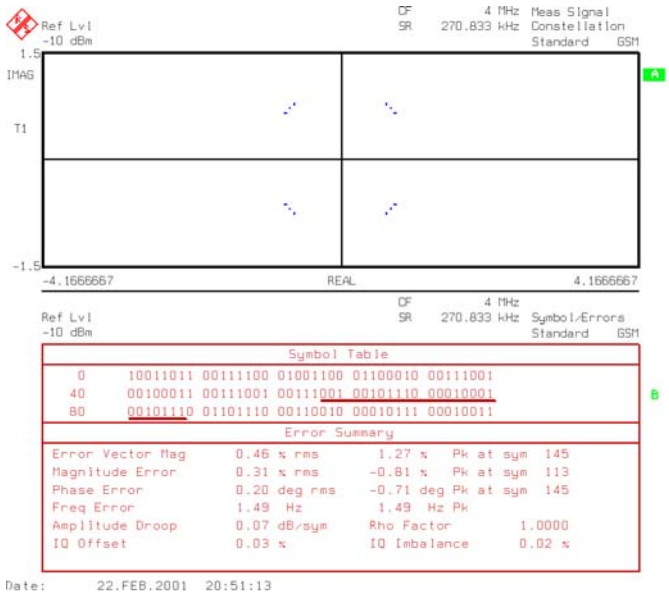


FIGURE 10. VECTOR ANALYZER OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 11. Enabling the halfband, the digital performance is improved as shown in Figure 12.

TXEN timing latency in the offset binary mode is shown in Figure 13.

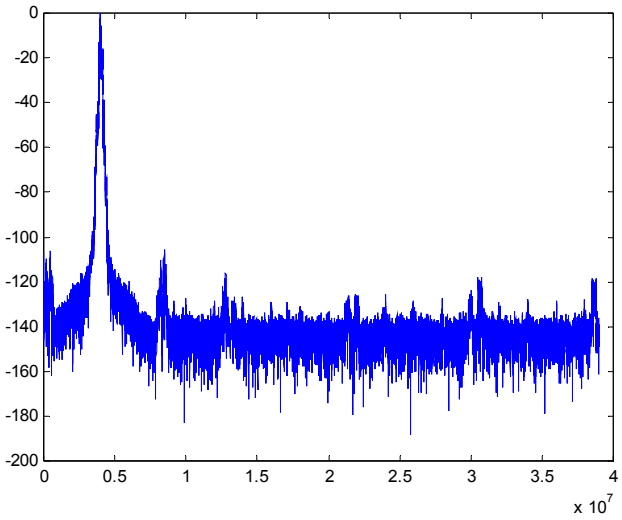


FIGURE 11. DIGITAL OUTPUT

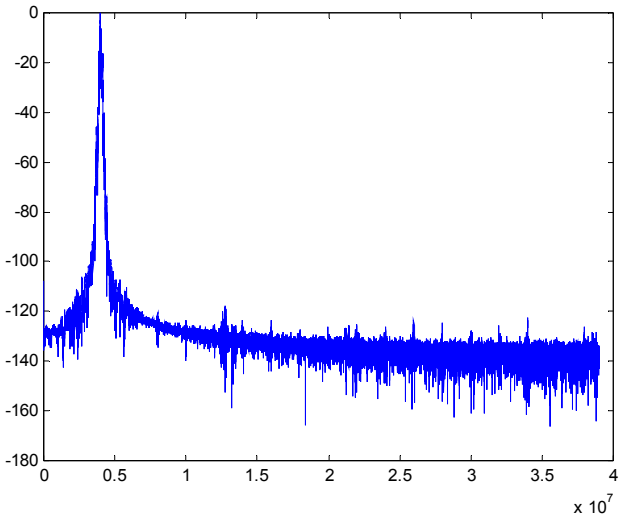


FIGURE 12. DIGITAL OUTPUT, HALFBAND ENABLED

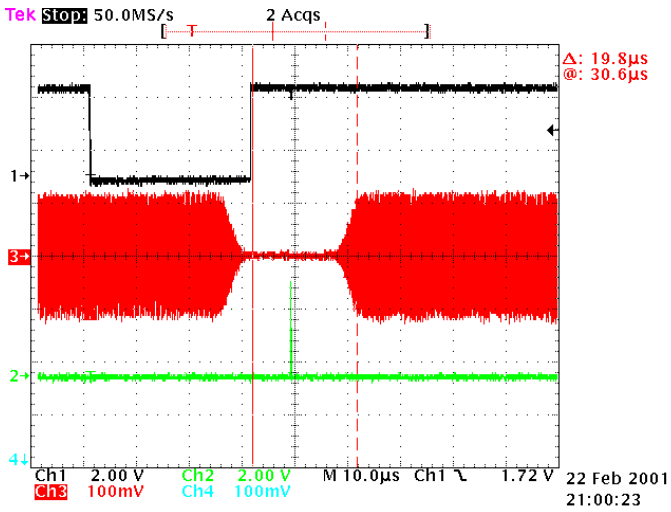


FIGURE 13. TXEN vs BURST TIMING (HALFBAND ON)

EDGE

The device is configured for QASK and outputting four channels of EDGE in continuous mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of f_S = 270.833kHz. The shaping FIR is programmed to interpolate by x16 with a dataspan of 5. The filter frequency response is shown in Figure 14. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 4, 8, 12, and 16MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 15, utilizing the on-board HI5828 dual DAC, and the vector analysis is shown in Figure 16. The stimulus file is 1022 samples of pseudo random 3/8pi 8psk data.

TABLE 3. EDGE CONFIGURATION

Clock Rate CLK =	80MHz
Sample Frequency f_S =	270.833kHz
Configuration File:	EDGE.js
Filter File:	edget16x.imp
Stimulus File:	edgem6db.imp
Dynamic Configuration File:	N/A

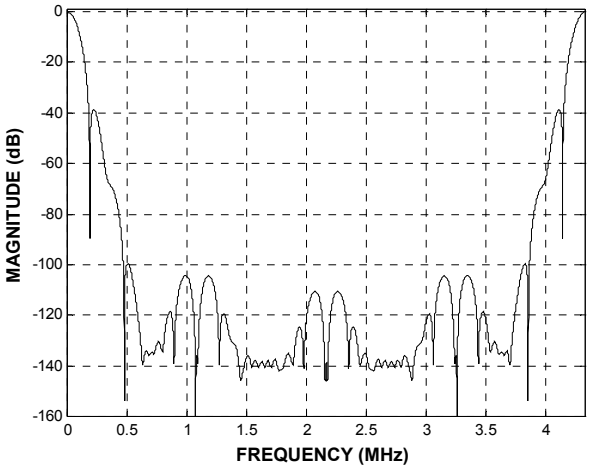


FIGURE 14. SHAPING FILTER FREQ. RESPONSE

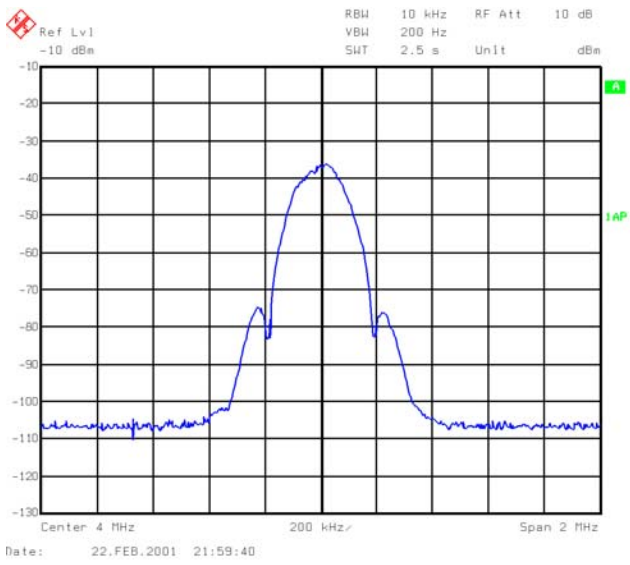


FIGURE 15. ANALOG SPECTRUM

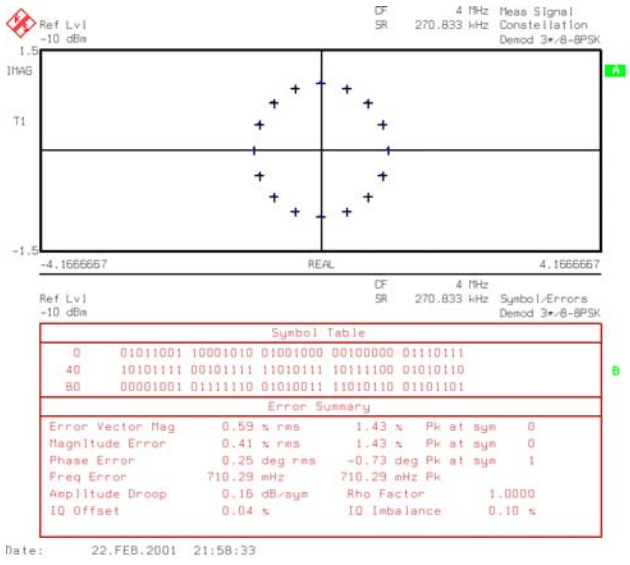


FIGURE 16. VECTOR ANALYZER OUTPUT

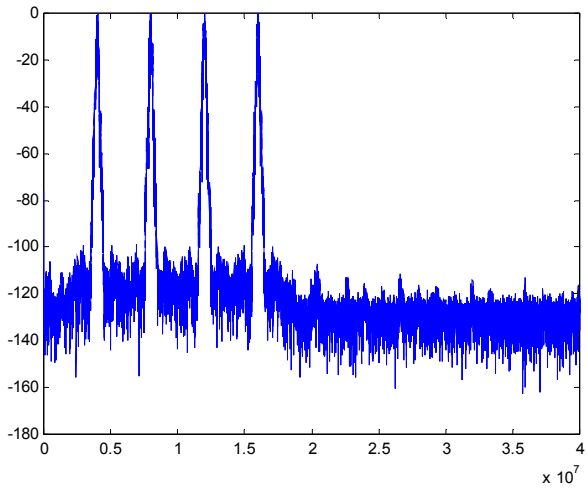


FIGURE 17. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 17. Enabling the halfband, the digital performance is improved as shown in Figure 18.

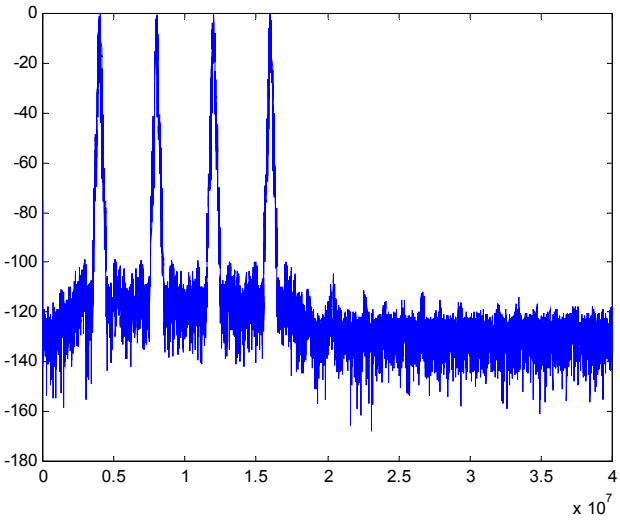


FIGURE 18. DIGITAL OUTPUT, HALFBAND ENABLED

EDGE Burst Mode

The device is configured for outputting one channel of EDGE in burst mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA input, and the fixed integer divider (FID) is enabled to provide an integer relationship of CLK/288 or f_S = 270.833kHz rate. The shaping FIR is programmed to interpolate by x16 with a dataspan of 6. The filter frequency response is shown in Figure 19. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequency is set to 4MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 20, utilizing the on-board HI5828 dual DAC, and the vector analysis is shown in Figure 21. The stimulus file is 148 samples of pseudo random QPSK data.

The dynamic configuration software mode is utilized with a programed value of TXEN on =148.5 bits (148.5 * (1/270.8333e3) / (1/78e6)) or 42768 clocks on and 8.25 bits (8.25 * (1/270.8333e3) / (1/78e6)) or 2376 clocks off. These settings allow the device to transmit 148 bits in the required on normal burst period and to ramp up/down in the guard period. The gain profile is not enabled, with the EDGE FIR coefficients providing the required pulse shaping.

TABLE 4. EDGE BURST CONFIGURATION

Clock Rate CLK =	78MHz
Sample Frequency f_S =	270.833kHz
Configuration File:	EDGE_Only.js
Filter File:	edget16xTest.imp
Stimulus File:	EDGE_Only.imp
Dynamic Configuration File:	EDGE_Only.imp

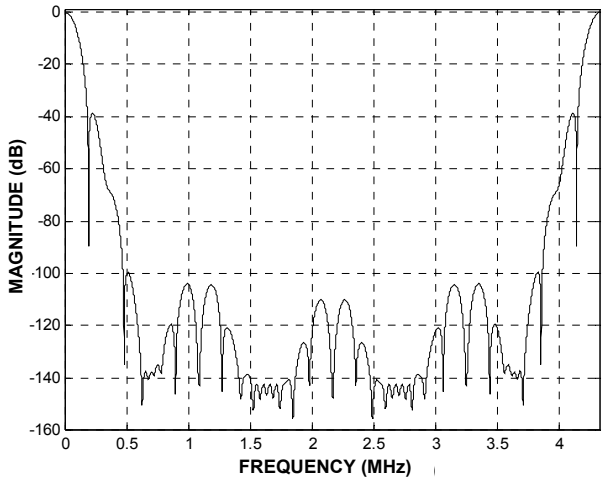


FIGURE 19. SHAPING FILTER FREQ. RESPONSE

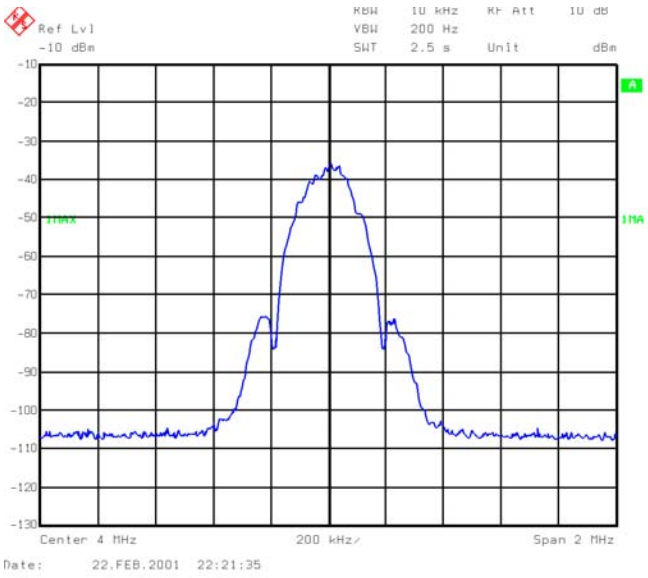


FIGURE 20. ANALOG SPECTRUM

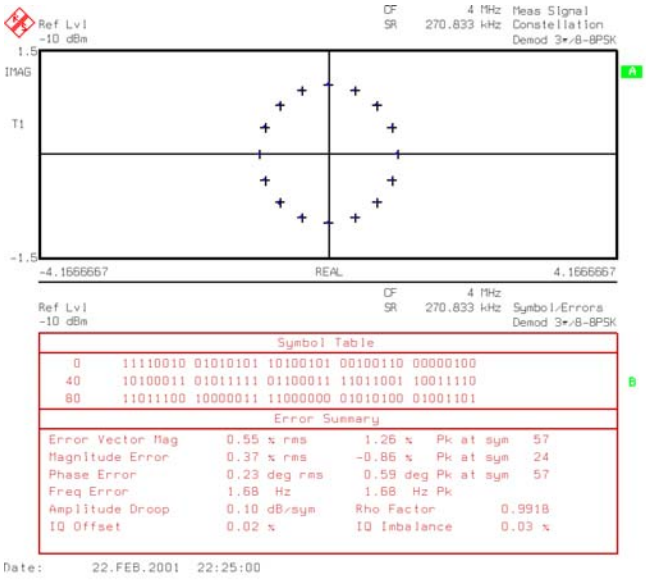


FIGURE 21. VECTOR ANALYZER OUTPUT

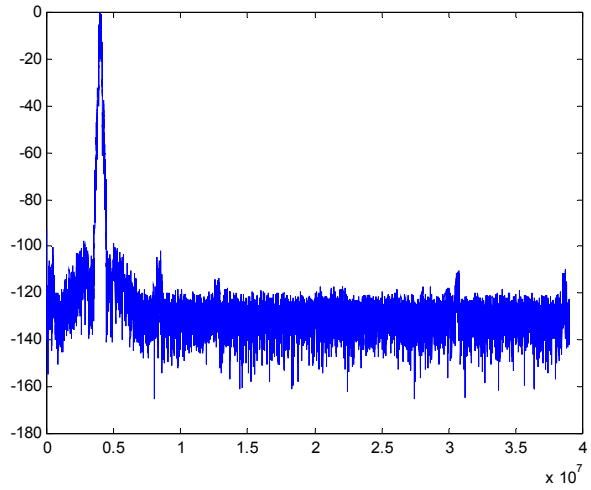


FIGURE 22. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 22. Enabling the halfband, the digital performance is improved as shown in Figure 23.

TXEN timing latency in the offset binary mode is shown in Figure 13, while 2's complement timing is approximately 13.2µS.

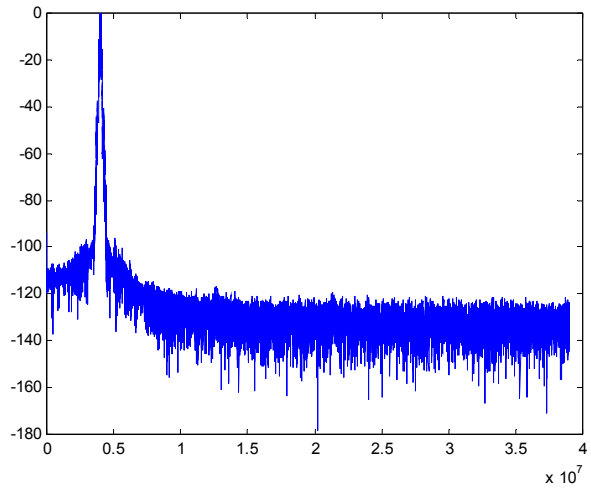


FIGURE 23. DIGITAL OUTPUT, HALFBAND ENABLED

GSM/EDGE Overlay

The device is configured for one normal burst of pre-filtered FM GSM followed by one normal burst of QASK EDGE with different filters. The 16-bit I and 16-bit Q data is input through the serial channel SDA input, and the fixed integer divider (FID) is enabled to provide an integer relationship of CLK/288 or f_S = 270.833kHz rate. The shaping FIR is programmed to interpolate by x16 with a dataspan of 6, with the GSM filter coefficients preloaded in memory bank one and the EDGE coefficients in bank two. The filters utilized are the same as for the GSM or EDGE burst mode. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequency is set to 4MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout

output on QOUT<19:0>. The analog performance of the device is shown in Figure 25, utilizing the on-board HI5828 dual DAC. Figures 26-34 show various timing depictions for the overlaid burst. The stimulus file is 148 samples of pseudo random GMSK data with a synchronization pattern included followed by 148 patterns of 3/8pi 8psk pn data.

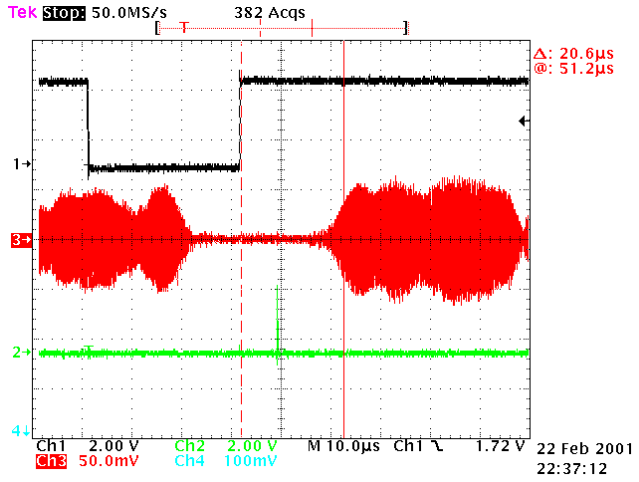


FIGURE 24. TXEN vs BURST TIMING (HALFBAND ON)

TABLE 5. GSM/EDGE OVERLAY CONFIGURATION

Clock Rate CLK =	78MHz
Sample Frequency f_S =	270.833kHz
Configuration File:	GSM_EDGE.js
Filter File:	gs5t16xTest.imp, and edget16xTest.imp
Stimulus File:	GSM_EDGE.imp
Dynamic Configuration File:	GSM_EDGE.cfg

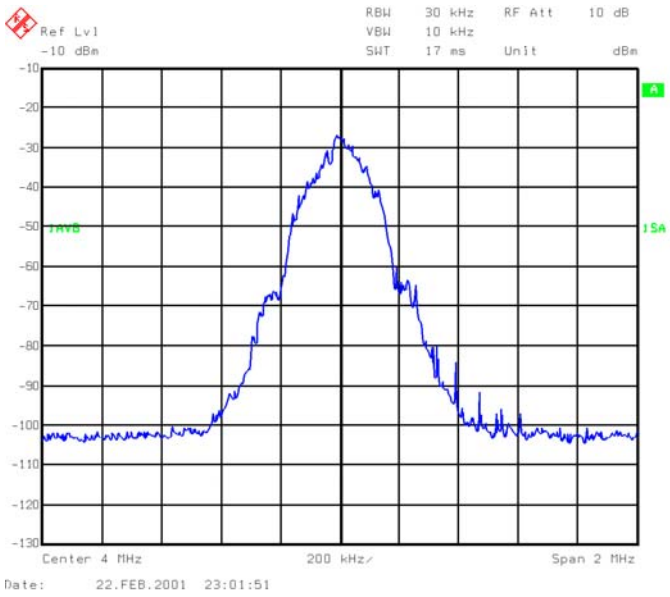


FIGURE 25. SPECTRUM GSM/EDGE

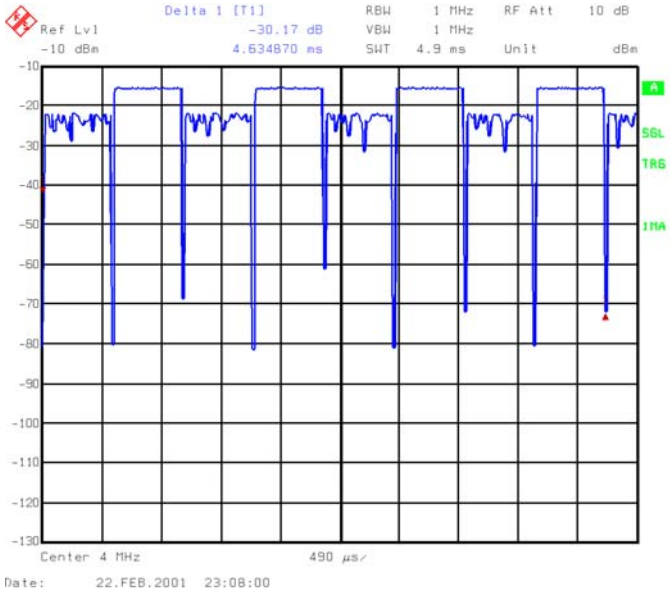


FIGURE 26. TDMA FRAME GSM/EDGE

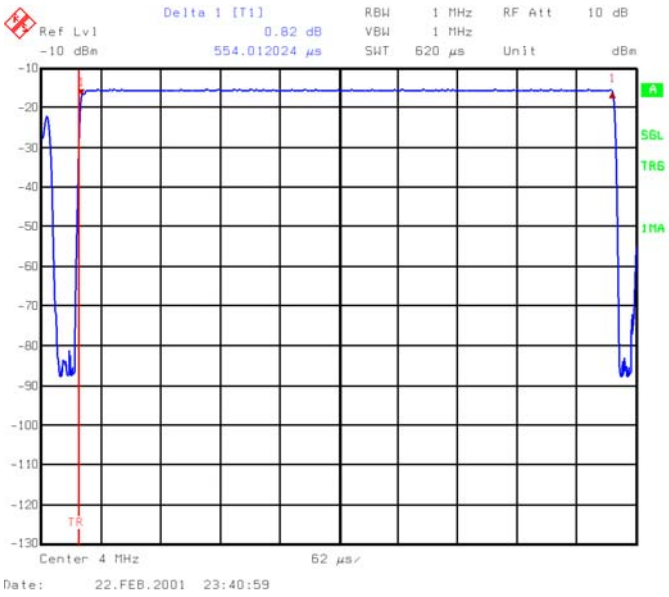


FIGURE 27. GSM FRAME TIMING

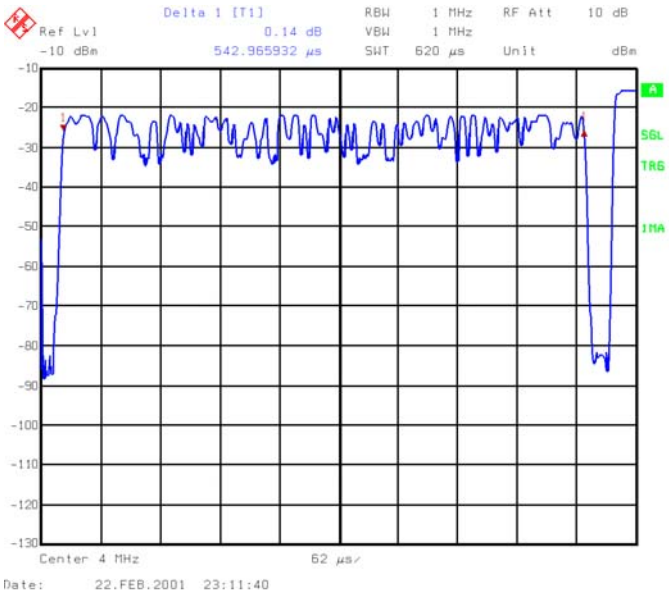


FIGURE 28. EDGE FRAME TIMING

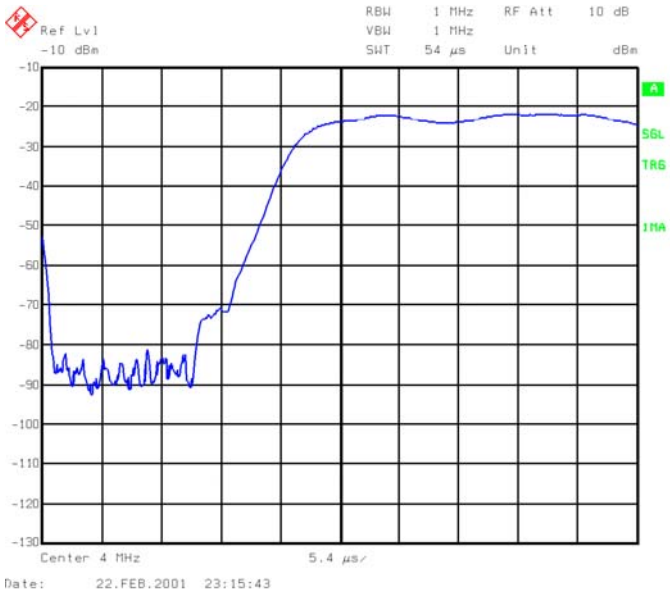


FIGURE 29. EDGE RAMP UP TIMING

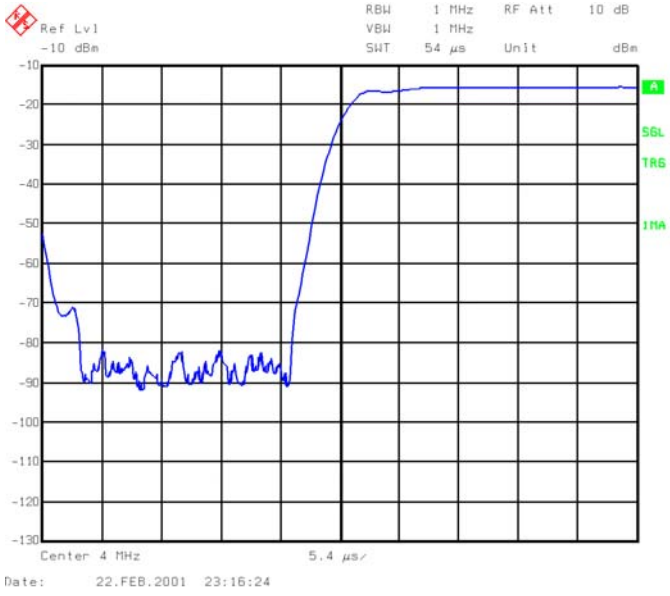


FIGURE 30. GSM RAMP UP TIMING

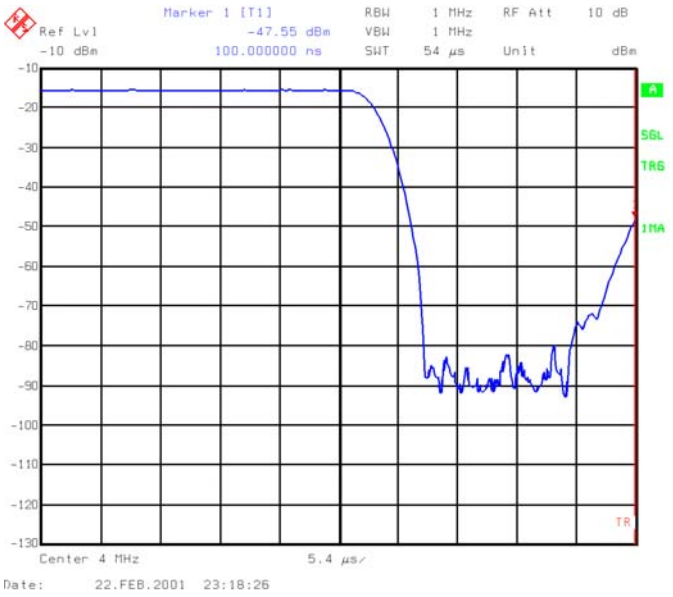


FIGURE 31. GSM QUENCH TIMING

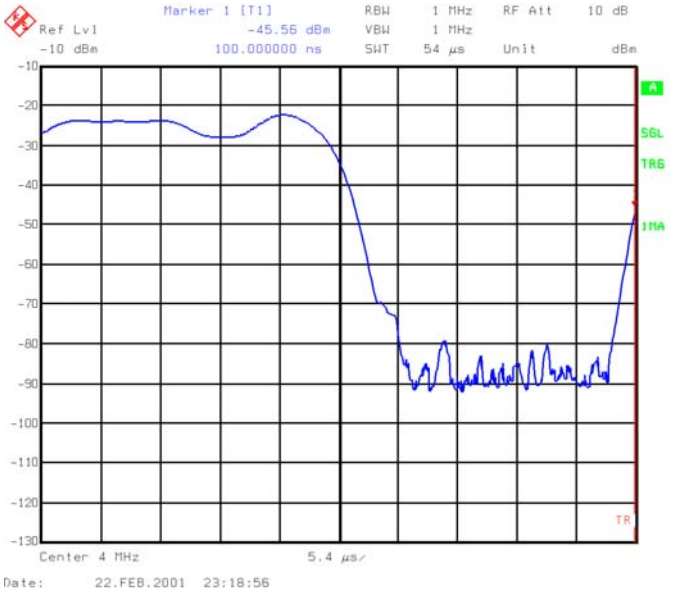


FIGURE 32. EDGE QUENCH TIMING

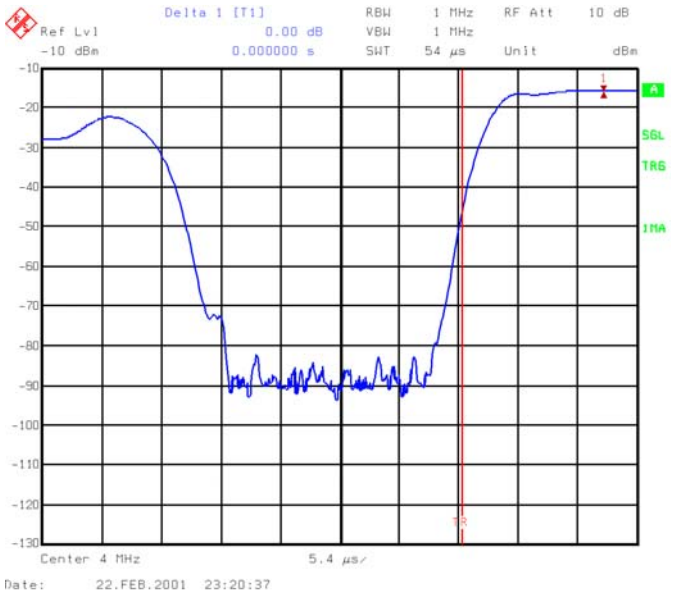


FIGURE 33. EDGE TO GSM GUARD TIMING

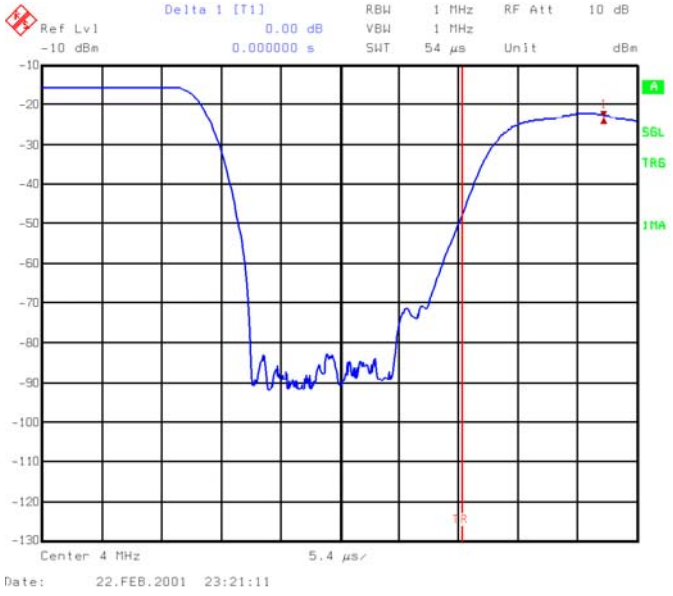


FIGURE 34. GSM TO EDGE GUARD TIMING

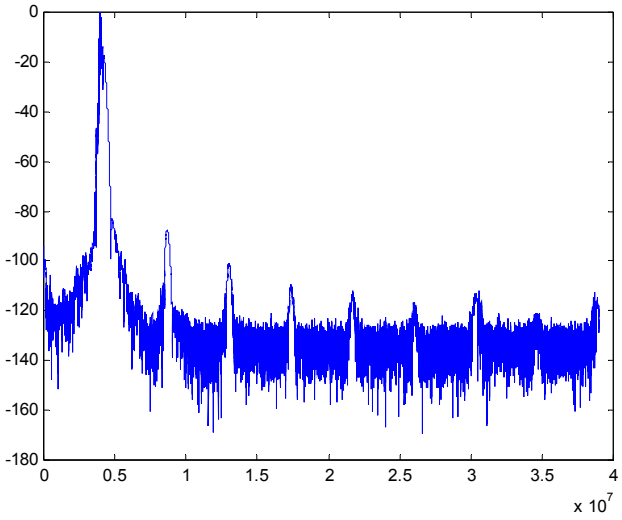


FIGURE 35. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 35. Enabling the halfband, the digital performance is improved as shown in Figure 36.

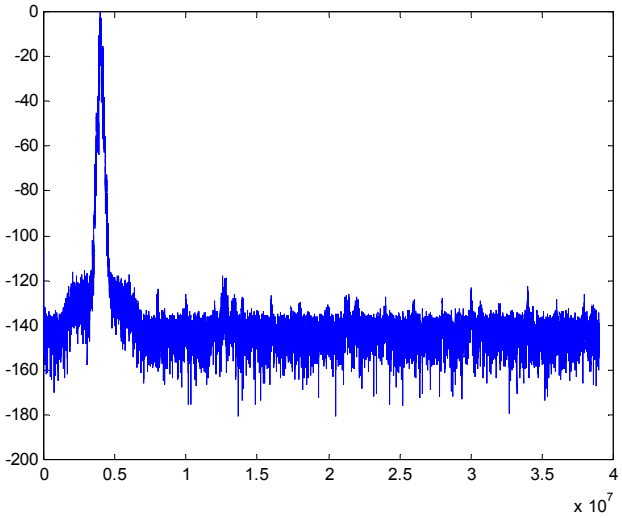


FIGURE 36. DIGITAL OUTPUT WITH HALFBAND

CDMA2000-1x

The device is configured for QASK and outputting four channels of CDMA in continuous mode with no phase equalization. The 16-bit I and 16-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of f_S = 1.2288kHz. The shaping FIR is programmed to interpolate by x4 with a dataspan of 12. The filter frequency response is shown in Figure 37. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 4, 8, 12, and 16MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 38, utilizing the on-board HI5828 dual DAC. The stimulus file is 511 samples of pseudo random QPSK data.

TABLE 6. CDMA2000-1X CONFIGURATION

Clock Rate CLK =	80MHz
Sample Frequency f_S =	1.2288MHz
Configuration File:	CDMA2000_1x.js
Filter File:	IS95CoefScaled.imp
Stimulus File:	qpskpn.imp
Dynamic Configuration File:	N/A

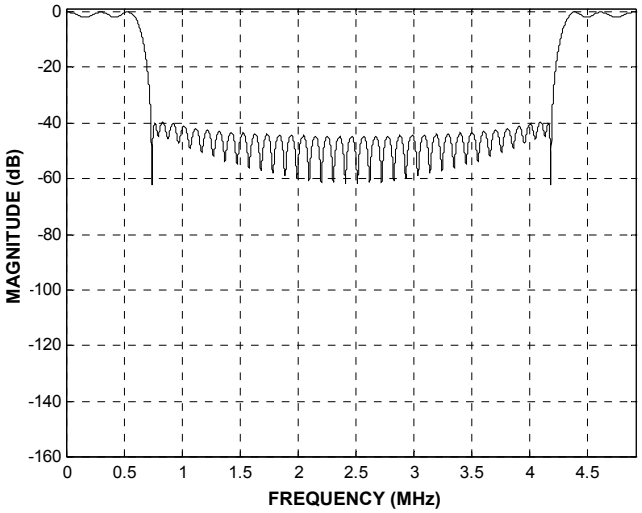


FIGURE 37. SHAPING FILTER FREQ. RESPONSE

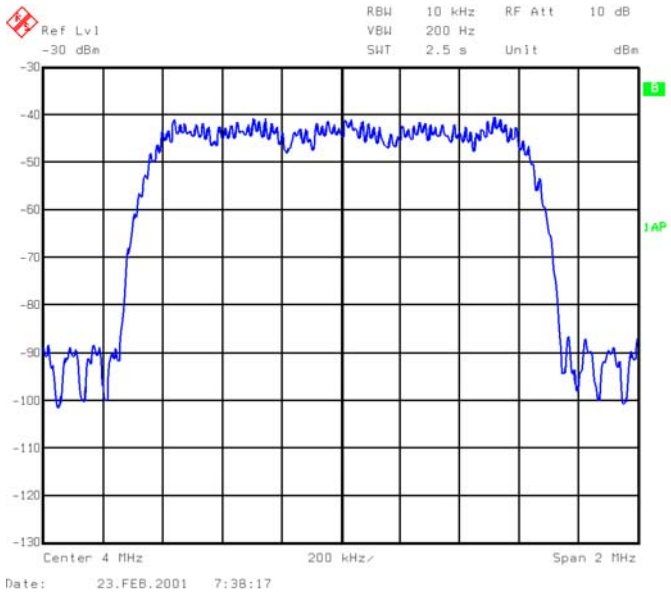


FIGURE 38. ANALOG SPECTRUM

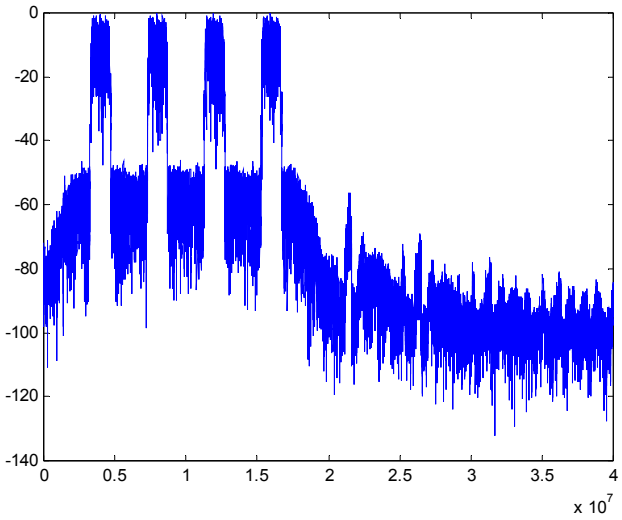


FIGURE 39. DIGITAL OUTPUT

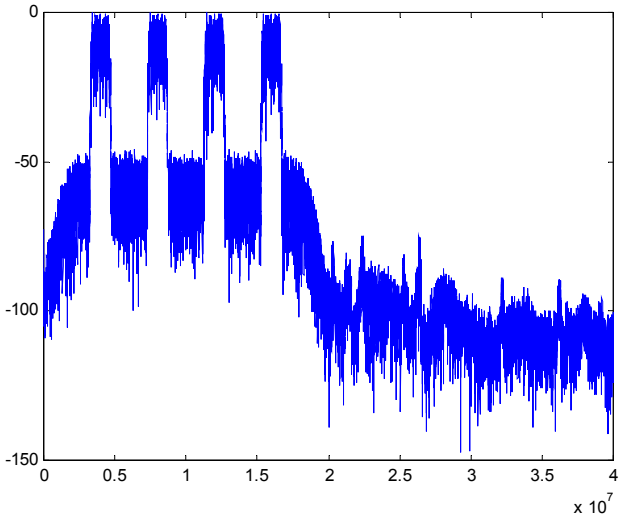


FIGURE 40. DIGITAL OUTPUT, HALFBAND ENABLED

CDMA2000-3x MC

The device is configured for outputting three channels of CDMA in continuous mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA-SDC inputs, and the symbol NCO is programmed to provide a sample rate of f_S = 1.2288kHz. The shaping FIR is programmed to interpolate by x4 with a dataspan of 12. The filter frequency response is shown in Figure 41. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 4, 5.25, and 6.5MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 42, utilizing the on-board HI5828 dual DAC, and the vector analysis is shown in Figure 43. The stimulus file is 511 samples of pseudo random QPSK data.

The digital data was collected utilizing a 32K FFT with the results shown in Figure 39. Enabling the halfband, the digital performance is improved as shown in Figure 40.

TABLE 7. CDMA2000-3X MC CONFIGURATION

Clock Rate CLK =	61.44MHz
Sample Frequency f_S =	1.2288MHz
Configuration File:	CDMA2000_3x_MC.js
Filter File:	IS95CoefScaled.imp
Stimulus File:	qpskpn.imp
Dynamic Configuration File:	N/A

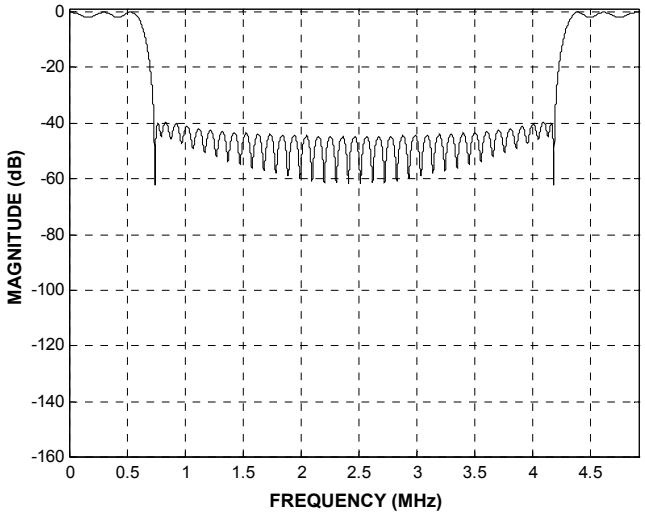


FIGURE 41. SHAPING FILTER FREQUENCY RESPONSE

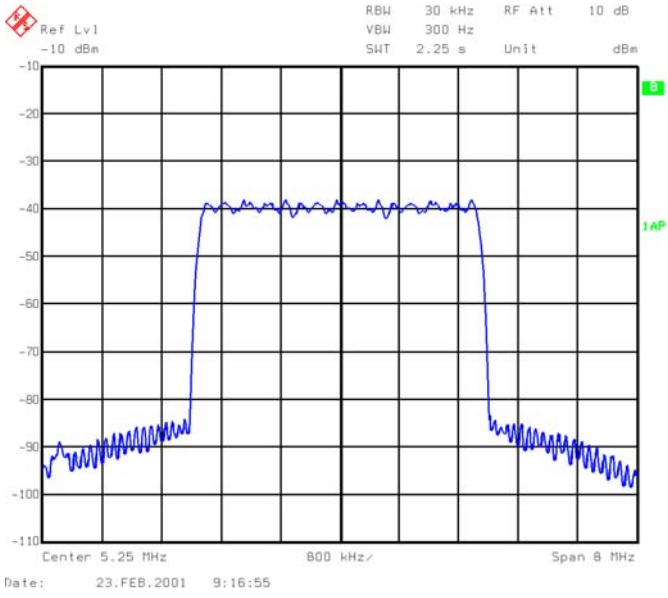


FIGURE 42. ANALOG SPECTRUM

The digital data was collected utilizing a 32K FFT with the results shown in Figure 43. Enabling the halfband, the digital performance is improved as shown in Figure 44.

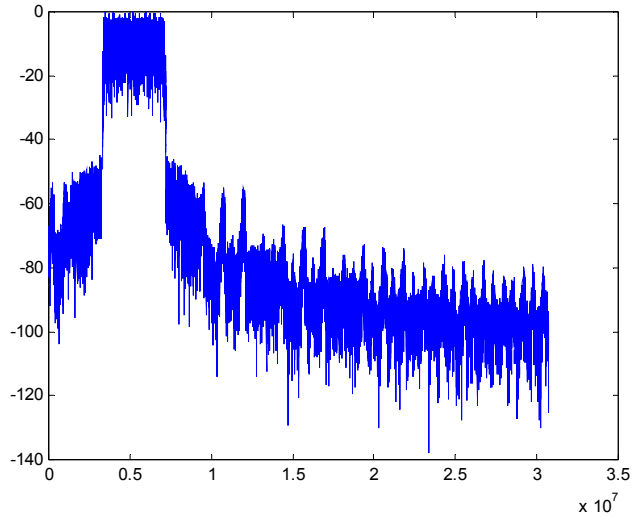


FIGURE 43. DIGITAL OUTPUT

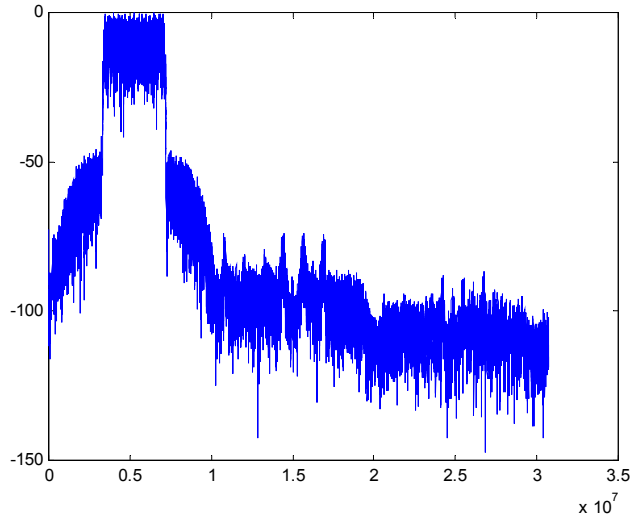


FIGURE 44. DIGITAL OUTPUT, HALFBAND ENABLED

CDMA-2000-3x DS

The device is configured for outputting one channel of CDMA in continuous mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of f_S = 960kHz. All four channels of the device are utilized in polyphase mode to create this wideband channel. The serial input samples are parsed into four inputs, with each channel receiving every fourth input, as shown in Figure 45. The shaping FIR is programmed to interpolate by x16 with a dataspan of 4, with the filters loaded in a time shifted configuration as shown in Figure 46. The coefficient location shift in the filters allows for the polyphased outputs from each channel to be re-combined in the summer to effectively produce a single wideband channel. The filter frequency response is shown in Figure 47. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 8MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 48, utilizing the on-board HI5828 dual DAC. The stimulus file is 511 samples of pseudo random QPSK data.

TABLE 8. CDMA2000-3X DS CONFIGURATION

Clock Rate CLK =	80MHz
Sample Frequency f_S =	0.960MHz overall 3.84MHz
Configuration File:	CDMA2000_3x_DS.js
Filter File:	IS95CoefScaled0-3.imp
Stimulus File:	parsedqpskpn0-3.imp
Dynamic Configuration File:	N/A

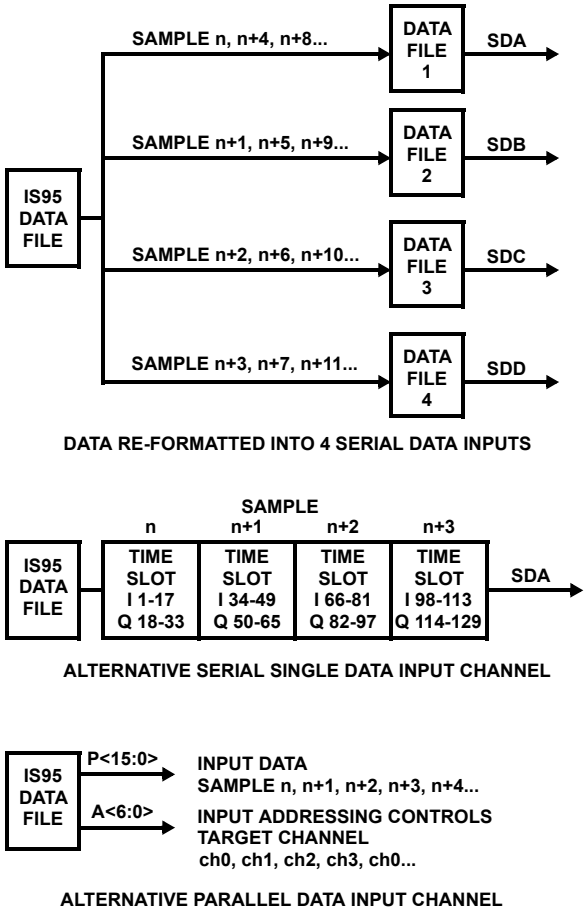


FIGURE 45. MULITPLE CHANNEL INPUT DATA FORMAT

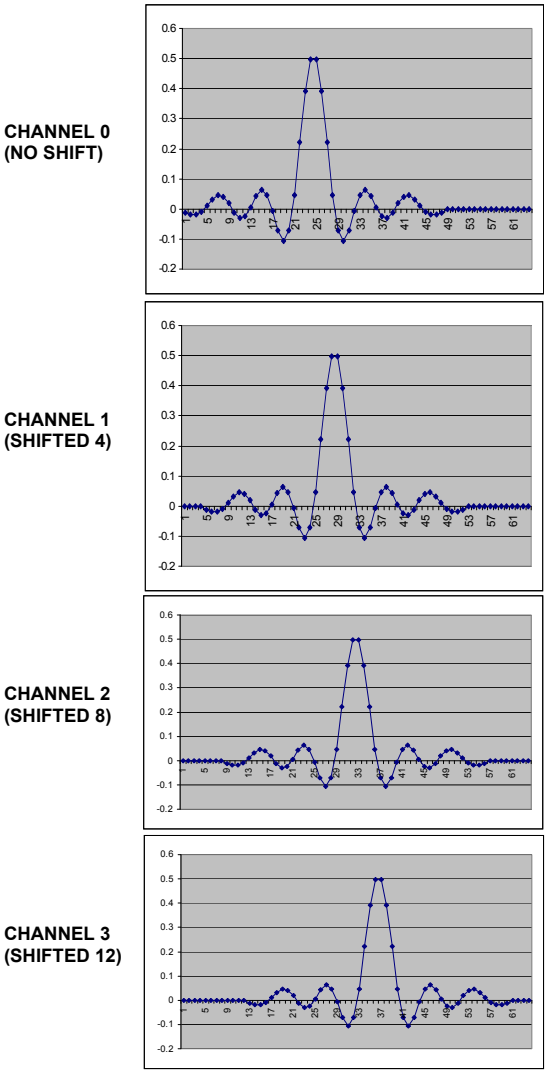


FIGURE 46. FILTER ALIGNMENT

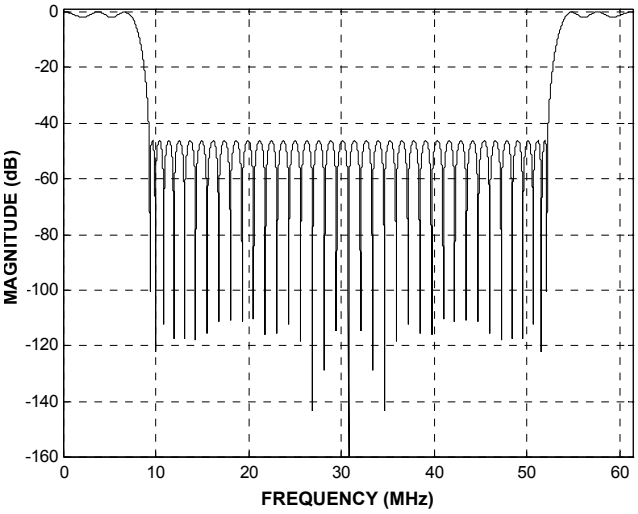


FIGURE 47. SHAPING FILTER FREQ. RESPONSE

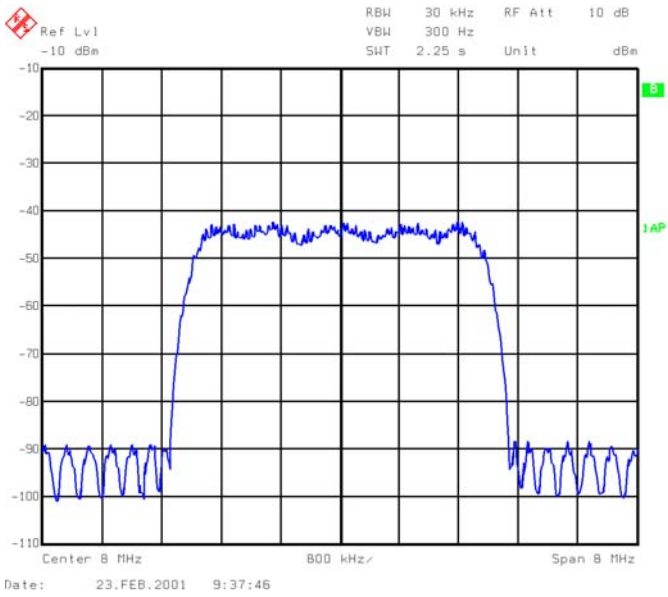


FIGURE 48. ANALOG SPECTRUM

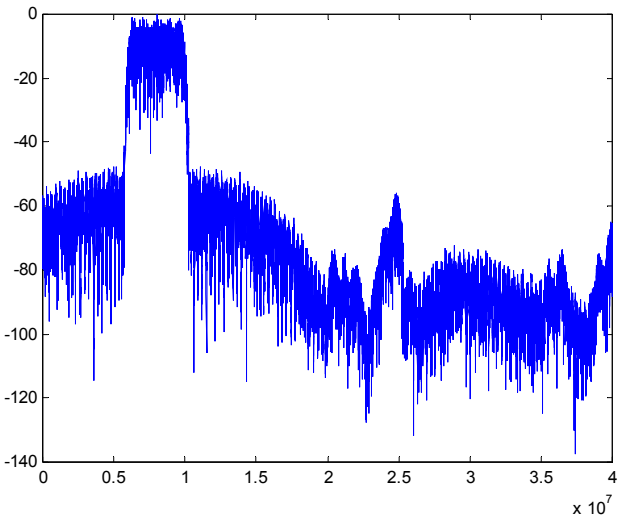


FIGURE 49. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 49. Enabling the halfband, the digital performance is improved as shown in Figure 50.

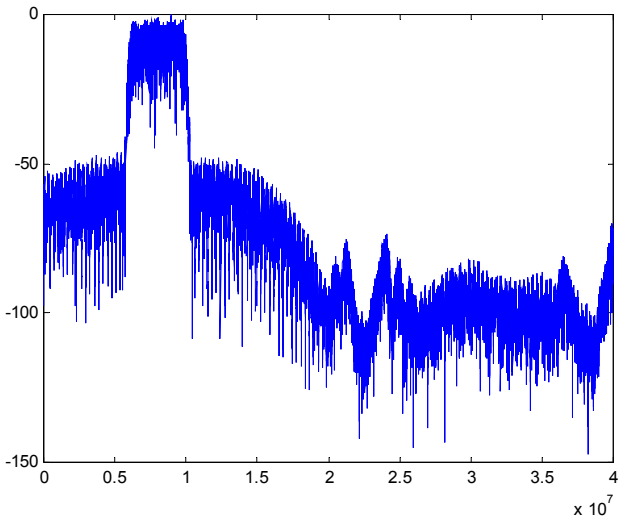


FIGURE 50. DIGITAL OUTPUT, HALFBAND ENABLED

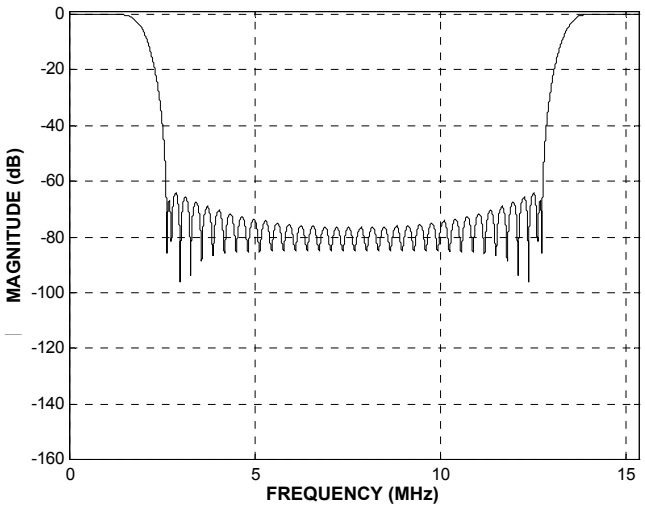


FIGURE 51. SHAPING FILTER FREQ. RESPONSE

UMTS

The device is configured for outputting one channel of UMTS in continuous mode. The 12-bit I and 12-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of f_S = 960kHz. All four channels of the device are utilized in polyphase mode to create this wideband channel. The serial input samples are parsed into four inputs, with each channel receiving every fourth input, as shown in Figure 51. The shaping FIR is programmed to interpolate by x16 with a dataspan of 4, with the filters loaded in a time shifted configuration as shown in Figure 52. The coefficient location shift in the filters allows for the polyphased outputs from each channel to be re-combined in the summer to effectively produce a single wideband channel. The filter frequency response is shown in Figure 53. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 7.3424MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 54, utilizing the on-board HI5828 dual DAC. The stimulus file is 511 samples of pseudo random QPSK data..

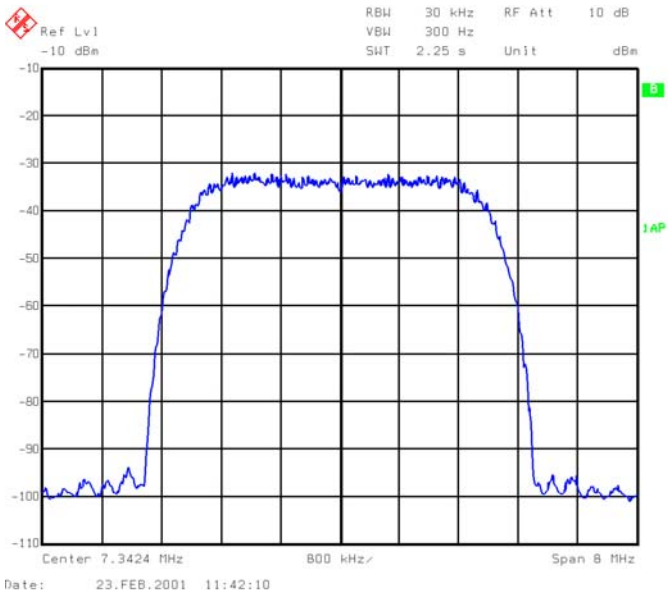


FIGURE 52. ANALOG SPECTRUM

TABLE 9. UMTS CONFIGURATION

Clock Rate CLK =	61.44MHz
Sample Frequency f_S =	0.960MHz overall 3.84MHz
Configuration File:	UMTS.js
Filter File:	UMTS0-3.imp
Stimulus File:	parsedqpskpn0-3.imp
Dynamic Configuration File:	N/A

The digital data was collected utilizing a 32K FFT with the results shown in Figure 51. Enabling the halfband, the digital performance is improved as shown in Figure 51.

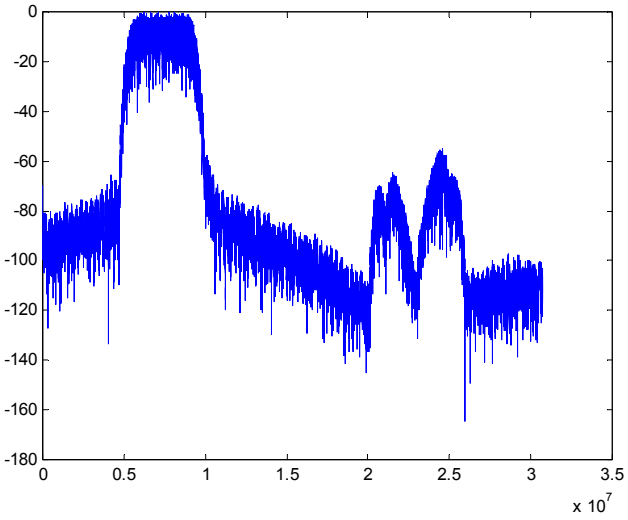


FIGURE 53. DIGITAL OUTPUT

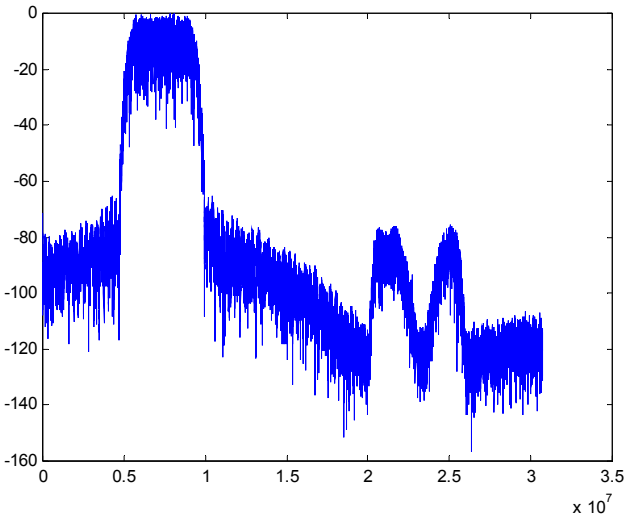


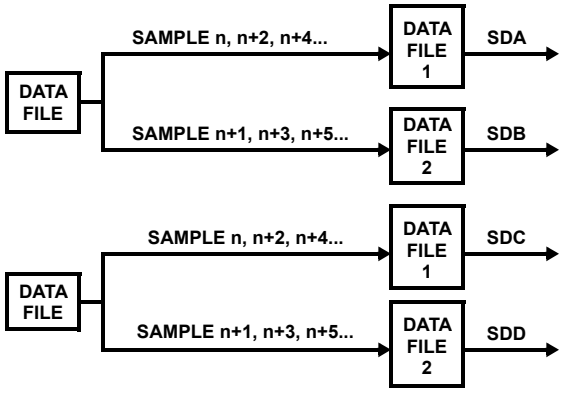
FIGURE 54. DIGITAL OUTPUT, HALFBAND ENABLED

UMTS-Two Channels

The device is configured for outputting two channel of UMTS in continuous mode. The 12-bit I and 12-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of f_S = 1.92MHz. All four channels of the device are utilized by combining 2 channels in polyphase mode to create each of the two wideband channels. The serial input samples are parsed into two inputs, with each channel receiving every second input, as shown in Figure 55. The shaping FIR is programmed to interpolate by x8 with a dataspan of 6, with the filters loaded in a time shifted configuration as shown in Figure 56. The coefficient location shift in the filters allows for the polyphased outputs from each channel to be recombined in the summer to effectively produce a wideband channel. The filter frequency response is shown in Figure 57. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 5 and 12MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 58, utilizing the on-board HI5828 dual DAC. The stimulus file is 511 samples of pseudo random QPSK data..

TABLE 10. UMTS CONFIGURATION

Clock Rate CLK =	92.16MHz
Sample Frequency f_S =	1.92MHz overall 3.84MHz
Configuration File:	UMTS2.js
Filter File:	UMTS_44t0-1.imp
Stimulus File:	2parsedqpskpn0-1.imp
Dynamic Configuration File:	N/A



DATA RE-FORMATTED INTO 4 SERIAL DATA INPUTS

FIGURE 55. MULITPLE CHANNEL INPUT DATA FORMAT

CHANNELS 0 AND 2 (NO SHIFT)

CHANNELS 1 AND 3 (SHIFTED 4)

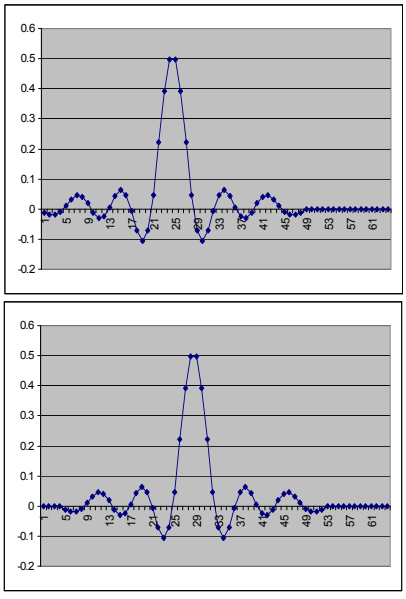


FIGURE 56. FILTER ALIGNMENT

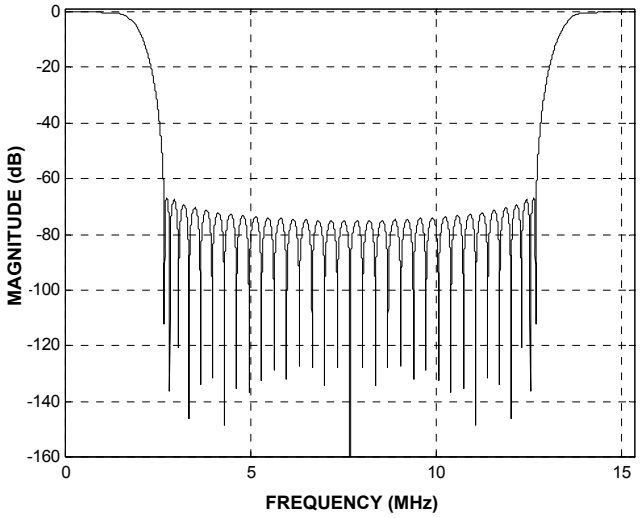


FIGURE 57. SHAPING FILTER FREQ. RESPONSE

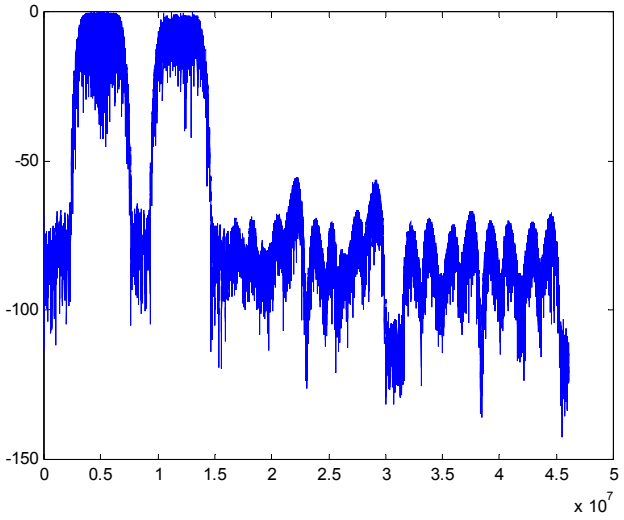


FIGURE 59. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 58. Enabling the halfband, the digital performance is improved as shown in Figure 59.

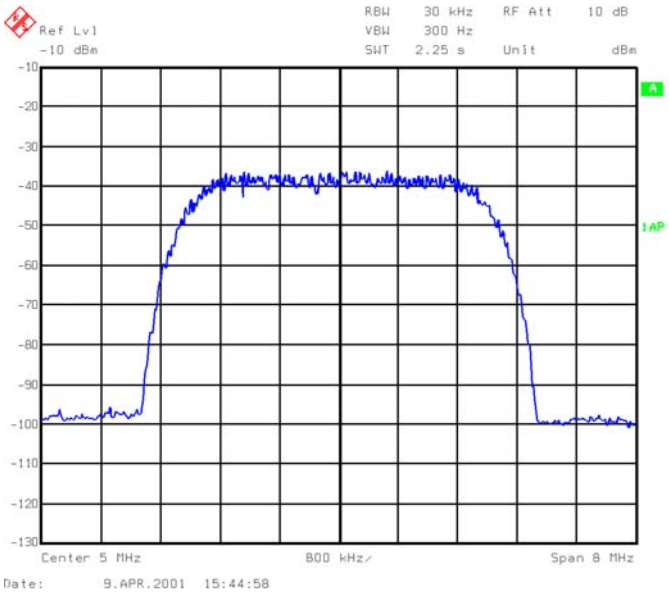


FIGURE 58. ANALOG SPECTRUM

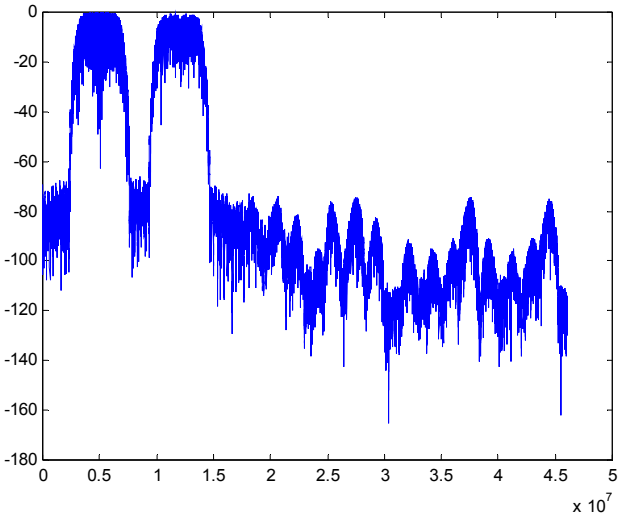


FIGURE 60. DIGITAL OUTPUT, HALFBAND ENABLED

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