Reducing The Minimum Decimation Factor Of The HSP50016 Digital Down Converter

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Introduction

This Application Note discusses a method for reducing the minimum decimation factor of the Intersil HSP50016 Digital Down Converter (DDC). As will be described in detail in this Application Note, reduction in the minimum decimation factor is accomplished by sample rate expanding the data stream which would normally be directly input to the DDC by a factor L (placing L-1 zero valued samples between each sampled data point). While this sample rate expansion process effectively reduces the maximum input sampling rate that the aggregate circuit (DDC and sample rate expander) can accept by a factor of L, the ratio of the maximum output bandwidth to input sample rate of the aggregate circuit is increased by a factor of L. The output bandwidths as a function of HDF decimation factor R, input sample rate of the aggregate circuit f_{SA}, and sample rate expansion L are:

$$3dB\ BW = 0.13957\ Lf_{SA}/R \quad \text{(EQ. 1)}$$

$$-102dB\ BW = 0.19903\ Lf_{SA}/R \quad \text{(EQ. 2)}$$

($f_{SA} = f_S/L$ where f_S is the frequency of CLK).

The DDC is a fully programmable single chip down converter architected to meet a wide range of down convert applications. A top level functional block diagram of the DDC Architecture is shown in Figure 1. The principle goal of the DDC is to filter and translate a band of interest to baseband and to output the band of interest at a sample rate commensurate with its bandwidth.

The decimation occurs in a two step process. Once the center of the band of interest is shifted to DC by the quadrature modulator, the real and imaginary outputs are each passed to a High Decimation Filter (HDF). The decimation factor of the HDFs, denoted R, is programmable from a minimum of 16 to a maximum of 32,768. The outputs of the HDF filters must be scaled for gain compensation.

The lowpass response of the HDF has a gradual roll off characteristic requiring a subsequent conventional FIR to achieve a sharp transition. The DDC employs a fixed shaping filter for ease of use. The output bandwidth of the DDC is a function of the input sampling rate, the programmable HDF decimation factor and the fixed shape of the FIR. This relationship is:

$$-3dB\ BW = 0.13957\ f_S/R \quad \text{(EQ. 3)}$$

$$-102dB\ BW = 0.19903\ f_S/R \quad \text{(EQ. 4)}$$

where BW is the double sided bandwidth and f_S is the input sample rate.

The FIR filter's passband compensates for the roll off inherent in the passband of the HDF filter to meet the goal of a low passband ripple [1].

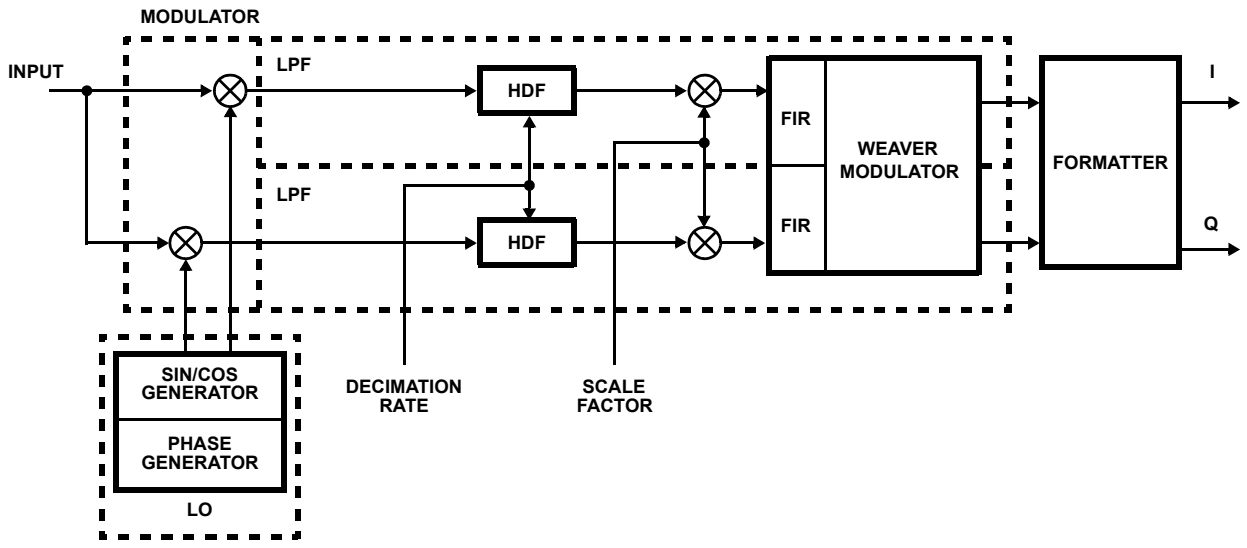

FIGURE 1. DDC FUNCTIONAL BLOCK DIAGRAM

The FIR filter automatically decimates by a factor of 4 if a quadrature output format has been selected. When a real output is selected, the FIR filters in the DDC automatically decimate by a factor of 2. The FIR decimation factor is denoted R_{FIR}. In the real output mode the FIR outputs are spectrally shifted by one fourth of the output sampling frequency and combined to produce a two sided spectrum. This process is conceptually performed by the Weaver Modulator [2] following the FIR filter pair.

We see that the minimum DDC decimation factor, R_T, is given by:

$$R_{TMIN}\ (M) = R_{MIN} \times R_{FIR} = 16 \times 4 = 64 \qquad \text{(EQ. 5)}$$

The minimum decimation factor for quadrature output mode is 16 x 4 = 64.

The minimum decimation factor for real output mode is 16 x 2 = 32.

The resulting signal is converted into one of several selectable formats for output. See reference [1] for a detailed description of the DDC and its operation.

A simple procedure can be used to reduce the minimum aggregate decimation factor of the DDC with a small amount of external circuitry. ***The trade-off in reducing the aggregate decimation factor is a one to one reduction in maximum input sampling rate.***

Reduction of the Minimum Decimation Factor

The minimum decimation factor of the DDC can be reduced by using external circuitry to convert the DDC from a strictly decimating device to a rate change device. By doing this, the DDC and external circuitry can first interpolate the input signal to a higher sampling rate before decimating it. This restricts the sampling frequency, f_S and correspondingly the bandwidth, of the input signal to be less than the clock frequency of the DDC. The result however, is a reduction in the end-to-end decimation factor of the aggregate circuit.

A rate change filter is an interpolation (rate increasing) filter combined with a decimation (rate reducing) filter. The combining of the actual filtering processes is done by implementing the filter process that requires the narrowest bandwidth of the two.

Because interpolation via digital filtering is not introduced in the DDC Data Sheet, it is presented at a top level here.

Interpolation

Interpolation is the increase in the sampling rate of a signal while preserving its original spectral content. The first step in interpolation is to stuff L-1 zero valued samples between each valid input sample to expand the sampling rate by a factor of L. The zero stuffing causes the original signal spectrum to be repeated L-1 times. To perform the actual interpolation, the zero valued input samples must be converted to approximations of signal samples. This is equivalent to preserving the original signal spectrum. Thus, the zero stuffed input stream is filtered by a lowpass filter which has its passband at the original spectrum location and filters out all of the repeated spectra. This process is illustrated in Figure 2.

Rate Change

The top level block diagram of a rate change filter [2] is shown in Figure 3A. In the diagram the sampling rate of the incoming signal is first expanded by a rate L by placing L-1 zero valued samples between each original sample. The lowpass filter following the sample rate expander is designed to: 1) remove the L-1 spectral images which result from the zero padding; 2) multiply the result by a gain of L to compensate for the power loss that occurs when the spectral images are removed; and 3) limit the width of the spectrum to allow sample rate compression by R without aliasing. An example of this process is illustrated in Figure 3B.

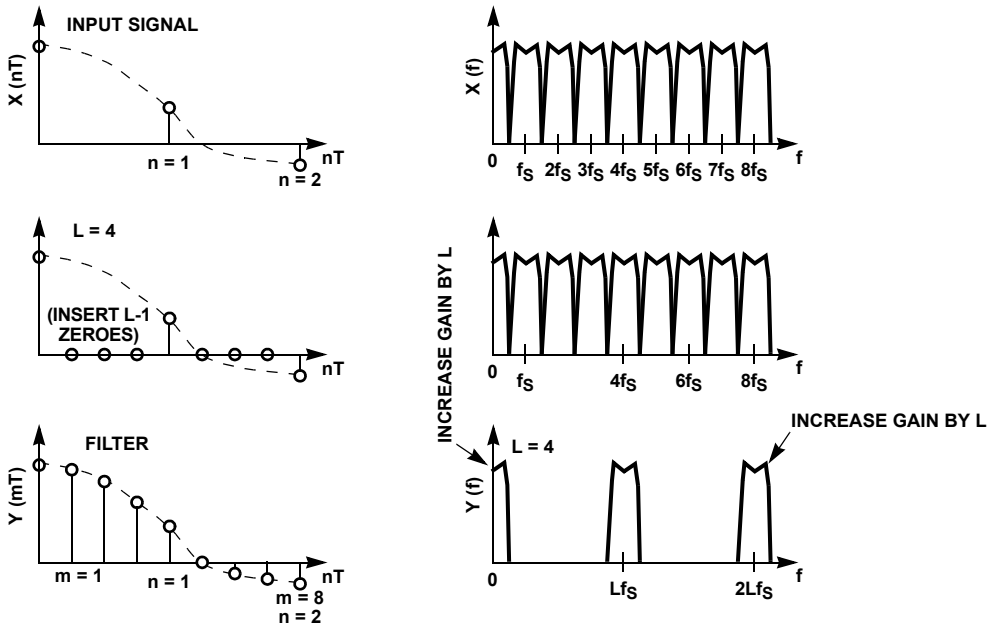

FIGURE 2. BLOCK DIAGRAM SPECTRAL REPRESENTATION OF THE RATE CHANGE PROCESS

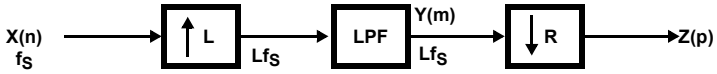

FIGURE 3A. TOP LEVEL BLOCK DIAGRAM OF A RATE CHANGE FILTER

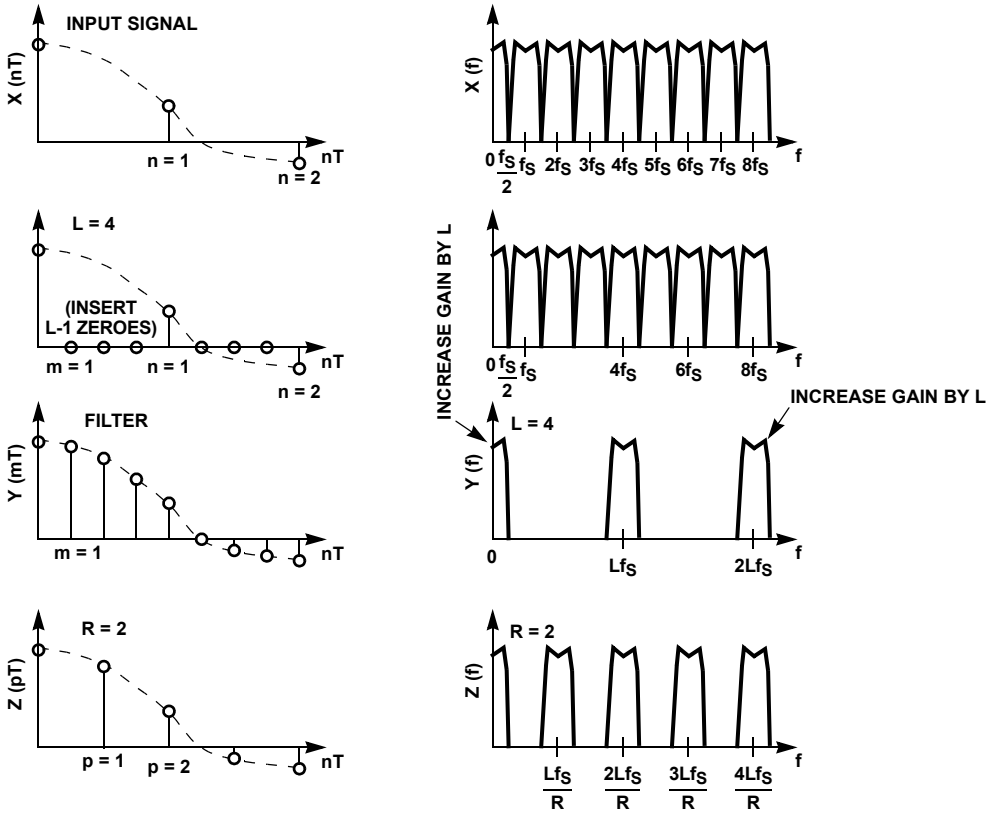

FIGURE 3B. SPECTRAL REPRESENTATION OF THE RATE CHANGE PROCESS

The first and third design criteria are combined by taking the more severe (narrowest bandwidth and shape factor) of the two.

In most implementations the least common denominator (LCD) of L and R is 1. In the application described here, this is not generally true because the DDC itself is not a rate change device.

The DDC in a Rate Change Configuration to Reduce the Minimum Decimation Factor

Figure 4 shows a conceptual block diagram of the modulation and filter processes in one of the two real processing chains in the DDC. The two stage decimation filter configuration is a conventional architecture [2] with the exception of the scaling multiplier between the first sample rate compressor and the second lowpass filter. The scaling multiplier is used to compensate for the variable gain of the programmable HDF [1,3,4,5,].

The input to the DDC is first multiplied by a sinusoid from the digital local oscillator (LO). The sinusoids for the inphase and quadrature paths are offset in phase by 90 degrees. The product is passed to the HDF.

Placing a sample rate expander in front of the HDF and using the fact that the multiplication of the input signal by the LO is a linear operation, we can redraw Figure 4 to get the rate change capability shown in Figure 5.

In the configuration shown in Figure 5 it is assumed that the constraint placed on the lowpass filtering by decimation is more severe than the interpolation constraint. This is in general the case when the decimation factor of the DDC is higher than the interpolation factor being generated by the external sample rate expander.

From Figure 5 it can be seen that the sample rate of the input to the sample rate expander, f_{SA}, has a maximum value of f_S/L where f_S is the DDC clock.

The sample rate expander can be constructed simply as a divide by L counter and a series of AND gates. Example implementations are shown in Figure 26, found later in this application note.

Example: Decimation By 8

As an example case we will use the DDC to decimate by 8 with a quadrature output. Note that this is lower than the decimate by 64 that the DDC can do in this mode. In this example the HDF section is programmed to decimate by the minimum value of 16 and the FIR section automatically decimates by 4. The aggregate DDC decimation factor is 16 x 4 = 64. To get a decimation factor of 8 we must interpolate by

$$L = \frac{\text{DDC DECIMATION}}{\text{DESIRED DECIMATION}} = 64/8 = 8 \qquad \text{(EQ. 6)}$$

The sample rate expander therefore, pads 7 zero samples between each sample that enters it. The maximum sampling frequency of the input signal is $f_S/8$. For the maximum DDC clock of 75MHz, the maximum input clock for this example is $\frac{75\text{MHz}}{8} = 9.375\text{MHz}$.

Assume that the input signal is wideband and that it is sampled at 2.5 times the highest frequency of interest, 3.75MHz. The resulting spectrum at the input to the sample rate expander is shown in Figure 6. Notice in the figure that the anti-aliasing filter design, has been relaxed, allowing aliasing to occur at frequencies above the maximum frequency of interest.

When the input signal has passed through the sample rate expander and has been padded with 7 zero samples between each input sample, the one sided spectrum illustrated in Figure 7 results. Also shown in the figure is the HDF lowpass response. Notice that the power in the original signal and each image is reduced by a factor of 8, or 18dB, from the input power level, defined as 0dB in the figure. This phenomenon occurs in digital interpolation because padding by L-1 zeros adds L-1 spectral repetitions without adding power.

The interpolation process is completed by removing the spectral images via a lowpass filter operation. This loss of power of 20 x log(L) dB in the filtering operation would result in a corresponding loss in dynamic range, unless the signal is scaled to compensate for the reduced amplitude.

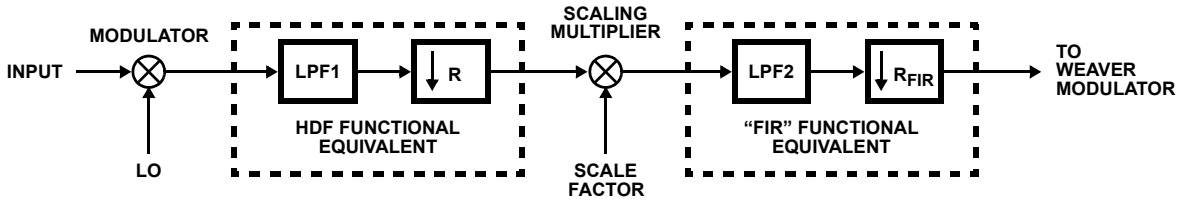

FIGURE 4. CONCEPTUAL BLOCK DIAGRAM OF HALF OF THE DDC MODULATION AND FILTER PROCESS

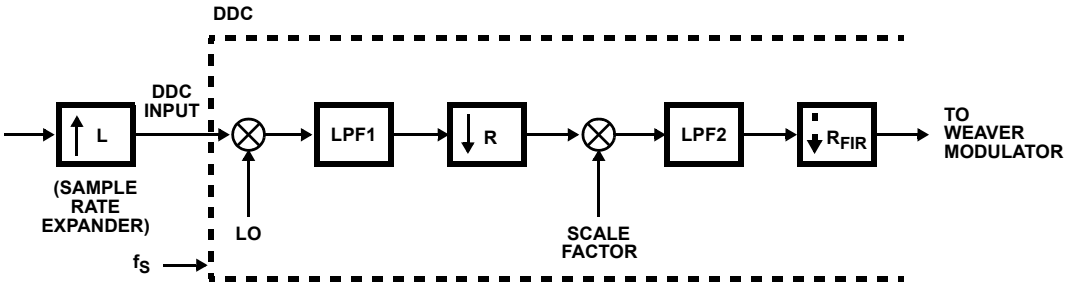

FIGURE 5. CONCEPTUAL BLOCK DIAGRAM OF ONE SIDE OF THE DDC MODULATION AND FILTER PROCESS WITH A SAMPLE RATE EXPANDER

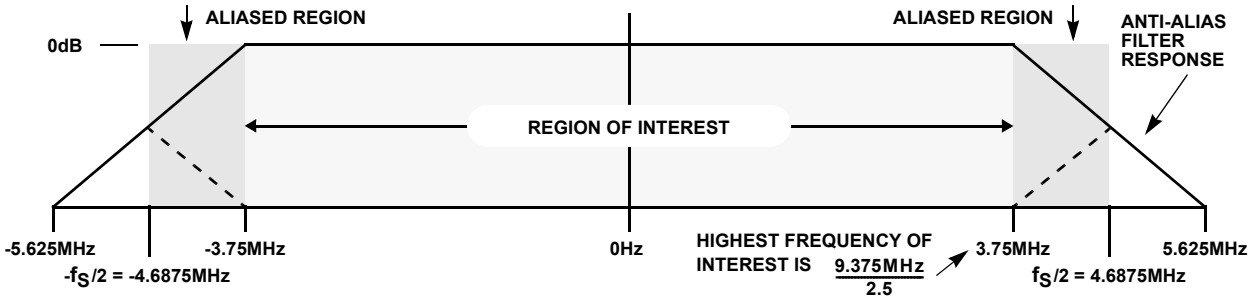

FIGURE 6. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE SUPERIMPOSED

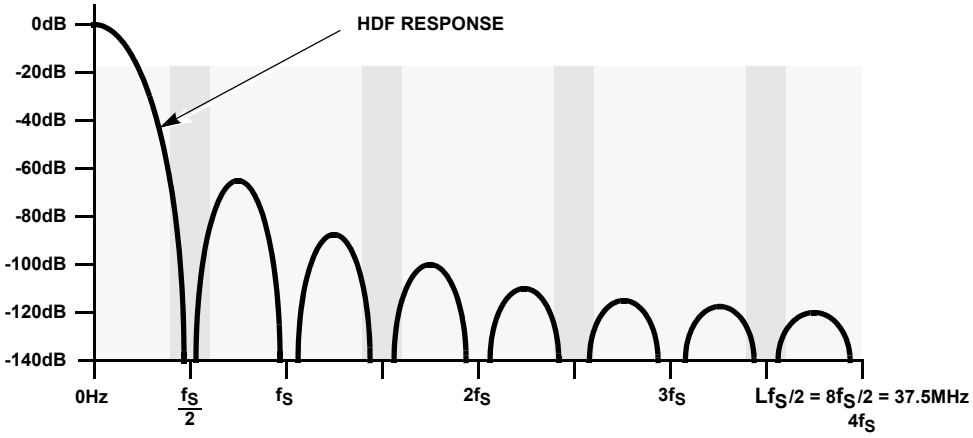

FIGURE 7. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE SUPERIMPOSED

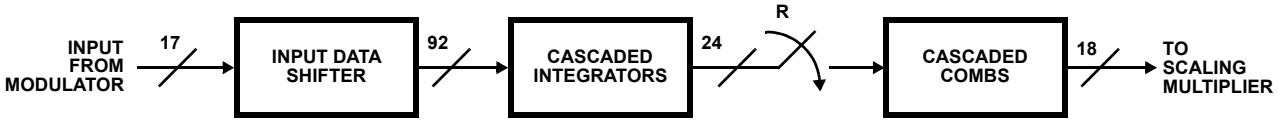

FIGURE 8. TOP LEVEL BLOCK DIAGRAM OF THE HIGH DECIMATION FILTER

The output -3dB bandwidth can be calculated from Equation 1 where f_{SA} is equal to 9.375 megasamples per second (MSPS). We get:

-3dB BW = 0.13957 x 8 x 9.375MSPS/16 = 654.234kHz.

From this result we see that for a DDC clock of 75MHz the maximum output bandwidth has not changed. What has changed is the maximum output bandwidth relative to the actual input sample rate of 9.375MSPS.

$$\text{3dB BW} = \frac{0.13957 f_{SA}}{R}$$

By rearranging and putting in terms of f_S = DDC clock rate, we have:

$$\frac{BW_{3dB}}{f_S} = \frac{0.13957}{R} \Rightarrow \frac{0.13957L}{R} \quad \text{(EQ. 7)}$$

L = 2, 4, 8

for the aggregate circuit.

Implementation Details

Figure 8 shows a more detailed block diagram of the HDF. The HDF is an efficient, multiplier free, decimating lowpass filter for moderate to high decimation rates[3]. As shown in the Figure, the HDF actually decimates before completion of the filtering process. However, the process is functionally equivalent to the process of filtering by LPF1 followed by sample rate compression by a rate R shown in Figure 4.

The frequency domain response of an unscaled HDF is:

$$H(f) = (\text{Sin}(\pi f)/\text{Sin}(\pi f R))^5 \quad \text{(EQ. 8)}$$

The DC gain of this response is R^5. This gain must be compensated for by multiplying by the inverse of the DC gain. The gain compensation is distributed between the input and output of the HDF in the DDC implementation. The gain compensation at the input of the HDF is accomplished via a shift register labeled the Input Data Shifter in Figure 8. Consequently, this gain compensation is in the form of powers of two. The gain compensation at the output of the HDF is accomplished via a multiplier. The multiplier compensates for non powers of two in the gain compensation.

The HDF Input Data Shifter positions the input data, as a function of the HDF decimation rate, so that the MSB of the output data will be aligned with the MSB of the output bus. The data shifter is programmed in terms of a data shift value. That is, the number of bits between the LSB of the input to the HDF and the LSB of the HDF. The data shift equation is:

$$\text{Data Shift} = 75 - \text{Ceiling}(5 \log_2(R)) \quad \text{(EQ. 9)}$$

where Ceiling(X) denotes taking the next greatest integer if X has a non integer component; R is the HDF decimation factor; in point of fact, the shift divides the HDF gain by a value which is greater than or equal to R^5 to guarantee that the input to the scaling multiplier is between 0.5 non inclusive and 1 inclusive. For a detailed explanation see reference [3].

After the data shift has been performed the HDF gain at the output is given by:

$$\text{HDF Gain} = R^5/2^{\text{CEILING}(5\text{LOG}_2(R))} \quad \text{(EQ. 10)}$$

The compensating scale factor, which is the input to the Scaling Multiplier quantized to 16 bits, is given by the equation:

$$\text{Scale Factor} = \left[2^{\text{CEILING}(5\text{LOG}_2(R))}\right]/R^5 \quad \text{(EQ. 11)}$$

The computed scale factor can take on values from 1 inclusive to 2 non inclusive. The programmable quantized scale factor can take on values from 0 to $2 - 2^{-15}$.

The validity of the HDF gain equation is predicated on the correct programming of the HDF data shifter. See referenced [1] for details.

The following two examples are used to illustrate the gain compensation procedure:

Example 1: R = 512

In this example we are decimating by a power of 2. The Data Shift value is:

$75 - \text{Ceiling}(5 \log_2(512)) = 30$.

The Scale Factor value is:

$2^{\text{CEILING}(5\text{LOG}_2(512))}/512^5 = 1$.

Example 2: R = 513

The Data Shift value is:

$75 - \text{Ceiling}(5 \log_2(513)) = 29$.

The Scale Factor value is:

$2^{\text{CEILING}(5\text{LOG}_2(513))}/513^5 = 1.98058267$

Interpolation Gain Compensation

An explanation of how to preserve the DDC's dynamic range when reducing its minimum decimation rate is now given in detail. In most normal operating conditions this procedure is simple and straight forward. Under certain worst case conditions however, special considerations must be made. We describe the straight forward case first, then detail how to handle the worst case conditions.

The removal of spectral images created in the sample rate expansion process is accomplished by the lowpass filtering in the DDC. As mentioned above, the removal of the images results in a loss in gain since no power is added to the signal during the sample rate expansion process. Power is removed in the lowpass filter process. Dynamic range through the DDC can be preserved by compensating for the gain loss due to the spectral image removal by adjusting the gain through the HDF.

Because the lowpass filter process is a two step process involving the HDF and FIR, the HDF may not suppress all images to the attenuation required to prevent overflow during the standard scaling process. This is the case in Figure 14 as will be explained in detail below. As long as the images are suppressed sufficiently to preclude overflow in the HDF and scaling operation however, no distortion occurs in the process.

Standard Gain Compensation

For an example of standard gain compensation, assume that an overall decimation rate of 4 is desired in the DDC. The input samples are expanded by 16 by placing 15 zero valued samples between each input sample. The resulting spectrum is illustrated in Figure 9.

(Note: Figures 9 through 24 show the repeated input spectrum superimposed on the HDF response curve. These superimpositions assume that the down convert frequency is zero. The analysis holds for any valid down convert frequency. Also shown in the figures by the vertical solid lines are the positions of the images of near DC areas of the spectra.)

Assume that the input signal consists of two equal amplitude tones, one at DC (desired in this example) and one at 4/5 of the pre-expanded input sampling frequency (to be ultimately rejected in this example). In the expanded spectrum the DC component repeats as illustrated by the vertical solid lines in Figure 9 and the 4/5 sampling frequency tone is repeated at each interface between the two shaded areas in the figure. Each tone is at -6dB on the pre-expanded input and down 30dB on the expanded spectrum.

To compensate for the gain loss due to the rejection of images requires a 24dB gain in the HDF. The requirement to prevent overflow in the gain compensation operation is that the sum of the signal power after compensation is $\leq$ 0dB.

As can be seen in Figure 9 all DC images lie in the HDF nulls. Since the original DC component is at -6dB after compensation, it is required that the sum of the power in the original 4/5 sampling frequency tone and it's images be $\leq$ -6dB after compensation. From the HDF curve it is determined that the total power from the tone and its images is approximately -10.9dB. As a result, no overflow will occur in the HDF or scaling multiplier due to gain compensation. The residual signals are then filtered in the FIR. The compensation scale factor required is equal to the interpolation factor, L. Combining the interpolation gain compensation with the HDF response gain compensation we have a total compensation of L/R^5. We now rewrite Equations 9 and 11 to incorporate the interpolation gain compensation.

$$\text{Data Shift} = 75 - \text{Ceiling}(\log_2(R^5/L)) \quad \text{(EQ. 12)}$$

$$\text{Scale Factor} = \left[2^{\text{CEILING}\left(\text{LOG}_2(R^5/L)\right)}\right]\left[\frac{L}{R^5}\right] \quad \text{(EQ. 13)}$$

Equations 12 and 13 are used when no overflow is possible in the HDF as a result of the interpolation and scaling process.

Special Case 1 - Overflow Possibilities When the Interpolation Factor Is Less Than or Equal to the HDF Decimation Factor

Figures 9 through 23 show interpolated spectra superimposed on the HDF filter response curve for interpolation cases 16 through 2. The figures are supplied to illustrate the possibility of overflow in the extreme case where full scale inputs to the DDC are supplied and all of the dominant spectral components meet two criteria.

- First, they are all within 1/125th of the main lobe
- Second, the majority of them generate an image or images that lie at the peaks of the first or second side lobe. (The peak value of the first HDF sidelobe is 1.168×10^{-4} which is approximately equal to 1 - the magnitude of the mainlobe at a frequency of 1/125th of the first HDF null).

(Note: the above paragraph describes a condition, specifically a full scale input, which should not occur in typical operations. The description of this special case is included for completeness).

To illustrate the potential for overflow in the extreme case described above we select a full scale single tone input which is mixed to DC in the down convert section of the DDC. The dark vertical lines in the figures highlight DC images. Examining Figure 14, the interpolate by 11 example, we see that the first image lies at 6.818MHz for a 75MSPS DDC input rate. This image is very near the 6.713MHz peak of the first HDF sidelobe.

The attenuated magnitude of the first and second images and fifth and sixth (not including the attenuation due to sample rate expansion) sum to approximately 5.109×10^{-4}. As a result, if Equations 12 and 13 are used for gain compensation, then the peak signal value coming out of the HDF would be 1.0005109 and the HDF would overflow. This would generate catastrophic errors.

To correct for the image components we can modify Equations 12 and 13 as follows: Let Sc be defined as the sum of the signal component magnitudes in the original spectrum times the normalized HDF response. For a single DC input to the HDF Sc = 1. Let Slg be the sum of the compensated image magnitudes times the normalized HDF response. In the interpolate by 11 example Slg $\cong$ 0.0005109.

If Sc + Slg is greater than 1, then

Data Shift =

$$75 - \text{Ceiling}(\log_2(R^5(Sc + Slg)/L)) \quad \text{(EQ. 14)}$$

Scale Factor =

$$\left[2^{\text{CEILING}(LOG_2(R)\ (SC + SLG)/L))}\right]\ [L(Sc + SLG)R^5] \quad \text{(EQ. 15)}$$

Applying Equations 14 and 15 would cause a negligible loss in dynamic range.

The image power which is passed in the HDF will be removed in the subsequent FIR filter.

It can be observed from Figures 9 through 23 that for the HDF set to decimation by 16 near DC images are so greatly attenuated for interpolation by power of 2 cases that Equations 12 and 13 can be used even for peak input conditions.

Special Case 2 - Overflow Possibilities when the Interpolation Factor is Greater than the HDF Decimation Factor

It is not recommended to use the DDC in a wideband application which requires an interpolation rate greater than the HDF decimation rate unless a loss in dynamic range can be tolerated.

As a general rule a 6dB loss in dynamic range will result for every factor of 2 that the interpolation rate is greater than the decimation rate.

An example of the interpolation factor being greater than the HDF decimation factor is shown in Figure 24. In this example the interpolation factor is 32 and the HDF decimation factor is 16.

As seen in Figure 24 images can lie in the main lobe of the HDF filter curve as well as side lobes. In this case Equations 14 and 15 are still applied with the exception that near DC image components in the HDF main lobe must be included in the Slg calculation. Further, the definition of near DC components is now dependent on the number of image components that can lie in the main lobe and the side lobes. The near DC “width” can be calculated by considering the slope of the HDF response curve in the area of the original spectrum and the total magnitude of the images. Since this is highly dependent on the interpolation rate in the case where the interpolation rate is greater than the HDF decimation rate, it is left to the user to derive.

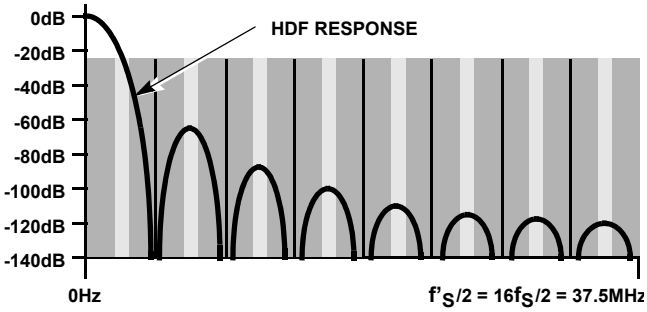

FIGURE 9. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 16 CASE

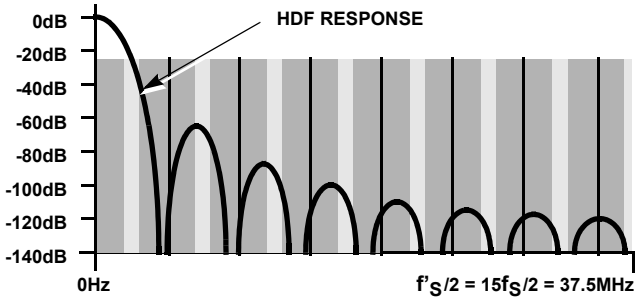

FIGURE 10. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 15 CASE

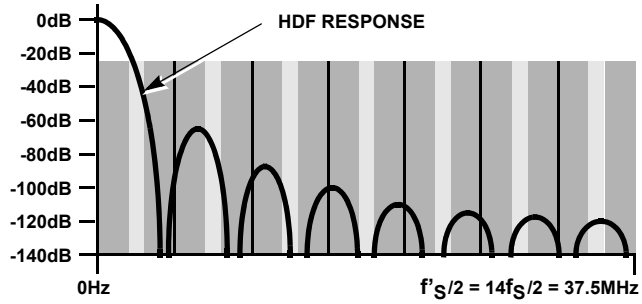

FIGURE 11. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 14 CASE

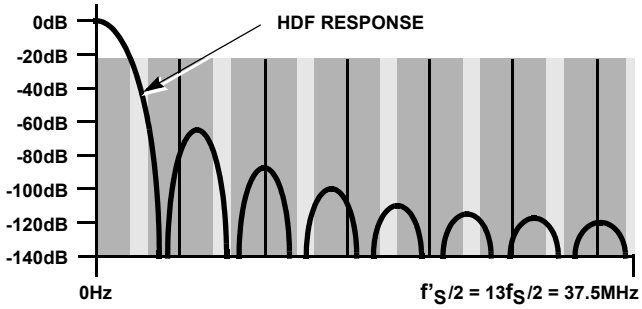

FIGURE 12. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 13 CASE

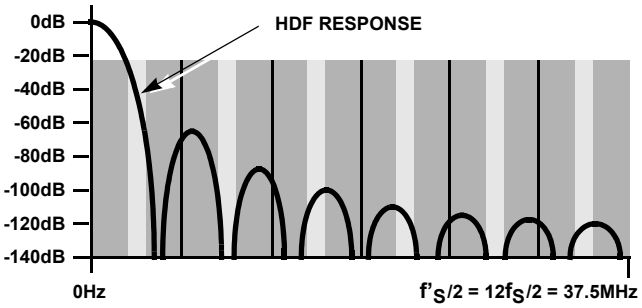

FIGURE 13. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 12 CASE

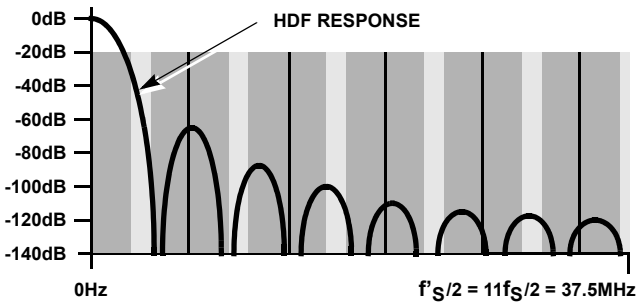

FIGURE 14. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 11 CASE

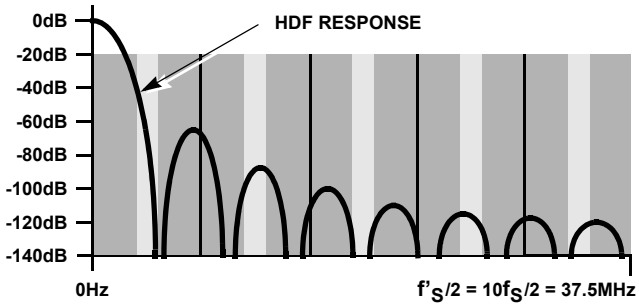

FIGURE 15. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 10 CASE

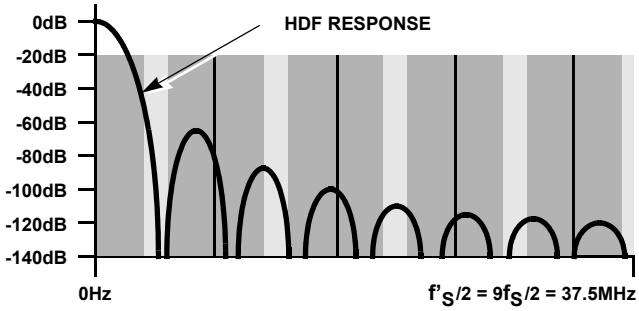

FIGURE 16. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 9 CASE

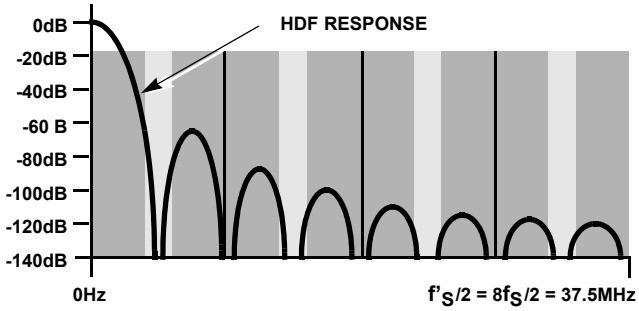

FIGURE 17. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 8 CASE

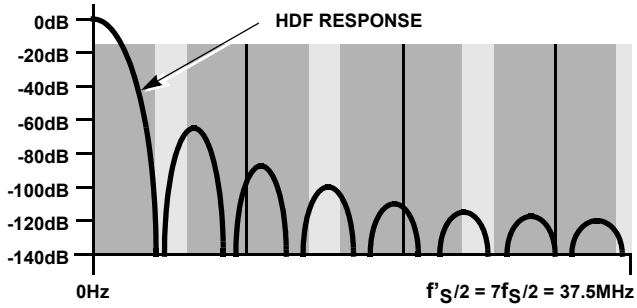

FIGURE 18. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 7 CASE

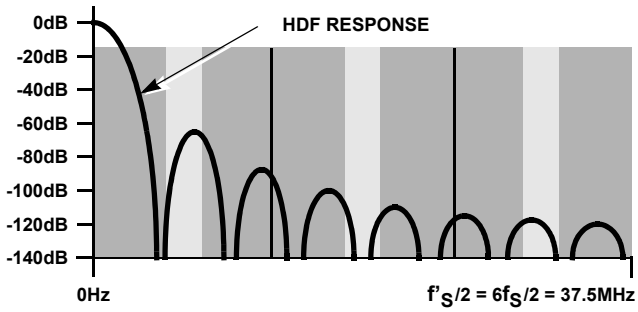

FIGURE 19. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 6 CASE

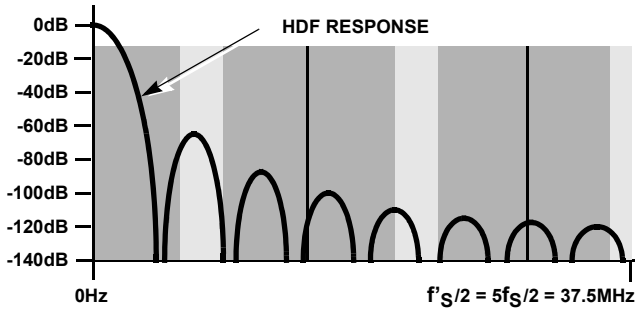

FIGURE 20. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 5 CASE

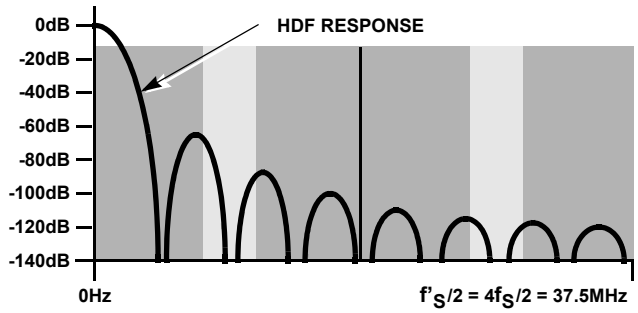

FIGURE 21. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 4 CASE

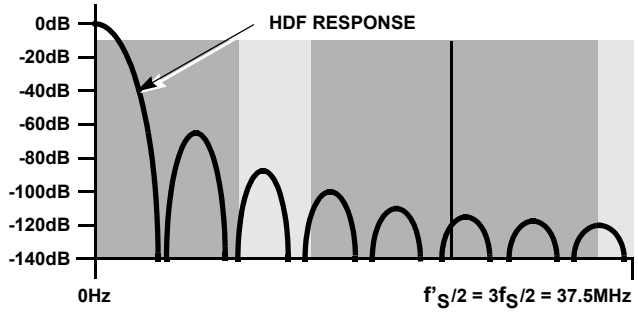

FIGURE 22. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 3 CASE

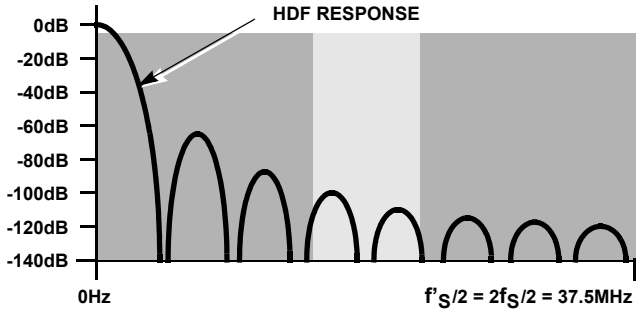

FIGURE 23. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 2 CASE

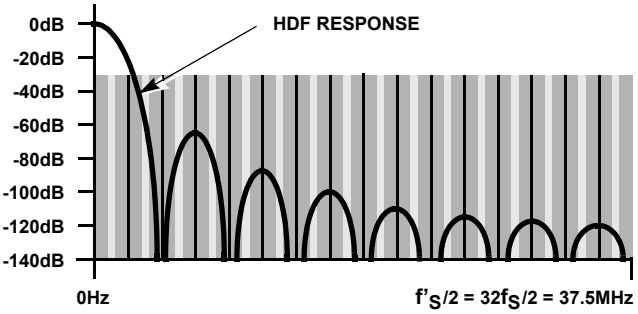

FIGURE 24. REPEATED INPUT SPECTRUM WITH THE HDF RESPONSE CURVE AND NEAR DC IMAGES SUPERIMPOSED FOR THE INTERPOLATE BY 32 CASE

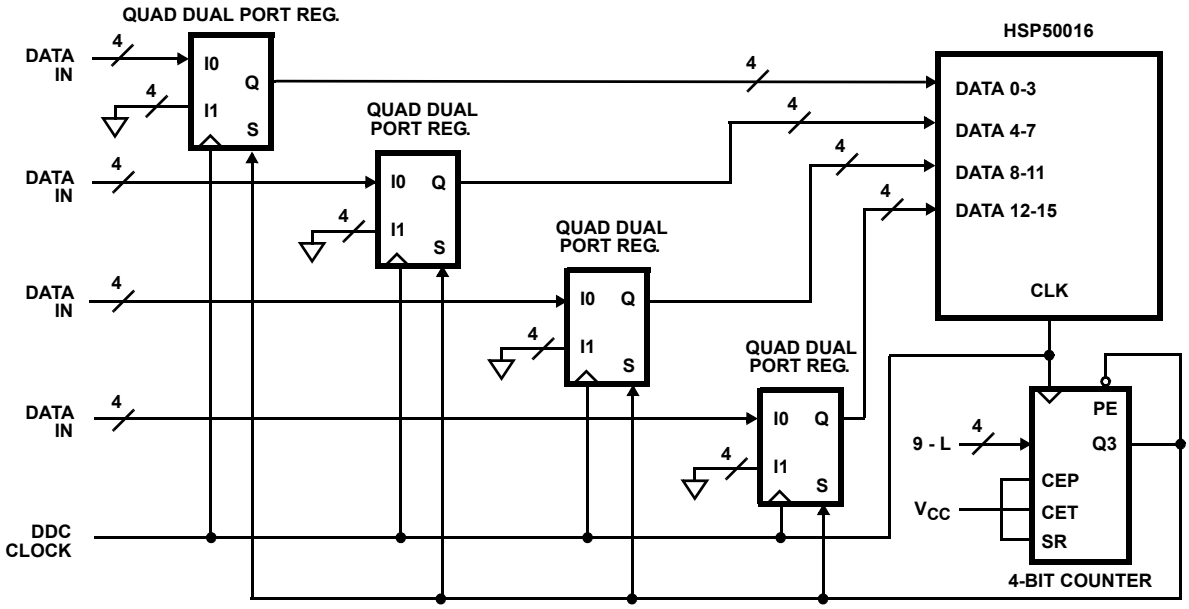

FIGURE 25. AN EXAMPLE SAMPLE RATE EXPANSION CIRCUIT WITH A MAXIMUM EXPANSION OF 8 AND A MAXIMUM CLOCK OF 65MHz

Center Frequency Calculation

Decreasing the minimum decimation factor of the DDC by interpolation impacts the calculation and resolution of the local oscillator control words with the exception of Phase Offset 4.

The Phase Generator in the DDC uses a 33-bit phase accumulator to generate an 18-bit phase word which controls the local oscillator [1]. In continuous Carrier Wave (CW) down convert mode the 32-bit Maximum Phase Increment is used to control the phase step between successive Phase Generator outputs. The Maximum Phase Increment represents phase increments from 0 to $\pi(1\text{-}2^{-32})$ relative to the DDC input sampling rate. When the DDC is proceeded by a sample rate expander the input sample rate is 1/L times the DDC input sample rate. Therefore, the maximum valid phase step relative to the input sample rate is 1/L that of the DDC. **Likewise, the frequency resolution is reduced by L.**

We now illustrate the afore stated points by way of example.

Assume a 4MSPS input and a desired decimation of 4. The DDC would be clocked at 64MHz and would be preceded by a sample rate expander which up samples by a factor of 16. The HDF decimation factor would be set to 16.

The Maximum Phase Increment can be programmed from 0_H to $FFFFFFFF_H$ representing an LO frequency from DC to just under 32MHz. However, the highest input frequency into the sample rate expander is 2MHz which is in turn the highest valid LO frequency. This LO frequency corresponds to a Maximum Phase Increment value of $FFFFFFFF_H/16$ or $FFFFFFF_H$.

If the DDC sampling rate were 4MHz, the frequency resolution would be $4MHz/2^{33}$. Since the DDC sampling rate is 64MHz the frequency resolution is $64MHz/2^{33}$, or 1/Lth that of $4MHz/2^{33}$.

In Chirp mode the Maximum Phase Increment, Minimum Phase Increment, and Delta Phase Increment must also be calculated for the input sample rate relative to the DDC sampling rate.

Example Sample Rate Expander Circuit

Figure 25 shows an example sample rate expander circuit built around a high speed CMOS synchronous counter and four high speed CMOS quad dual port registers.

The synchronous counter is preset with 9 minus L, the desired interpolation rate. The Count Enable Parallel (CEP), Count Enable Trickle (CET), and Synchronous Reset (SR) inputs are tied high. For L-1 counts of the DDC clock the counter's Q3 output line is low and is used to select the grounded I1 inputs into the quad dual port registers. On the Lth count Q3 goes high, initiating two actions. First it selects the input data on the I0 inputs to the quad dual port registers. Second, it presets the counter. The high rate outputs of the quad dual port registers are connected to the DDC's data inputs. This action results in sample rate expansion by L. This circuit can be used for DDC clock factors up to approximately 65MHz and interpolation factors of up to 8. Additional ANDing logic can be attached to the counter outputs to increase the possible interpolation rates to 16. Figure 26 shows a similar circuit using two PAL's.

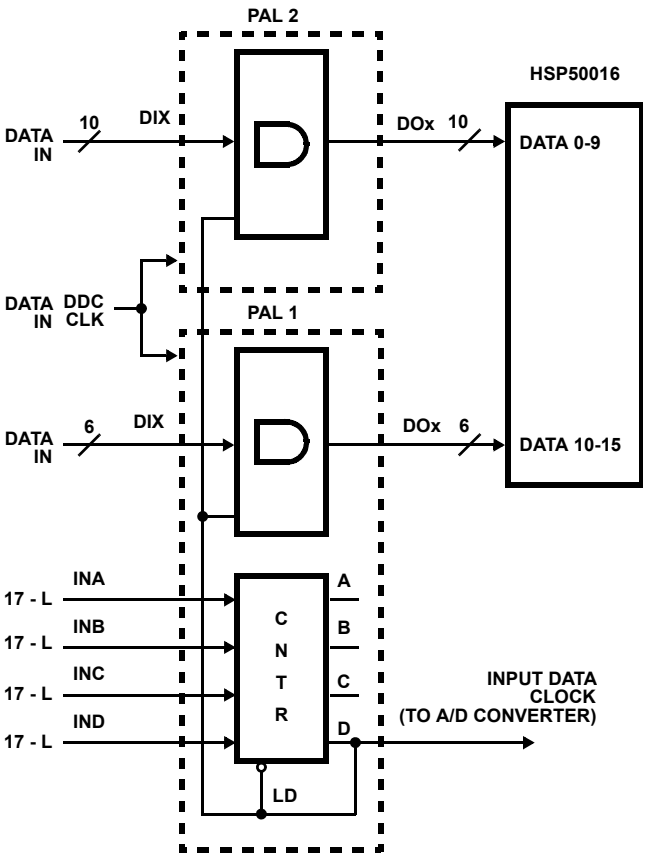

FIGURE 26. AN EXAMPLE SAMPLE RATE EXPANSION CIRCUIT USING TWO PALS WITH A MAXIMUM EXPANSION OF 8 AND A MAXIMUM CLOCK OF 75MHz

The first PAL is configured as a counter and six AND gates with one input of each AND gate tied to a common control line coming from the counter and the other input connected to an input data line. The logical configuration of the first PAL is as follows.

DOx = DIx and $\overline{D}$

A = (D and $\overline{A}$) + ($\overline{D}$ and INA)

B = (D and A and $\overline{B}$) + ($\overline{D}$ and INB) + (D and $\overline{A}$ and B)

C = (D and A and B and $\overline{C}$) + ($\overline{D}$ and INC)

+ (D and $\overline{A \text{ and } B}$ and C)

D = ($\overline{A \text{ and } B \text{ and } C}$ and D) + ($\overline{D}$ and IND)

The other PAL is configured as ten AND gates with one input of each AND gate tied to a common control line coming from the counter via an input line and the other input connected to an input data line. Logically the second PAL is configured as follows:

DOx = DIx and $\overline{D}$

All outputs are registered.

The operation of this circuit begins as the counter is preset with a value of 17 minus L, the interpolation factor L can be up to 8. On successive DDC clocks the counter counts up until it rolls over to zero. Until the roll over occurs D is in a high state and thus $\overline{D}$ is in a low state. Since $\overline{D}$ is in a low state, all data outputs are in a low state. This stuffs zeros between the low rate data input to the PALs.

When the counter rolls over $\overline{D}$ goes high resulting in two actions. First the input data is passed through the AND gates and into the registered outputs to be passed to the DDC. Second, it reloads the counter to begin the count sequence anew.

This action results in sample rate expansion by L. This circuit can be used for DDC clock rates up to the maximum 75MHz and interpolation rates of up to 8. Additional logic can be incorporated in the counter to increase the possible interpolation rates.

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