Recommended Test Procedures for Analog Switches

The following text describes the basic test procedures that can be used for most Intersil CMOS switches. Various test conditions are used with the various switches. Table 1 has been included to help define the specific test setups to be used with each variety of switch. One additional note, all schematics assume an open switch for high logic inputs (i.e., NC).

**DC Switch Parameters**

**+V_S, -V_S: ANALOG SIGNAL RANGE**

The analog signal range is the maximum input signal level which can be switched to the output with minimal distortion. For supply voltages lower than nominal, the analog signal range should be restricted to the voltage span between the supplies. Note that other parameters, such as “ON” resistance and leakage currents, are guaranteed over a smaller input range and tend to degrade toward the analog limits (+V_S and -V_S). Intersil switches can tolerate the positive analog signal limit (+V_S) applied to one side of a switch cell while the negative analog signal limit (-V_S) is applied to the other side (the switch must be open to avoid excessive currents).

The analog signal range is measured (Figure 1) by increasing an input waveform until the output shows evidence of distortion or the maximum analog level is reached (as stated in the maximum ratings section of the data sheet).

**RON: ON RESISTANCE**

“ON” resistance is the effective series on-switch resistance measured from input to output under specified conditions. Note that R_ON typically changes with temperature (highest at high temperature), and to a lesser degree with signal voltage and current. R_ON is calculated from the voltage drop across a switch with a known current flow as in Figure 2.

**I_S(OFF), I_D(OFF), I_D(ON): LEAKAGE CURRENTS**

Intersil prefers to guarantee only worst case high temperature leakage currents because the room temperature picoampere levels are virtually impossible to measure repeatedly on currently available automated test equipment. Even under laboratory conditions, fixture and test equipment leakage currents may frequently exceed the device leakage currents. Since the leakage currents tend to double for every 10°C increase in temperature, it is reasonable to assume that the +25°C value is about 1/1000 the +125°C value; however, in some cases there may be ohmic leakage paths, such as across the package, which would tend to make the +25°C reading slightly higher than expected.

I_S(OFF), measured directly with the circuit in Figure 3, consists largely of the diode leakage current from the source-body junction. I_D(OFF), also measured directly with the circuit in Figure 3, is largely due to the diode leakage current in the drain-body junction.
"ON" leakage current (I_{D(ON)}) is the current flowing through both the source-body and drain-body junctions of a closed switch. I_{D(ON)} tends to have the most noticeable effect since it creates an offset voltage across the switch equal to I_{D(ON)} \times R_{ON}. I_{D(ON)} is measured directly with the circuit in Figure 4.

**Dynamic Switch Parameters**

**t_{ON}, t_{OFF}: ACCESS TIME**

Switch "Turn On" time t_{ON} is the time required to activate an "OFF" switch to an "ON" state. t_{ON} is measured from the 50% point of the logic transition to the 90% point of the output transition (Figure 5).

Switch "Turn Off" time t_{OFF} is the time required to deactivate an "ON" switch to an "OFF" state. t_{OFF} is measured from the 50% point of the logic transition to either the 90% point or 10% point (Figure 5).

**CHARGE INJECTION**

Cycling a switch "ON" or "OFF" results in a small amount of charge being injected into the analog signal path. This charge injection is generated through the capacitive coupling between the digital control lines and the analog outputs. The ensuing voltage spikes create an acquisition interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled onto the analog lines is especially critical when switching voltage to a capacitor since the injection charge will change the capacitor voltage at the instant of switching.

Charge injection, measured in pico-coulombs, is measured with the aid of the circuit in Figure 6.

**OFF ISOLATION**

Off isolation is the degree of attenuation seen at the output of an "Open" switch when a high frequency signal is applied to the input. This feed through occurs through the source-body and drain-body capacitances and has a greater effect at higher frequencies. Off isolation is usually specified in decibels where Off Isolation = 20Log (V_{OUT}/V_{IN}), see Figure 7. The isolation generally decreases by 10dB/decade with increasing frequency.
**CROSSTALK**

Crosstalk is the amount of signal cross coupling from an “OFF” analog input to the output of another “ON” channel output. Crosstalk is usually measured in decibels where: \( \text{Crosstalk} = 20\log\left(\frac{V_{\text{OUT}2}}{V_{\text{IN}1}}\right) \), see Figure 8.

\[
\text{CROSSTALK} = 20\log\left(\frac{V_{\text{OUT}2}}{V_{\text{IN}1}}\right) \text{ dB}
\]

![Figure 8. General Crosstalk Test Circuit](image)

**SETTING TIME**

Setting time is the time required for the switch output to settle within a given percentage of the final value following a change in the digital input level. Usually the worst-case settling time occurs when the switch is required to slew across its full dynamic range (generally a 0V to +10V transition). This is known as full-scale settling time.

The settling time circuit, Figure 10, employs two resistors to generate an error voltage equal to the output error. A FET is used to buffer the summing junction from the oscilloscope probe capacitance.

![Figure 9. Break-Before-Make-Delay Test Circuit and Waveforms](image)

**T(BBM): BREAK-BEFORE-MAKE-DELAY**

The break-before-make-delay \( T_{\text{BBM}} \) is the elapsed time between the “Turn Off” of one switch and the corresponding “Turn On” of another for a common change in logic states (Figure 9). The delay measurement is taken at the 50% levels of the output transitions. The \( T_{\text{BBM}} \) delay prevents the switches from being simultaneously closed during switching transitions.
Switch Logic Parameters

VAL, VAH: INPUT THRESHOLDS
The input thresholds are the digital input upper and lower limits at which proper switching action is guaranteed to take place. The input low threshold VAL is the maximum allowable voltage that can be applied to the digital input and still be recognized as a logic low ("0") input. The input high threshold VAH is the minimum allowable voltage that can be applied to the digital input and still be recognized as a logic high ("1") input. All other parameters will be valid if the logic inputs are either below VAL or above VAH.

IAL, IAH: INPUT LEAKAGE CURRENT
Input leakage current is the bias current flowing either into or out of the digital input terminal. Input leakage current high (IAL) is the current flowing while the digital input is in the high state (≥ VAH), while input leakage current low (IAL) is the current flowing when the digital input is in the low state (< VAL). Input leakage currents are measured directly using the circuits in Figure 11.

SETTLING TIME (Ts) IS MEASURED USING A HIGH SPEED RECOVERY OSCILLOSCOPE TO DISPLAY THE ERROR VOLTAGE VE.
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS
**Static and Package Related Switch Parameters**

**I+, I-, PD: POWER DISSIPATION**

Quiescent power dissipation $P_D = (+V_{CC}*I+) + (-V_{CC}*I-)$ (Figure 12). $P_D$ may be specified with the switch in either a cycling or a steady state condition. Note that, as with all CMOS devices, power dissipation increases with switching frequency.

![Figure 12. Supply Current Test Circuit](image)

$P_D = (+V_{CC}*I+) + (-V_{CC}*I-)$

SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

**C\text{S(OFF)}, C\text{D(OFF)}, C\text{D(ON)}, C\text{DS(OFF)}, C\text{A}: SWITCH CAPACITANCE**

The various switch capacitances are stated as typical values. These values are given by design and are not subject to production testing (Figure 13).

Capacitance Source-Off $C_{S(OFF)}$ is the capacitance with respect to ground seen at the analog input with the switch open. This capacitance is the sum of the source capacitance of the N-channel and P-channel switching devices.

$$C_{S(OFF)} = C_{SGP1} + C_{SBP1} + C_{SGN} + C_{SBN}$$

Capacitance Drain-Off $C_{D(OFF)}$ is the capacitance with respect to ground seen at the output terminal with the switch open. This capacitance is the sum of the drain capacitance of the N-channel and P-channel switching devices.

$$C_{D(OFF)} = C_{DGP1} + C_{DBP1} + C_{DGN} + C_{DBN}$$

Capacitance Drain-On $C_{D(ON)}$ is the capacitance with respect to ground at the drain with the switch closed. Generally $C_{D(ON)}$ is the total of the source-off and drain-off capacitances.

$$C_{D(ON)} = C_{D(OFF)} + C_{S(OFF)}$$

Input to output capacitance $C_{DS(OFF)}$ is the capacitance between the analog input and output with the switch open.

Digital input capacitance $C_A$ is the capacitance with respect to ground at the digital input. $C_A$ chiefly affects propagation delays when the switch is driven by CMOS logic.
**Switch Test Fixture Design Rules**

The high performance characteristics of Intersil switches require high quality test fixtures for accurate characterization. The following design rules should eliminate most sources of error and provide highly accurate results.

- Decoupling capacitors should be placed as close to the supply pins as possible.
- A ground plane should be used to minimize distributed capacitance.
- All grounds should terminate at a single point ground.
- All sensitive analog lines should be routed between ground traces and kept away from digital lines.
- Analog and digital lines should cross at right angles.
- All unused logic pins should be connected to either \( V_{AL} \) or \( V_{AH} \).
- All unused analog pins should be connected to ground through a 1k\( \Omega \) resistor.
- Teflon sockets should be used to minimize socket capacitance.

**FIGURE 13. EQUIVALENT SWITCH CIRCUIT INCLUDING CAPACITANCES**

SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS
# TABLE 1. TEST CONDITIONS FOR “HI” TYPE SWITCHES

<table>
<thead>
<tr>
<th>SWITCH</th>
<th>LOGIC LEVELS</th>
<th>LOGIC REFERENCE</th>
<th>R&lt;sub&gt;ON&lt;/sub&gt;</th>
<th>I&lt;sub&gt;S&lt;/sub&gt;, I&lt;sub&gt;D&lt;/sub&gt;</th>
<th>R&lt;sub&gt;ON&lt;/sub&gt;, I&lt;sub&gt;OFF&lt;/sub&gt;</th>
<th>CHARGE INJECTION</th>
<th>CROSS TALK</th>
<th>OFF ISOLATION</th>
<th>SETTLING TIME</th>
<th>BREAK-BEFORE-MAKE</th>
<th>I&lt;sub&gt;AL&lt;/sub&gt;, I&lt;sub&gt;AH&lt;/sub&gt;</th>
<th>POWER DISSIPATION</th>
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<td>HI-200</td>
<td>V&lt;sub&gt;AL&lt;/sub&gt; = 0.8V V&lt;sub&gt;AH&lt;/sub&gt; = 2.4V</td>
<td>V&lt;sub&gt;REF&lt;/sub&gt; OPEN</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = +10V I&lt;sub&gt;DS&lt;/sub&gt; = 1mA</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = +14V</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = +10V R&lt;sub&gt;L&lt;/sub&gt; = 1kΩ C&lt;sub&gt;L&lt;/sub&gt; = 35pF V&lt;sub&gt;A&lt;/sub&gt; = 0V, 4V</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 3V&lt;sub&gt; RMS&lt;/sub&gt; f = 100kHz R&lt;sub&gt;L&lt;/sub&gt; = 1kΩ C&lt;sub&gt;L&lt;/sub&gt; = 10pF V&lt;sub&gt;A&lt;/sub&gt; = 5V, 0V</td>
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<td>V&lt;sub&gt;AL&lt;/sub&gt; min = 0V V&lt;sub&gt;AH&lt;/sub&gt; max = 5V</td>
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<td>V&lt;sub&gt;IN&lt;/sub&gt; = +14V</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = +10V R&lt;sub&gt;L&lt;/sub&gt; = 1kΩ C&lt;sub&gt;L&lt;/sub&gt; = 35pF</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 3V&lt;sub&gt; RMS&lt;/sub&gt; f = 100kHz R&lt;sub&gt;L&lt;/sub&gt; = 1kΩ C&lt;sub&gt;L&lt;/sub&gt; = 10pF V&lt;sub&gt;A&lt;/sub&gt; = 5V, 0V</td>
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