Introduction

The following text describes the basic test procedures that can be used for most Intersil Op Amps. Note that all measurement conversions have been taken into account in the equations stated.

1. Offset Voltage

The offset voltage (V_{IO}) of the amplifier under test (AUT) is measured via Test Circuit 1 as follows:

1. Set V+ and V- supplies to values specified in Table 1, Column (1) and V_{DC} to 0V.
2. Close S1 and S2, open S3.
4. Measure voltage at E in volts (label as E1).
   \[ V_{IO} = \frac{E_1}{1000} \text{mV} \quad \text{for} \quad R_F = 50K, \text{or} \]
   \[ V_{IO} = \frac{E_1}{10} \text{μV} \quad \text{for} \quad R_F = 5M \]

The gain of this circuit with R_F = 50K (R_F = 5M) requires the output to be driven to 1000 (100,000) times the offset voltage necessary to maintain the output of the AUT at 0V. Note that the AUT output is always identical to V_{DC}. Overall circuit stability is maintained by the adjustable feed-back capacitor C_A.

2. Input Bias Current

The bias current flowing in or out of the positive terminal of the AUT (I_{IB+}) is obtained using Test Circuit 1 by:

1. Measuring E_1 as in procedure 1 (use R_S = 100K for JFET input devices).
2. Maintain V_{DC} at 0V.
3. Close S2, open S1 and S3.
4. Measuring voltage at E in volts (label as E2).
   \[ I_{IB+} = \frac{E_1 - E_2}{100} \text{nA} \quad \text{for} \quad R_F = 50K, \text{or} \]
   \[ I_{IB+} = \frac{E_1 - E_2}{10} \text{nA} \quad \text{for} \quad R_F = 50K \]

The bias current flowing in or out of the negative terminal (I_{IB-}) is found by:

1. Following steps 1 and 2 for I_{IB+}.
2. Close S1, open S2 and S3.
3. Measuring voltage at E in volts (label as E3).
   \[ I_{IB-} = \frac{E_1 - E_3}{100} \text{nA} \quad \text{for} \quad R_F = 50K, \text{or} \]
   \[ I_{IB-} = \frac{E_1 - E_3}{10} \text{nA} \quad \text{for} \quad R_F = 50K \]

3. Input Offset Current

Using Test Circuit 1, the input offset current (I_{IO}) of the AUT is determined by:

1. Measuring E_1 as in procedure 1.
2. Maintaining V_{DC} at 0V.
3. Open S1, S2 and S3.
4. Measuring voltage at E in volts (label as E4).
   \[ I_{IO} = \frac{E_1 - E_4}{100} \text{nA} \quad \text{for} \quad R_F = 50K, R_S = 10K, \text{or} \]
   \[ I_{IO} = \frac{E_1 - E_4}{10} \text{nA} \quad \text{for} \quad R_F = 50K, R_S = 100K \]

4. Power Supply Rejection Ratio

Both positive and negative PSRRs are measured via Test Circuit 1. For PSRR+:

1. Close S1 and S2, open S3.
2. Choose: R_F = 50K
3. Set V_{DC} = 0, V+ = 10V, and V- = -15V.
4. Measure voltage at E in volts (label as E5).
5. Change V+ to +20V.
6. Measure voltage at E in volts (label as E6).
   \[ \text{PSRR}^+ = 20 \log_{10} \left( \frac{10^4}{E_5 - E_6} \right) \text{dB} \quad \text{for} \quad R_F = 50K \]

Similarly for PSRR-:

1. Follow steps 1 and 2 for PSRR+ above.
2. Set V_{DC} = 0V, V+ = +15V, and V- = -10V.
3. Measure voltage at E in volts (label as E7).
4. Change V- to -20V.
5. Measure voltage at E in volts (label as E8).
   \[ \text{PSRR}^- = 20 \log_{10} \left( \frac{10^4}{E_7 - E_8} \right) \text{dB} \quad \text{for} \quad R_F = 50K \]

5. Common Mode Rejection Ratio

The CMRR is determined by adjusting Test Circuit 1 as follows:

1. Close S1 and S2, open S3.
2. Choose: R_F = 50K
3. Set V+ = +5V, V- = -25V, and V_{DC} = -10V.
4. Measure voltage at E in volts (label as E9).
5. Set V+ = 25V, V- = -5V, and V_{DC} = 10V.
   \[ \text{CMRR} = 20 \log_{10} \left( \frac{2 \times 10^4}{E_9 - E_{10}} \right) \text{dB} \quad \text{for} \quad R_F = 50K \]

6. Output Voltage Swing

Test Circuit 2 is adjusted to measure V_{OUT+} and V_{OUT-}, the procedure is:

1. Select appropriate V+ and V- supply values from Table 1, Column 1.
2. Select specified R_L from Table 1, Column 2.
3. Set $V_{IN} = 0.5V$.
4. Measure voltage at $E$ in volts. $V_{OUT}^+ = E \text{ (V)}$
   Similarly $V_{OUT}^-$ is found by:
1. Selecting specified $R_L$ from Table 1, Column 1.
2. Setting $V_{IN} = -0.5V$.
   $V_{OUT}^- = E \text{ (V)}$

7. Output Current
The output current corresponding to the output voltage of procedure 6 is found by:
1. Measuring $V_{OUT}^-$ and $V_{OUT}^+$ as in procedure 6.
   \[ I_{OUT}^+ = \frac{V_{OUT}^+}{R_L} \text{ where } R_L \text{ is from Table 1, Column 2.} \]
   \[ I_{OUT}^- = \frac{V_{OUT}^-}{R_L} \text{ where } R_L \text{ is from Table 1, Column 2.} \]

8. Open Loop Gain
Both positive ($A_{VOL}^+$) and negative ($A_{VOL}^-$) open loop gain measurements are determined by adjusting Test Circuit 1.
For $A_{VOL}^+$:
1. Close $S_1$, $S_2$ and $S_3$.
2. Select specified $R_L$ from Table 1, Column 3.
3. Set $R_F = 50K$.
4. Set $V_{DC} = 0V$, $V^+ = +15V$, and $V^- = -15V$.
5. Measure voltage at $E$ in volts (label as $E_{13}$).
6. Set $V_{DC} = 10V$.
7. Measure voltage at $E$ in volts (label as $E_{14}$).
   \[ A_{VOL}^+ = \frac{10}{E_{14} - E_{13}} \text{ (V/mV) for } R_F = 50K \]
For $A_{VOL}^-$:
1. Follow steps 1, 2, 3, 4, and 5 above.
2. Set $V_{DC} = -10V$.
3. Measure voltage at $E$ in volts (label as $E_{15}$).
   \[ A_{VOL}^- = \frac{10}{E_{13} - E_{15}} \text{ (V/mV) for } R_F = 50K \]

9. Slew Rate
Test Circuit 3 is used for measurement of positive and negative slew rate. For SR+:
1. Select specified $R_L$, $A_{CL}$, and $C_L$ from Table 1, Columns 4, 5 and 6.
2. Apply a positive step voltage to $V_{AC}$ (refer to data book for test waveform).
3. Observe $\Delta V$ and $\Delta t$ at $E$. A standard approach is to use the 10% and 90% points or else the 25% and 75% points on the waveform.

For SR- repeat above procedure with negative input pulse.

\[ SR = \frac{\Delta V}{\Delta t} \]

10. Full Power Bandwidth
Full power bandwidth is calculated by:
1. Measuring slew rate as above in procedure 9.
2. Measuring $V_{OUT}^+$ as in procedure 6. (Typically $V_{OUT}^+$ is assumed to be the guaranteed minimum $V_{OUT}$, usually 10V.)
   \[ \text{FPBW} = \frac{SR^+}{2\pi V_{OUT(PEAK)}} \]

11. Rise Time, Fall Time and Overshoot
The small signal step response of the AUT is determined via Test Circuit 3. The procedure requires:
1. Selecting the appropriate $R_L$, $A_{CL}$, and $C_L$ from Table 1, Columns 4, 5 and 6.
2. Applying a positive input step voltage for rise time $t_R$ and positive overshoot $OS^+$. Applying a negative input step voltage for fall time $t_F$ and negative overshoot $OS^-$. (Refer to data book for input waveforms.)
3. Observe output of AUT noting the key points as shown.
12. Settling Time

Test Circuit 6 is appropriate for settling time (tS) measurement, the procedure is:

1. Select R1 and R2 such that AUT is at the A_{CL} stated in Table 1, Column 5.
2. Select R3 and R4 so that \( R_3 \geq 2R_1 \) and \( R_4 \geq 2R_2 \) with the condition that the ratio
\[
\frac{R_3}{R_4} = \frac{R_1}{R_2} \quad \text{be maintained.}
\]
3. Apply step voltage as specified in data book.
4. Measure the time from \( t_1 \) (time input step applied) to \( t_2 \) (the time \( E_S \) settles to within a specified percentage of \( V_{OUT} \) - see data book). \( t_S = t_2 - t_1 \)

NOTE: Clipping diodes of Test Circuit 6 prevent overdrive of oscilloscope. (Recommend fast Schottky diodes.)

13. Gain Bandwidth Product

Test Circuit 4 is used for measuring GBP. The procedure is:

1. Sweep \( V_{IN} \) thru the required frequency range.
2. With a network analyzer view gain (dB) versus frequency as below.

\[
\text{Gain (dB)}
\]

3. At the voltage gain of interest (A_V) determine the corresponding frequency \( f_C \). Note that chosen A_V must be greater than or equal to that stated in column 5 of Table 1. \( \text{GBP} = A_V \times f_C \) (Hz) where \( A_V \) is in V/V.

14. Phase Margin (Network Analyzer Method)

Test Circuit 4 is used to obtain phase margin measurement. The procedure is:

1. Sweep \( V_{IN} \) thru the required frequency range.
2. Display gain in dB and phase in degrees versus frequency on analyzer as shown.

15. Input Noise Voltage

Test Circuit 5 is designed for measuring input noise voltage. Use of the Quantec Noise Analyzer is recommended to obtain measurements at 1Hz bandwidth around a specific center frequency. The procedure is:

1. Set \( R_G = 0 \)
2. Set circuit card to gain of 10.
3. Select measurement frequency of interest.
4. Record noise voltage (label as \( E_{n1} \)). Units are nV/\( \sqrt{\text{Hz}} \).

16. Input Noise Current

Using Test Circuit 5, the input noise current is obtained by:

1. Measure \( E_{n1} \) as above for the desired frequency of interest.
2. Adjust \( R_G \) so that \( V_O > 2E_{n1} \) (label \( V_O \) as \( E_{n2} \)).

\[
I_n = \frac{(E_{n2})^2 - (E_{n1})^2 - 4kT}{R_G^2} \text{ mV/Hz}
\]

Where \( K = 1.38 \times 10^{-23} \) (Boltzmann’s Constant)
\( T = 300^\circ C (27^\circ C) \)

17. Channel Separation (Crosstalk)

Test Circuit 7 is used to measure channel separation (CS). The procedure is as follows:

1. Apply \( V_{IN} \) at the frequency of interest to input of channel 1.
2. Select \( R_L \) from Table 1, column 4.
3. Measure \( V_{O1} \).
4. Measure \( V_{O2} \) of channel 2.

\[
\text{CS} = 20 \log_{10} \left| \frac{V_{O2}}{100V_{O1}} \right| \text{ dB}
\]
<table>
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<th>PART NUMBER</th>
<th>SUPPLY VOLTAGE (V_{S})</th>
<th>PARAMETERS TO MEASURE</th>
<th>SLEW RATE, OS, t_R, t_F</th>
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<td>(1)</td>
<td>(2) ( V_{OUT} ) ( R_L (k\Omega) )</td>
<td>(3) ( A_{VOL} ) ( R_L (k\Omega) )</td>
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TEST CIRCUIT 1

TEST CIRCUIT 2

TEST CIRCUIT 3

ACL = 1 + \frac{R_F}{R_I}
R_{L(EFF)} = (R_F + R_I)||R_L

TEST CIRCUIT 4

TEST CIRCUIT 5
Test Circuits (Continued)

**TEST CIRCUIT 6**

**TEST CIRCUIT 7**

**CHANNEL 1** (INPUT CHANNEL)

**CHANNEL 2** (LEAKAGE CHANNEL)
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