1 Introduction

Designing Zilker Labs controllers into a system requires four tasks:

1. Design the power architecture, or power conversion stage, by selecting the frequency and major power components. This is an iterative design process that you use to make the trade-offs that define the power characteristics of the part implementation.
2. Develop the basic pin-strapping and stored configuration for the Zilker Labs device that meets your power requirements, including input and output voltage, delay and ramp settings, maximum output current, and a global fault response.
3. Create the PCB layout for the power components. You should use CAD layout software and be aware of several sensitive connections.
4. Implement any additional advanced stored configuration features that you want for your system, including power sequencing, tracking, margining, and advanced fault and thermal management.

This guide provides a task-based approach to designing with the ZL2006, using an actual design, the ZL2006EV1 evaluation board.The ZL2006EV1 board is intended to meet the following objectives:

- V_{IN} = 12 V
- V_{OUT} = 1.2 V / 15 A (20 A max)
- f_{sw} = 615 kHz
- Efficiency: 90% at 50% load
- Output ripple: ±1%
- Dynamic response: ±3%
- Board temperature: 25°C

The complete EVB information can be found in the *ZL2006 Evaluation Board Data Sheet*. Additional example design configurations are shown in the appendix of this document.

2 Designing the Power Architecture

Designing the power architecture involves making decisions on trade-offs between competing design goals: size, cost, efficiency, and transient load performance.

Before you begin a new design, you must determine what the primary design consideration should be to enable the trade-off decisions you will need to make.

For example, if cost is the primary consideration, you will want to use inexpensive parts, which may have a larger footprint, and optimize your output for the smallest ripple current you can achieve.

For this sample design, we chose to optimize transient performance. Our primary goal was to achieve a transient response of plus or minus 3% for up to a 50% load step in a constrained footprint. So we designed to meet that goal, while providing as much efficiency and economy as possible as our secondary goals.

Setting an efficiency goal provides us with a power loss budget. For example, if we want 90% efficiency, we can calculate what the 10% loss would be (our power loss budget) and design the sum of the power loss for all components to be no greater than that budget amount.

2.1 Overview of Key Design Factors

Power design is affected by a number of key factors you should consider, which are often interrelated. The following table lists a number of those factors, what they affect, and what they are affected by.

Table 1. Key Design Factors

Design Element:	Affects:	Affected By:
input ripple current	noise, input capacitor	previous converter
inductor value	transient slew rate, output ripple voltage, circuit footprint	transient deviation budget, input and output voltage, switching frequency
high-side MOSFET	efficiency, circuit footprint	switching frequency, input and output voltages
low side MOSFET	efficiency, circuit footprint	input and output voltages
output ripple current	transient response, output ripple voltage, efficiency	inductor value, input and output voltages
inductor DCR	efficiency, current sensing accuracy, inductor temperature	temperature
output capacitor value	transient response, output ripple voltage, circuit footprint, compensation	output ripple current
output capacitor ESR	output ripple voltage, transient response, compensation	temperature, choice of capacitor type
dead time	efficiency	MOSFETs, output current

Figure 1 provides an example of the transient response envelope and defines key measurements for voltage regulation.

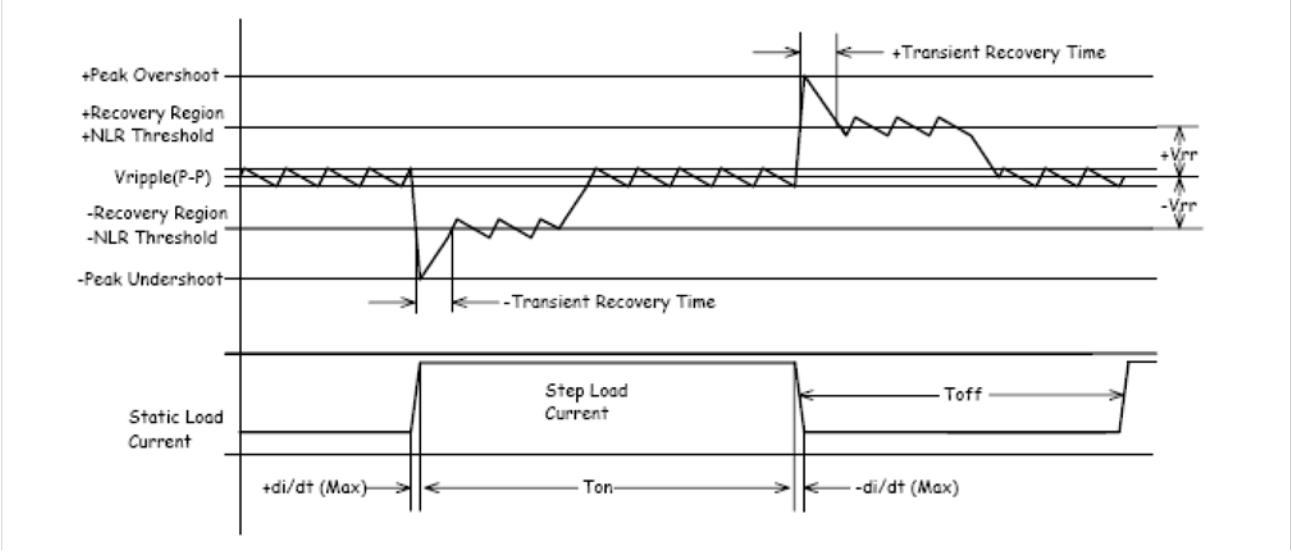


Figure 1. Transient Envelope Definition

Keeping these key factors and our primary design goals in mind, we can begin an iterative design process. Since we want to meet the power requirements of the downstream devices, we start with the power output characteristics, and then select the bias strategy.

2.2 Define the Power Characteristics Goals

To design the power stage, you will need to identify these electrical characteristics:

- Transient tolerance -- As our primary goal, we want the example design to achieve a transient response of less than 3% for a 50% load step at a slew rate of 2.5 A/µs.
- Ripple voltage -- In our example design, we are setting a goal of output ripple voltage variation of plus or minus 1%.
- Regulation voltage -- The regulation voltage will be 1.2V at 15 A (20 A transient) drawn from a source of 12V. The 1.2V at 15 A is a common voltage requirement for high-density logic devices. We also want to allow for a 5V input voltage.
- Characteristic load -- This is defined as the range of the load capacitance. If the regulator is going to be on a fixed board, with set supported components, then the load will not change. If the power board assembly will be used to support multiple board configurations, then you need to design based on the range of load capacitance you are expecting.

These numbers will provide a means of evaluating your design decisions as your design evolves.

2.3 Design the Power Stage

Because of the number of trade-offs possible with each design decision, you should first create a ballpark, or straw man design, that helps you identify the critical factors in your design. Then, through an iterative design process, you can fine-tune the design, making the calculations you need to fully model your design. See the appendices for a variety of sample power stage designs.

To define the power characteristics, we want to:

1. Select a switching frequency.
2. Select the major output components.
   - — Output capacitors
   - — Inductors
   - — MOSFETs
3. Calculate power loss budget
4. Calculate bias losses.
5. Repeat the process to fine-tune design characteristics.

2.4 Select a Switching Frequency

The selection of the switching frequency affects efficiency and performance. Lower switching frequencies are more efficient, reducing switching loss, and higher frequencies provide better performance, with faster transient response.

The following table illustrates the effect of switching frequency on efficiency, circuit size, and transient response.

Table 2. Switching Frequency Design Considerations

Frequency Range	Efficiency	Circuit Size	Transient Response
200-400 kHz	High	Large	Low
400-800 kHz	Moderate	Small	High
800 kHz - 1.4 MHz	Low	Smallest	Best

Another factor to consider is whether or not your switching frequency needs to synchronize with another frequency. Is there a need for the power switching frequency to synchronize with an external source, such as with devices that broadcast on certain frequencies? If so, the design should be planned to support the given frequency and synchronization requirement, which affects component selection and overall performance capabilities of the power design.

For this design, we picked a switching frequency of 615 kHz, higher than the more common 300-400 kHz range, to increase the transient response performance, since our primary design goal is transient response.

Design Step: For your design, select an initial target switching frequency to use as you begin your component selection process. As you determine the results of that process, you may choose to increase or decrease your switching frequency, to better meet your design goals.

2.5 Select the Major Power Components

The selection of the major output components define the output characteristics. By understanding the relationships between the components, you can make the selections to fine-tune the output characteristics, such as output voltage, ripple current, transient response, and power loss.

Output Capacitors

Selecting output capacitors involves a trade-off between low equivalent series resistance (ESR) and capacitance.

A low ESR value is desirable for both small deviations during transient load steps and low output ripple. However, capacitors with low ESR typically have low capacitance values, which don't handle high ripple currents or high transient load steps.

You will need to calculate the approximate capacitance and the ESR of the component. The formulas are available in the AN2011 Component Selection Application Note.

Design Step: As a starting point for your output capacitor selection, apportion half the output ripple voltage to the capacitor ESR and half to the capacitance rating. You have the option of choosing a capacitor with low ESR and high capacitance, or a parallel combination of capacitors with higher ESR that provide the necessary capacitance.

Inductors

Choosing inductors involve several important factors and trade-offs that include the following issues:

- Resulting ripple current
- Transient load slew rate
- Saturation characteristics
- Total power dissipation

Higher inductance that generates a low ripple current allows smaller capacitance to be used on the output. However, a balance needs to be made between the higher inductance values and transient load performance that is improved with higher ripple currents. By understanding the design's expected load transient step magnitude, you can calculate the optimum ripple current, and inductor average and peak current ratings.

You should calculate the load requirements of your downstream powered components. This should include the transient load slew rate you will need to provide. For converters, such as this sample design, that are aimed at the best transient performance, this value determines the inductor value.

Calculating Inductor Requirements: Transient Slew Rate. Our primary constraint on the inductor value is the current slew rate. The inductor current slew rate must approximate the load step slew rate, in order to maintain good regulation during the transient with minimal capacitance. If the load slew rate exceeds the inductor slew rate, then the voltage may vary.

Knowing the design load slew rate, 2.5 A/µs, we can calculate the necessary inductor slew rate to match. We can calculate the inductance for rising current transients by dividing the voltage difference by the slew rate, using the formula:

$$L \cong \frac{V_{in} - V_{out}}{slewrate}$$

Similarly, for falling current transients, we use the formula:

$$L \cong \frac{V_{out}}{slewrate}$$

For this design, with the high ratio between the input and output voltage, we will need to use the lower inductance value to meet the falling current transient performance goal. Using our design voltages and load slew rate, the results for rising transient the inductance equals 4.32 µH, and for the falling it comes out to 480nH. To meet the transients on both edges, we will take the smaller value. So, for this design, we have initially chosen an inductor of 360nH.

As you can see, for designs where the difference between input and output voltage is less, the difference between the two calculations is also less.

Calculating the Ripple Current Requirement. Using the previously calculated inductor value, we can now calculate the ripple current (I_{opp}), using the maximum input voltage (V_{inmax}), the output voltage (V_{out}), the switching frequency (f_{sw}), and our calculated output inductance (L_{out}) in the following formula:

$$I_{opp} = \frac{V_{out} \times \left(1 - \frac{V_{out}}{V_{inmax}}\right)}{fsw \times L_{out}}$$

Now we can check the calculated ripple current to see how it compares to the load current. Typically, for an efficient design, the ripple current should equal 20-50% of the load current.

For this design, we use a ripple current (I_{opp}) of 4.9 A. This value is 24.4% of our rated load current of 20 A.

The average inductor current is equal to the maximum output current. The peak inductor current is equal to the maximum output current plus half of the ripple current, about 22.5 A for this design.

Thus, we select an inductor rated for the average DC current with a peak current rating above the peak current rating computed previously. The peak current rating of the selected inductor is more than 30 A.

Saturation characteristics. Over-current or short-circuit handling capabilities are affected by the inductor performance. How well the inductor performs at up to 2X the normal maximum rated output current determines the protection it can provide for the load and the power supply MOSFETs. Inductors that have poor saturation characteristics, that rapidly drop in inductance as current increases, such as gapped ferrite inductors, should be avoided.

Total power dissipation. To understand the power dissipation of the inductor, use the manufacturer's data sheet DCR winding loss to determine the total power dissipation. Use the formula:

$$P_{cu} = (I_{out})^2 \times DCR$$

For our sample design, the inductor we chose has a DCR of 1.1 mΩ, which, for a continuous current of 15 amps, yields a power loss of 248 mW. We'll use this value when we calculate our power loss budget.

Design Step: Choose the smallest inductor value that can support load and unload transients and the ripple current approximation of 20-50% of the load current, and that also meets the average DC current and peak current ratings.

MOSFETs

You should evaluate MOSFETs on their efficiency: channel loss, switching loss and gate drive current loss. Both gate drive current loss and switching loss are greater at higher frequencies, so lower frequencies mean higher efficiency. Also, note that the channel loss is temperature dependent, so that at higher temperatures, the loss is greater.

In addition, MOSFETs with lower channel loss typically have higher gate charge requirements, which increase the gate drive loss, related to switching frequency.

We will make our selection of MOSFETs based on load current and ripple current ballpark calculations. For our sample design, the duty ratio for the high and low side should be approximately 10 to 1, with the high side on 10% of the time and the low side on 90% of the time.

Selecting the QL MOSFET. Synchronous or QL MOSFETs for this case should be chosen on the basis of the channel resistance and gate drive current. The duty cycle, calculated as V_{out} divided by the V_{in}, (V_{out}/V_{in}), affects the current calculations for the MOSFETs.

Calculate the RMS current, channel loss, and gate drive current based on data sheet values for the candidate MOSFETs. MOSFETs with lower channel loss tend to have higher drive currents. Allow 2-5% of the rated output power for channel loss in QL, calculated using the following equation:

$$P_{QL} = 0.05 \times V_{out} \times I_{out}$$

For the sample design, P_{QL} is less than 0.9 W.

Calculate the RMS current using the duty cycle percentage in QL as follows:

$$I_{QL} = I_{out} \times \sqrt{1 - D}$$

The I_{QL} is 14.23 A for our sample design.

Calculate the desired maximum $R_{DS(ON)}$ as follows:

$$R_{DS(ON))} = \frac{P_{QL}}{(I_{QL})^2}$$

Using our calculated values, we get 4.44 mΩs for the channel resistance.

Note that the $R_{DS(ON)}$ provided in the manufacturer's data sheet is measured at 25°C. Since the loss is temperature dependent, your application $R_{DS(ON)}$ will be much higher. In a typical example, with a junction temperature of 125°C, the $R_{DS(ON)}$ is 1.4X higher than the value at 25°C.

Therefore, we can take the calculated RDS and divide it by 1.4 as a basis for comparison with data sheet MOSFET RDS values to get a value of 3.2 mΩs. We will select a candidate QL MOSFET based on the data sheet RDS matching our desired RDS. We picked a MOSFET with an RDS of 3.5 mΩs, which is conservative for a design that is not expected to run at 125°C.

Once you have selected a candidate QL MOSFET, calculate the required gate drive current as follows:

$$I_g = f_{sw} \times Q_q$$

The requirement for our design using the ZL2006, using the internal drivers, is that the gate drive current for both QH and QL is 80mA or less. If the gate drive current for our candidate MOSFET is too high, we will need to select another part. The calculated gate drive current for our sample design is 12.3 mA.

Since the gate drive circuits are integrated in the ZL2006, you can calculate the power to turn the MOSFETs on and off with the formula:

$$P_{QLdr} = f_{sw} \times Q_g \times V_{inmax}$$

For initial calculations, the gate drive power loss for the QL should not exceed 1 or 2% of the total output power. Our sample design uses 0.6% of load power for gate drive.

Note that the candidate we have chosen works acceptably well if our input voltage is 5V instead of 12V.

Selecting a QH MOSFET. Control or QH MOSFETs have switching loss, in addition to channel and gate-drive current loss. When selecting a QH MOSFET, calculate the channel loss and switching loss to determine the total power dissipated by the QH.

To select a QH, use the same formulas you used for QL to determine channel and gate-drive current loss, with the exception of the RMS, in which the current is calculated using the duty cycle percentage in QH as follows:

$$I_{QH} = I_{out} \times \sqrt{D}$$

For our design, the desired channel loss is 0.9 W, channel resistance is 29 mΩs, the RMS current (I_{QH}) turns out to be 4.74 A.

Using these results, first, we find a MOSFET that meets our channel resistance specification, on or below the 29 mΩ value. Second, we make sure the candidate supports the RMS current value. Finally, we want the channel loss to be 0.9 W or less, and to be sure that the candidate package can dissipate the maximum power dissipated.

One of our design goals is to support a 5V input as well as the 12V input voltage. Recalculating for this case, the target RDS value is about 11 mΩs.

To meet the requirement that we support 5 and 12V input, we pick a MOSFET that is 9 mΩs.

Based on our selection, we can now calculate the switching loss.

First, calculate the switching time (t_{sw}) with the formula that uses the QH gate charge (Q_g) and the peak gate drive (I_{gmax}) available from the ZL2006:

$$t_{sw} = \frac{Q_g}{I_{gmax}}$$

Although the ZL2006 has a typical gate drive current of 3 A, we'll use the minimum guaranteed value of 2 A for a conservative design. The gate charge is 8 nC, resulting in a switching time of 4ns.

Using the calculated switching time, you can now calculate the switching loss with the formula:

$$P_{QHsw} = V_{inmax} \times t_{sw} \times I_{out} \times f_{sw}$$

For our sample design, this results in a switching loss of 2.46% of P_{out}.

The total power dissipated by QH is:

$$P_{QHtot} = P_{QH} + P_{QHsw}$$

P_{QH} is 22.5 mW, and the switching loss is 443 mW, for a total of 465.5 mW, which is 2.6% of the P_{out}.

Efficiency Goals. The MOSFET conduction and switching loss in your design should be 50% or less of your target loss budget for each MOSFET. Based on our calculations, the MOSFETs chosen support the efficiency goals. Note that these numbers are at the continuous current rating. At lower current ratings, the efficiency should be even higher.

Package Selection. Using the calculated power dissipation numbers, you can calculate the junction temperatures, to check the thermal characteristics of the MOSFET.

The package you select must be able to dissipate the generated heat. You should budget the size according to the heat dissipation requirement.

Design Step: Choose your MOSFETs based on channel loss, gate drive loss and switching loss, calculated using the load current and ripple current for the design. Your chosen components should meet both your efficiency and heat dissipation goals.

2.6 Calculate the Power Loss Budget

The power loss budget needs to be measured using two calculations:

- Determine the sum of the power loss for the capacitors, inductors, and MOSFETs in your design. These include:
  - QL channel loss
  - QH channel loss
  - QH switching loss
  - Total gate drive loss
  - Inductor DCR loss
- Determine bias losses. To calculate the bias losses, you will need to select a bias strategy for the ZL2006. You can use the ZL2006 internal regulators, or an external rail to provide power for the ZL2006. The sample design uses the internal regulators. Bias loss includes:
  - High drive QL (I_{gl})
  - High drive QH (I_{gh})
  - Controller I_{dd}, available from the data sheet, is 8-12 mA.

Calculating Bias Loss

Calculate the QL and QH high drive losses.Since the gate drive circuits are integrated in the ZL2006, you can calculate the power to turn the MOSFETs on and off with the formula:

$$P_{dr} = f_{sw} \times (Q_{GH} + Q_{GL}) \times V_{inmax}$$

For initial calculations, the gate drive power loss for the QL and QH should not exceed 1 or 2% each of the total output power. Our sample design uses 1.1% of load power.

Total Power Loss

The total power loss of our design is:

Table 3. Total Power Loss

Item	Loss
Inductor	248 mW
QL RDS	900 mW
QH RDS	465.5 mW
Q gate drive	207 mW
I_{dd}	144 mW
Total	1.964 W

These numbers define a power loss of 10.9% of load power, which is approximately 10% of our input power.

If the sum of all of the bias loss and component loss exceeds your power budget, you will need to adjust your design.

Design Step: Are you over or under your loss budget? If you are over budget, you may need to rethink the DCR of your inductor, and the MOSFET selection. You may need to increase size.

2.7 Run the Numbers and Revise the Design

Once you have completed a ballpark design, you have the information you need to calculate all of the electrical

characteristics of the power stage, to determine how effectively the design is at meeting your goals.

At this point you can fine-tune your design by changing single elements and recalculating the resulting performance.

2.8 Selecting Input Capacitors

Even when using a heavily filtered 5 or 12 volt computer-grade power supply, input capacitors are highly recommended. Using dedicated input capacitors reduces the DC converter's high RMS ripple current, which couples noise into the system circuitry, and, potentially creates excessive heat for filter capacitors not rated for high ripple currents. The input capacitors should be rated at 1.2X the RMS ripple current.

To calculate the RMS ripple current, use the formula:

$$I_{RMS} = I_{out} \times \sqrt{D \times (1 - D)}$$

The amount of capacitance is determined by the target input ripple voltage, which is usually kept below 10% of the DC value of the voltage. You can use the formula:

$$C \approx \frac{I_{out} \times D(V_{inmin}) \times t_{sw}}{10\% \times V_{inmin}}$$

For this design, with the 5V case, the formula gives us a capacitance of 11.7 µF that is easily achieved.

Design Step: We recommend you choose ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage.

3 Develop the Basic Configuration

The ZL2006 is configurable through pin strapping and software. You will need to determine a configuration strategy for your design. Your options include:

- Pin strap only. No software configuration is used.
- Preload a software configuration in the ZL2006 before manufacture.
- On-board stored configuration loading at start-up time.

3.1 Required Pin Straps

No matter which option you choose, you will need to configure a minimum number of pin-strap features. With the exception of the SMBus address and maximum voltage, the values for these pinstrap settings can be overridden using a software stored configuration. These pins include:

- SMBus Address -- Configuration of the SMBus address is only necessary if you are planning to communicate with the part for configuration, monitoring, or using advanced features with other controllers. You can configure the SMBus address in one of three ways: through pinstrapping of SA0 and SA1, or using one resistor connected to SA0, or two resistors connected to SA0 and SA1. We selected two resistors to allow five addresses to be used in the range 0x20 to 0x24. We allowed multiple addresses to allow flexibility in communicating with other parts on the same bus. See section 6.9 of the ZL2006 data sheet for the table of available addresses and resistor values.
- Maximum voltage out -- You can select one of three modes for setting your maximum output voltage: POLA, DOSA, and Standard modes. You select the mode through V0 and V1. We selected standard mode, since our design was not part of a module. You can select a set of standard voltages using pin-strapping only on V0 and V1, or set the voltages by using a resistor on each. We used the two-resistor method to set a nominal of 3.3 V, with a maximum of 10% greater than the set value. This sets a hard upper limit that cannot be violated even if software configuration settings are incorrectly set too high. See section 5.3 of the ZL2006 data sheet for more information on these resistor settings.
- Configuration pin -- This pin can be used for several purposes. The configuration pin determines how the

sync pin operates: as an input, or as an output. The input can look for a fixed external signal to synchronize with, or it can use a resistor value to determine an internal frequency of operation. When configured as an output, the pin outputs a standard 400 kHz, and the part operates at the same frequency. For our sample design, we left the configuration and sync pins open, for the default frequency of 400 kHz as a safe start-up configuration, making the sync pin an input, and set our 615 kHz switching frequency as a stored configuration. For information on setting the configuration and sync pins, see section 5.7 of the ZL2006 data sheet.

- Sync pin -- Provides the hardware setting for the switching frequency for the part, based on the settings of the configuration pin.
- Bootstrap pin -- Connect the bootstrap capacitor as shown in the reference circuit in the ZL2006 data sheet, and determine the capacitor value using the method defined in section 5.8.5.
- Communication busses -- The SMBus and DDC busses must both have pull-up resistors.
- Initial compensation setting -- FC0, FC1 should be set to a safe default compensation until a specific compensation configuration setting is loaded. See sections 5.10-5.11 of the ZL2006 data sheet for information on setting these values. For our sample design, we left these open, to select our default compensation settings.

Design Step: Make sure your pin-strap configuration is a safe configuration that will not start potentially damaging operation before the part configuration is loaded.

3.2 Base Configuration Settings

Once the minimum required pinstrapping configuration has been developed, we can start to define the stored configuration values we want to use.

Here is the set of base settings you need to configure for the ZL2006 to operate.

These settings can be made using the Zilker Labs Power Navigator software. See Appendix A for the screen shots that display the settings we defined for our sample design.

These settings include:

- Output voltage thresholds. Once you select the output voltage, the software calculates recommended over and under voltage protection thresholds. For our design, we accepted those default values.
- Input voltage thresholds. Once you select the input voltage, the software calculates recommended over and under voltage protection thresholds. For our design, we accepted those default values.
- Max output current characteristics. Output current protection thresholds and scaling factors must be set. Entering an output current populates the protection thresholds. For our sample design we chose to override those values. We decreased the average limit to 16 A, and reverse current limits are decreased to -16 and -10 A. We used our inductor DCR value for the current sensing scale.
- Delay and ramp timing characteristics
- Switching frequency. Although we set our pinstrap frequency to be 400 kHz, we want to use a value of 615 kHz for operation.
- Global fault response characteristics. Based on the PMBus specification for standard fault responses, our choices are:
  - Shutdown immediately
  - Shutdown after a specified delay
  - Shutdown and retry with a specified number of attempts and delay time.

We chose the shutdown and retry with maximum delay and infinite attempts for our sample design.

- Current sensing configuration. You have two choices for current sensing, using the inductor or the MOSFET. The inductor is more accurate, but limited to a maximum of 4 V output. The MOSFET current sensing is less expensive, and less accurate, but supports higher output voltages. We chose inductor DCR output sensing for higher accuracy.
- Deadtime configuration. You will need to define the initial dead time to ensure that QH and QL are not both active at the same time. The ZL2006 features an algorithm that dynamically adjusts dead time during operation. The following suggested values for the ZL2006 dead time settings should provide a safe and efficient dead time setting for most common designs. For the ZL2006, use a DEADTIME

value of 0x3838, and a DEADTIME_CONFIG value of 0x0808.

Other basic settings you may want, although they are not required, include:

- Synchronization and Interleave settings -- This is important if you are using multiple controllers, and you want to optimize their power usage.
- Temperature sensing characteristics -- These default to wide values for fault limits and warning thresholds. We used the default values for our design. Note that you can use the internal or external temperature sensing. We chose to use external temperature sensing, with a sensor placed near the inductor, for accurate temperature compensation for the current sensing.

4 Create the PCB Layout

The first step in your PCB layout process should be to examine a Zilker Labs example layout or previous design. The EVB data sheet provides PCB layout information. To ensure a successful layout, use CAD tools for routing the sensitive traces. There are some critical connections in a power converter design. These are explained in the Zilker Labs Layout Design Application Note AN2010.

To create your PCB layout, you should:

- Consult Zilker Labs documentation.
- Verify that the schematic design is implemented properly in the layout.
- Verify the thermal design characteristics of the layout.

4.1 Verify the Schematic Design Implementation

Verify that the key schematic design decisions are implemented properly in the layout:

- Pin straps
- SMBus configuration
- DDC bus configuration
- Switching clock configuration
- Regulator pin decoupling
- Input and output capacitance
- FET and inductor selection
- Enable configuration and operation.
- Sensitive traces routing and polarity for Faraday shielding and Kelvins
- Output filter does not introduce parasitic inductance.
- Verify that there are an adequate number of vias for current carrying and plane interconnects.

4.2 Verify the Design's Thermal Characteristics

- Verify that the design has adequate heat sinking for controller and drivers
- Verify adequate heat sinking for FETs and inductor
- Estimate thermal connection between current sensing element and temperature sensing element.
- Does the unit need to run with no forced air? You will need additional heat sinking if this is your situation.

5 Implement Advanced Configuration Features

The ZL2006 supports a number of advanced features that can be configured for your design. These features are documented in the Zilker Labs Application Notes, and include:

- ***Power Sequencing*** -- The ZL2006 supports event-based power sequencing among multiple controllers. This is accomplished by defining the DDC ID for each controller, and defining a prequel and sequel ID for each controller to define the sequence of powering up and down. This is useful for powering up or down different power rails in a specific order. These options are in the Group page of the PowerNavigator software, or in the DDC Advanced tab.
- ***Voltage Tracking*** -- The ZL2006 can be configured to track another output voltage connected to the VTRK pin. With this feature the tracking can be at 100% or 50% ratio, and can track continuously or can track up to a a target voltage setting maximum. These settings are available on the PowerNavigator Advanced tab.
- ***Non-linear Response loop*** -- For faster transient load step response. Most controllers respond in a linear fashion to transient load steps. The NLR feature allows you to define other response characteristics for limiting transient deviations. You can define triggers for more rapid adjustments to step load transients. These functions are defined in the NLR_CONFIG values on the PowerNavigator Advanced tab.
- ***Current Sharing*** -- The current sharing feature allows you to construct multiphase converter arrays

for higher current or higher transient capabilities. This function uses the ISHARE_CONFIG and VOUT_DROOP commands. Individual phases can be added or dropped from the array using the PHASE_CONTROL command. These commands are on the Basic and DDC Advanced tabs of PowerNavigator.

- ***Fault Spreading*** -- For designs with multiple controllers, this mode allows you to power down a set or all of the controllers if there is a fault with a single controller. This is set up using the DDC_GROUP on the DDC Advanced tab.
- ***Advanced Operating Modes***:
  - Frequency adaptation -- Using this mode, if the controller is experiencing small load currents, the operating frequency can be dynamically reduced to increase efficiency. Set this in the MISC_CONFIG on the DDC Advanced tab.
  - Diode emulation -- This mode improves efficiency at light load conditions. It is also set by the MISC_CONFIG on the DDC Advanced tab.
  - Adaptive compensation -- The controller has the ability to vary the compensation between two stored sets of values in proportion to the measured load current. This allows the frequency response of the regulation loop to be nearly independent of load current. This feature is set using the PID_TAPS_ADAPT command and MISC_CONFIG in the DDC Advanced tab.
- ***Snapshot Data Collection*** -- Using the SMBus, you can signal the chip to capture a set of data points of chip status within a narrow time window. This allows calculation of efficiency and other parameters from values taken at nearly the same time. This feature uses the SNAPSHOT_CONTROL command on the DDC Advanced tab.
- ***Droop Characteristics*** (also called active voltage positioning) -- The VOUT_DROOP command controls the output voltage to follow a programmed resistance characteristic vs. load current. This behavior is required for some processor loads, and also required in current sharing applications. The VOUT_DROOP command is on the Basic tab.

6 Summary

Upon reaching this point in the design process, you have accomplished the following initial steps for properly designing and configuring the Digital-DC parts into a circuit:

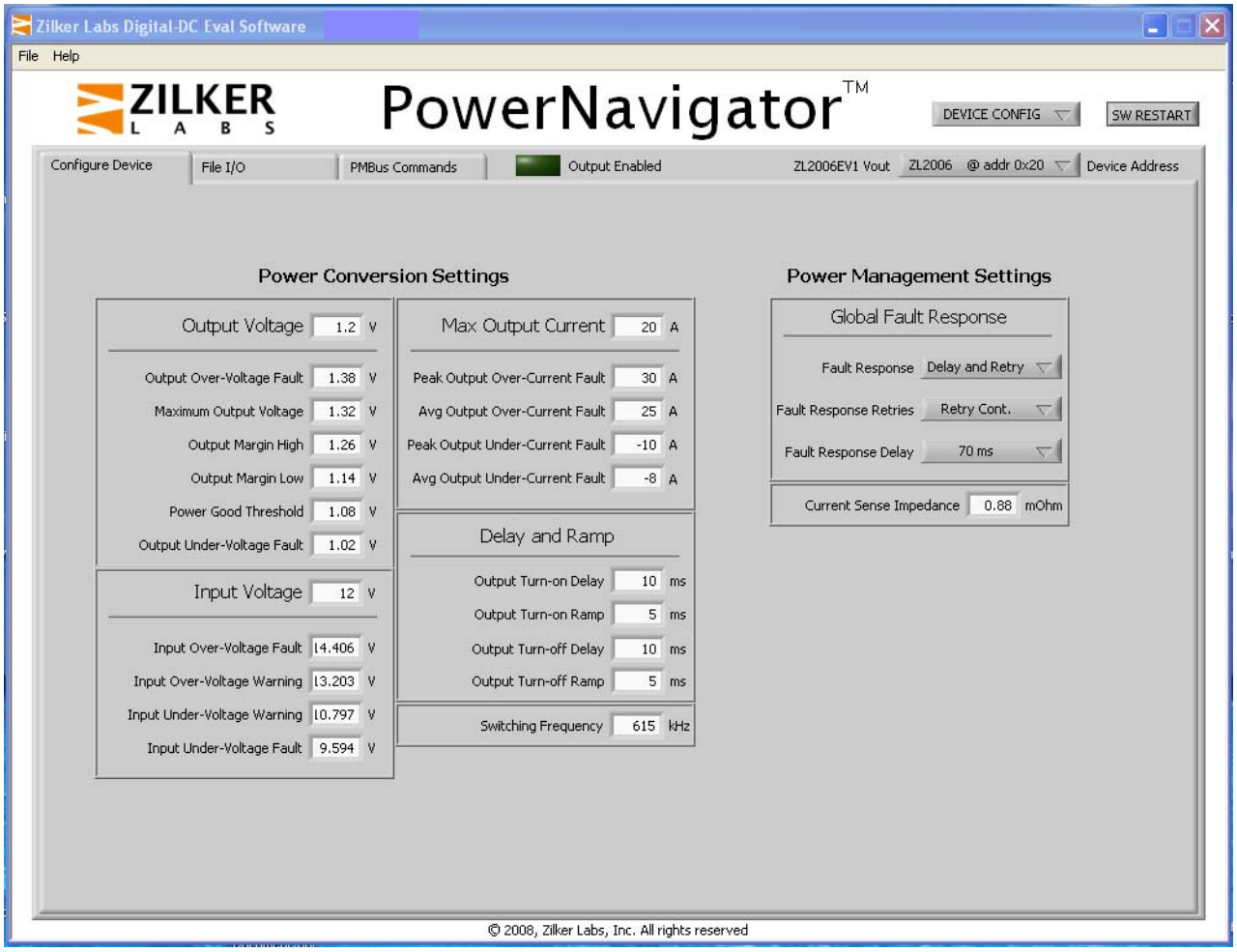
- You have determined the target specifications of the regulator and power management functions and also the design optimization goals of the circuit.
- You have designed a first pass at the power stage components which will achieve the desired specifications and goals.
- You have determined the initial and required pinstraps for achieving safe power-up of the controller.
- You have determined pinstraps and stored configurations for the advanced features of the controllers.

With these steps accomplished, you should have a working regulator and power management strategy, as well as a good baseline design to make small changes for further optimization and perfection of the implementation. Due to the flexibility and ease of use of the Zilker controllers, this process can be accomplished quickly, allowing you to focus on other issues of importance in the system design.

Appendix A

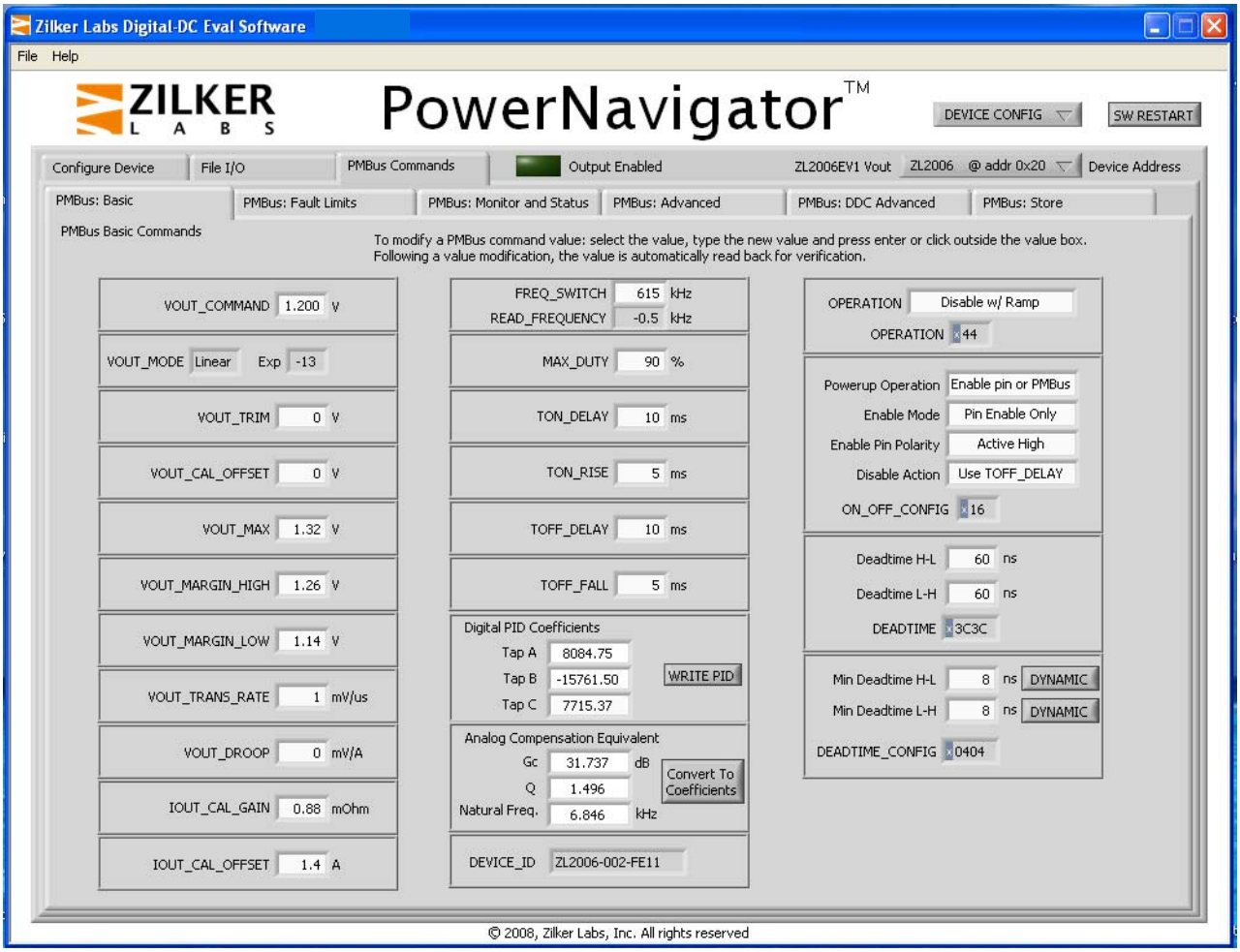
This appendix shows the settings used in the PowerNavigator software for our ZL2006 sample design configuration.

This is the Configure Device screen.



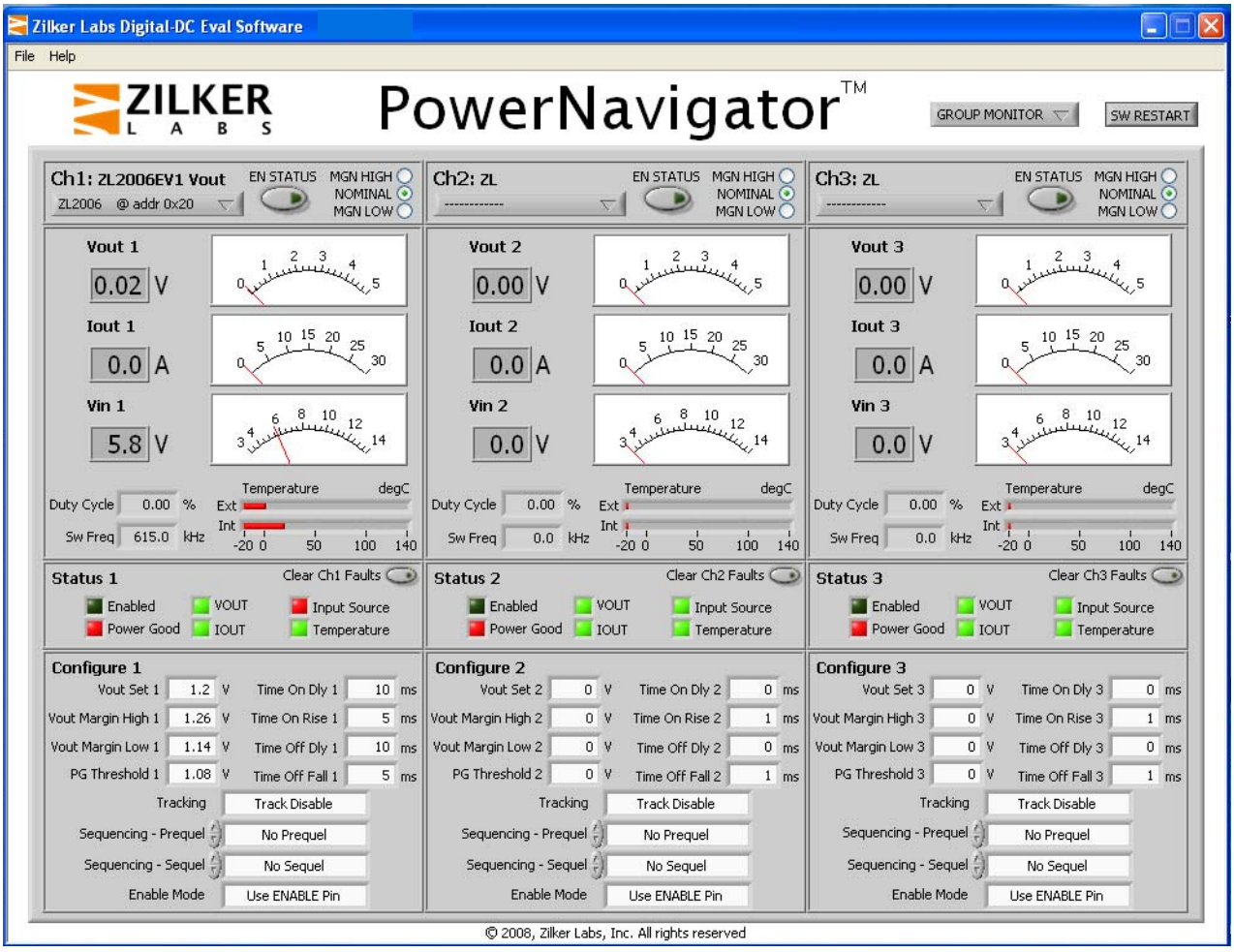
This appendix shows the settings used in the PowerNavigator software for our ZL2006 sample design configuration.

This is the PMBus basic configuration screen.



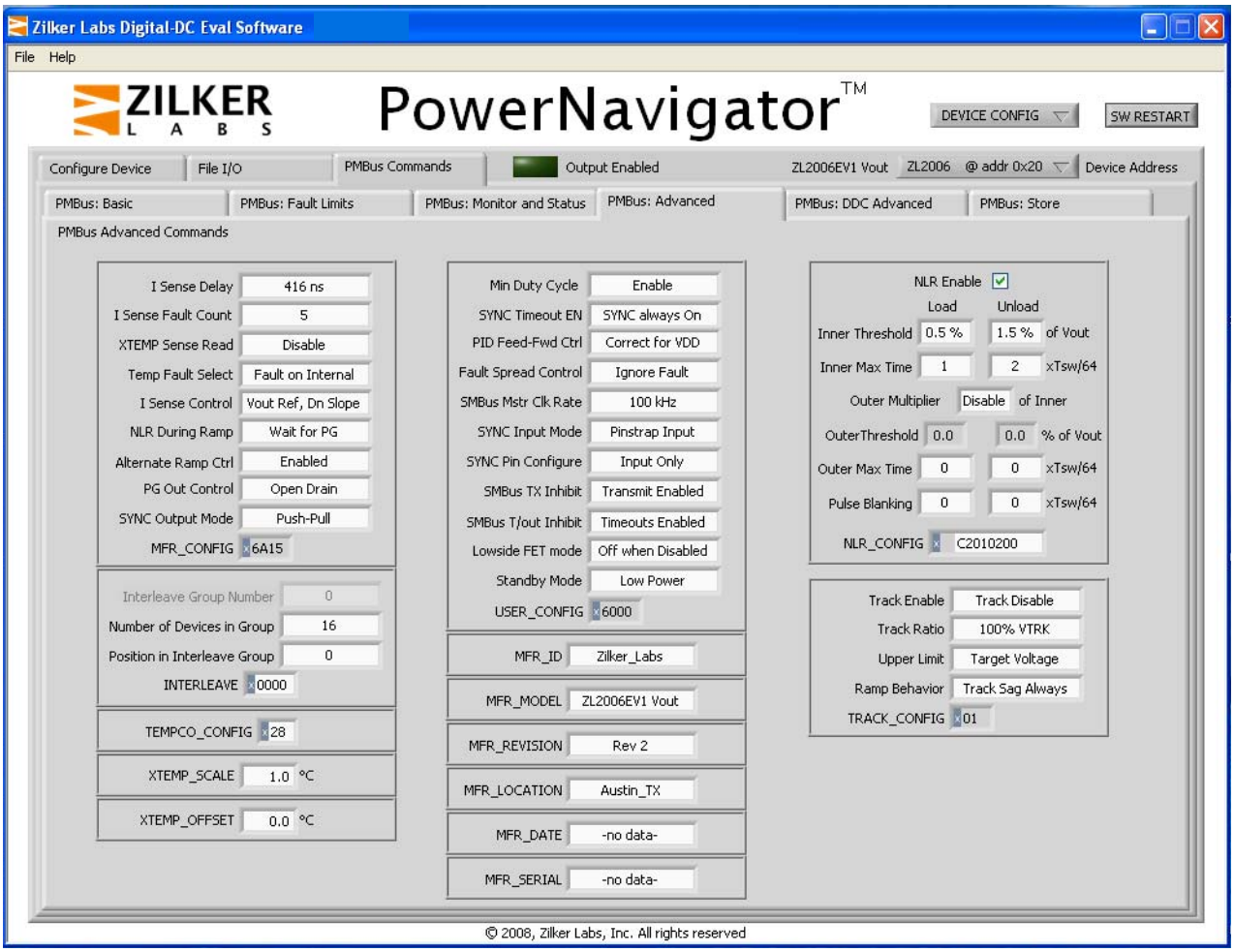
This appendix shows the settings used in the PowerNavigator software for our ZL2006 sample design configuration.

This is the Group Settings screen.



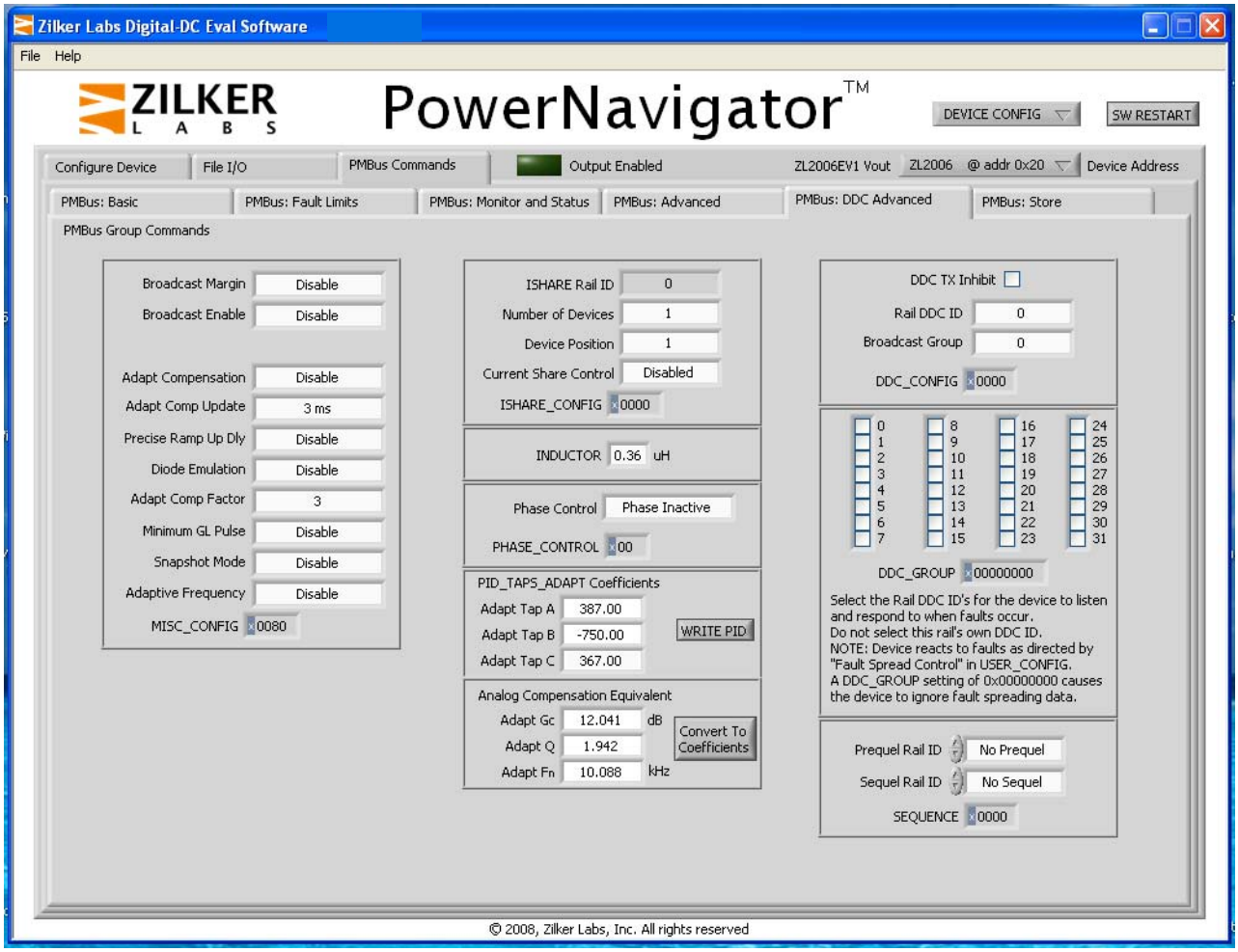
This appendix shows the settings used in the PowerNavigator software for our ZL2006 sample design configuration.

This is the PMBus Advanced screen.



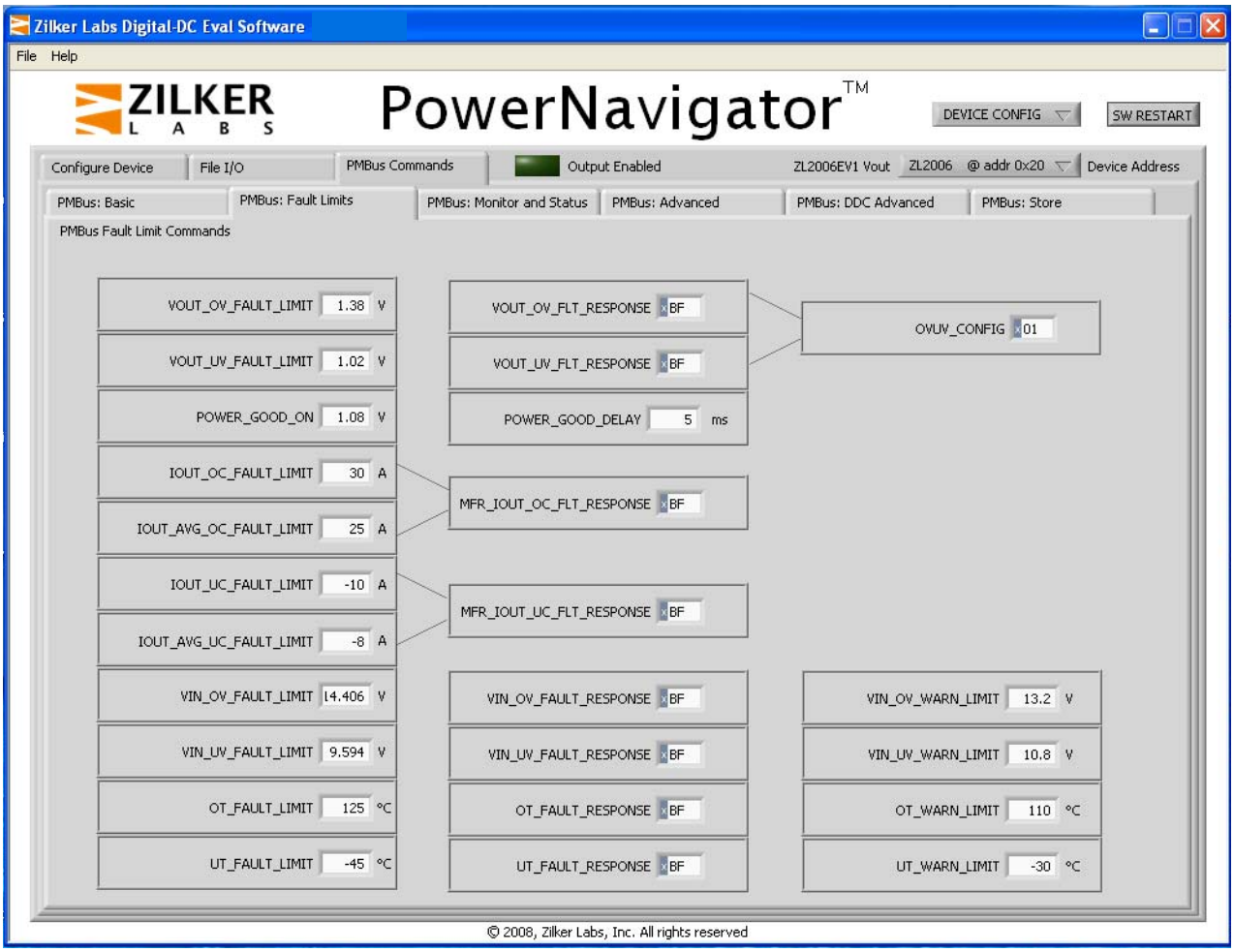
This appendix shows the settings used in the PowerNavigator software for our ZL2006 sample design configuration.

This is the PMBus Advanced DDC screen.



This appendix shows the settings used in the PowerNavigator software for our ZL2006 sample design configuration.

This is the PMBus Fault Limits screen.



Appendix B: ZL2006 Design Example for 12V input:1.2V@15A rated output, Transient Optimized

Design Specification

Parameter	Design Goal	Units
Output voltage	1.2	V
Output current	15	A
Output current	20	A surge 10µs
Frequency	615	kHz
Ripple voltage	12	mV
Transient Deviation	36	mV

Component Requirements

	Value	Units	Value	Units	Vendor	Part Number
Lout	360	nH	1.1	mΩ	VISHAY	IHLP4040DZERR36M61
Cout	5x100	µF	2	mΩ	TAIYO YUDEN	JMK325BJ107MY-T
Cout	2x680	µF	15	mΩ	UNITED CHEMI-CON	APXA6R3ARA681MJC0G
QH	11	mΩ	8	nC	FAIRCHILD	FDMS8692
QL	3.5	mΩ			FAIRCHILD	FDMS8670AS
Cin	5x10	µF			PANASONIC-ECG	ECJ-3YB1E106K

Pinstrap Table

Function	Pin	Setting	Result
Address	SA0	SA0=19.6k	0x20
	SA1	SA1=11k	
VOUT_MAX	V0	V0=16.2k	VOUT_MAX=3.63V VOUT_COMMAND=3.3V
	V1	V1=34.8k	
Clock Config	CFG	CFG=Z	Fsw=400kHz, SYNC=Input
Compensation	FC0	FC0=Z	fsw/120 < fn < fsw/60
	FC1	FC1=Z	fsw/10 > fzesr > fsw/30

ZL2006 Configuration File Example for 12V input:1.2V@15A rated output, Transient Optimized

```
#File name of config file
#<Project/BoardName>_<DeviceAddr>_<RailName/No.>_<Devi-
ceNo.>_<FileRev>.txt
#ZL2006EV1_0x20_1V2_ZL2006_4R1.txt

#This configuration file is intended for the device
# described in the filename of this file and the
# ASCII MFR_xxxx # commands in this file
#with L=400nH, Co=5x(100uF/2.0mohm)+(2X680uF/10mohm)
#All PASSWORD protections must be cleared on the #device
before loading this file

#Device ID:   ZL2006
#Schematic revision: 01
#BOM revision:   02
#PowerNavigator Revision:   3.2.1
#Revision Log:
#Rev. 4.1  10/22/08, K. Dehnel
#-----------------------------------------------------
#Configuration File Format:
#PMBus Command <tab> Hex Value

#Erase user store & default store
RESTORE_FACTORY
STORE_USER_ALL
STORE_DEFAULT_ALL

#Prepare device for all commands to be
# added to the DEFAULT store
RESTORE_DEFAULT_ALL

#Manufacturer information fields in ASCII:
#MFR_SERIAL reserved for use at time of manufacturing
#MFR_DATE  reserved for use at time of manufacturing
MFR_ID  Zilker Labs
MFR_MODEL  ZL2006EV1
MFR_LOCATION  Austin
MFR_REVISION  Rev 4.1

#Output Voltage commands
VOUT_COMMAND  1.200000  #V
#VOUT_MARGIN_HIGH   1.545    #V
#VOUT_MARGIN_LOW  1.455    #V
#VOUT_OV_FAULT_LIMIT   1.724976    #V
#VOUT_UV_FAULT_LIMIT   1.275024    #V
#POWER_GOOD_ON  1.349976    #V
#POWER_GOOD_DELAY  5.000000    #ms
#VOUT_OV_FAULT_RESPONSE  0x80    #immediate shutdown
#VOUT_UV_FAULT_RESPONSE  0x80    #immediate shutdown
OVUV_CONFIG  0x01    #2 counts

#Output current
IOUT_CAL_GAIN  0.920000    #mohms
IOUT_CAL_OFFSET  1.4    #A
IOUT_OC_FAULT_LIMIT  30.000000    #A
IOUT_AVG_OC_FAULT_LIMIT  24.000000    #A
IOUT_UC_FAULT_LIMIT  -15.000000    #A
IOUT_AVG_UC_FAULT_LIMIT  -10.000000    #A
#MFR_IOUT_OC_FAULT_RESPONSE  0x80 #immediate shutdown
#MFR_IOUT_UC_FAULT_RESPONSE  0x80 #immediate shutdown

#Input Voltage
VIN_OV_FAULT_LIMIT  13.4    #V
VIN_OV_WARN_LIMIT  13.0    #V
#VIN_OV_FAULT_RESPONSE    0x80    #immediate shutdown
VIN_UV_WARN_LIMIT      4.7    #V
VIN_UV_FAULT_LIMIT      4.5    #V
#VIN_UV_FAULT_RESPONSE    0x80    #immediate shutdown

#Other Faults
OT_FAULT_LIMIT      120.000000  #deg C
OT_WARN_LIMIT       110.000000  #deg C
#OT_FAULT_RESPONSE  0x80    #immediate shutdown
UT_WARN_LIMIT      -20.000000  #deg C
UT_FAULT_LIMIT      -30.000000  #deg C
#UT_FAULT_RESPONSE  0x80    #immediate shutdown
#VMON fault threshold (in applicable devices)
#VMON fault response (in applicable devices)

#General converter commands
TON_DELAY         5.000000  #ms
TON_RISE      5.000000  #ms
TOFF_DELAY        5.000000  #ms
TOFF_FALL         5.000000  #ms
FREQUENCY_SWITCH    615.000000  #kHz
#PID_TAPS    A=8084.75, B=-15761.41, C=7715.36
PID_TAPS    A=15141.91, B=-29677.9, C=14599.08
MAX_DUTY        90.000000  #%
DEADTIME  0x3838    #56ns max
DEADTIME_CONFIG  0x0404    #8ns min, dynamic
INDUCTOR  0.36    #uH
#OPERATION  0x44
#ON_OFF_CONFIG  0x16

#Advanced commands
MFR_CONFIG    0x6A14
USER_CONFIG    0x6000
NLR_CONFIG    0xCA010200
#NLR_CONFIG    0x00000000
ISHARE_CONFIG    0x1200
#TRACK_CONFIG    <nn>
MISC_CONFIG    0x0480
INTERLEAVE    0x0000
DDC_CONFIG    0x0012
DDC_GROUP    0x00000000
SEQUENCE    0x0000
TEMPCO_CONFIG    0x28
#XTEMP_SCALE    <nn>
#XTEMP_OFFSET    <nn>

#Security Settings
#PUBLIC_PASSWORD  <xxxx>
#PRIVATE_PASSWORD  <yyyyyyyyy>
#UNPROTECT     <nnnnnnnnnnnn>

STORE_DEFAULT_ALL
RESTORE_DEFAULT_ALL  #comment out if USER stores follow this
command

# - end of file -
```

Appendix C: ZL2005 Design Example for 12V input:1.2V@10A rated output, Size Optimized

Design Specification

Parameter	Design Goal	Units
Output voltage	1.2	V
Output current	10	A
Frequency	615	kHz
Ripple voltage	12	mV
Transient Deviation	48	mV

Component Requirements

	Value	Units	Value	Units	Vendor	Part Number
Lout	470	nH	4	mΩ	VISHAY	IHLP2525CZERR47M01
Cout	5x47	µF	2.5	mΩ	TDK	C3216X5R0J476M
QH	16.8	mΩ	5	nC	INFINEON	BSZ130N03LS
QL	4.8	mΩ			INFINEON	BSZ035N03LS
Cin	2x22	µF			MURATA	GRM32ER61C226KE20L

Pinstrap Table

Function	Pin	Setting	Result
Address	SA0	SA0=19.6k	0x20
	SA1	SA1=11k	
VOUT_MAX	V0	V0=16.2k	VOUT_MAX=3.63V VOUT_COMMAND=3.3V
	V1	V1=34.8k	
Clock Config	CFG	CFG=Z	Fsw=400kHz, SYNC=Input
Compensation	FC0	FC0=Z	fsw/120 < fn < fsw/60
	FC1	FC1=Z	fsw/10 > fzesr > fsw/30

ZL2005 Configuration File Example for 12V input:1.2V@10A rated output, Size Optimized

```
# Configuration file for ZL2005PEV4

#syntax:
#PMBus Command <tab> Value

#Erase default and user store
RESTORE_FACTORY
STORE_DEFAULT_ALL

MFR_ID  ZilkerLabs
MFR_MODEL   ZL2005PEV4
MFR_REVISION   Rev_1.6
MFR_LOCATION   Austin_TX

VIN_OV_FAULT_LIMIT 13.5
VIN_OV_WARN_LIMIT 13.2
VIN_UV_FAULT_LIMIT 4.2
VIN_UV_WARN_LIMIT 4.5

VOUT_COMMAND   1.2 #V
FREQUENCY_SWITCH 600 #kHz

POWER_GOOD_DELAY 1
TON_DELAY      15
TON_RISE      5
TOFF_DELAY    15
TOFF_FALL     5
SEQUENCE   0x0000



#Use Rdson current sense method with
# internal temp sensor
MFR_CONFIG    0x7981

USER_CONFIG     0x0000

PID_TAPS  A=1569.69, B=-2903.12, C=1412.91

IOUT_OC_FAULT_LIMIT   20.
IOUT_AVG_OC_FAULT_LIMIT  15.

IOUT_UC_FAULT_LIMIT   -10.
IOUT_AVG_UC_FAULT_LIMIT  -8.

#low FET not enabled for output OV, output OV and
# UV count to 2
OVUV_CONFIG   0x01

IOUT_SCALE     3.65

IOUT_CAL_OFFSET    0

#Set temperature compensation at 4000ppm/ C internal
# temp sensor
TEMPCO_CONFIG  0x28

NLR_CONFIG  0xB303

#VOUT_DROOP   2 #mV/A

STORE_DEFAULT_ALL
RESTORE_DEFAULT_ALL
```

Appendix D: ZL2006 Design Example for 12V input:1.8V@30A, rated output, Efficiency Optimized (Current Sharing)

Design Specification

Parameter	Design Goal	Units
Output voltage	1.8	V
Output current	30	A
Frequency	300	kHz
Ripple voltage	12	mV
Transient Deviation	36	mV

Component Requirements

	Value	Units	Value	Units	Vendor	Part Number
Lout	560	nH	1.2	mΩ	VISHAY	IHLP5050FDERR56M01
Cout	8x47	µF	2.5	mΩ	TDK	C3216X5R0J476M
Cout	4x820	µF	10	mΩ	UNITED CHEMI-CON	APXA6R3ARA821MJC0G
QH	3.8	mΩ	20	nC	INFINEON	BSC030N03LS
QL	1.8/2	mΩ			INFINEON	BSC016N03LS (2 each)
Cin	6x10	µF			PANASONIC-ECG	ECJ-13YB1E106K
Cin	4x330	µF	18	mΩ	UNITED CHEMI-CON	APXA160ARA331MJC0G

Pinstrap Table

Function	Pin	Setting	Result
Address	SA0	SA0=19.6k	0x20
	SA1	SA1=11k	
VOUT_MAX	V0	V0=16.2k	VOUT_MAX=3.63V VOUT_COMMAND=3.3V
	V1	V1=34.8k	
Clock Config	CFG	CFG=Z	Fsw=400kHz, SYNC=Input
Compensation	FC0	FC0=Z	fsw/120 < fn < fsw/60
	FC1	FC1=Z	fsw/10 > fzesr > fsw/30

ZL2006 Configuration File Example for 12V input:1.8V@30A rated output, Efficiency Optimized (Current Sharing)

```
# This configuration is intended for Zilker Labs ZL2006EV2-
Ch1a
# U1 / ZL2006
# ZL Configuration File Revision 2
# Schematic revision level 02
# BOM revision level_
# ZL Author B. KATES

#Erase default and user stores
RESTORE_FACTORY
STORE_USER_ALL
STORE_DEFAULT_ALL
RESTORE_DEFAULT_ALL

MFR_ID Zilker_Labs
MFR_MODEL   ZL2006EV2R2
MFR_REVISION   Prod_Rev8
MFR_LOCATION   Austin_TX
MFR_DATE   10_1_08
MFR_SERIAL   ch1A

VOUT_COMMAND  1.80
VOUT_MAX   3.65
VOUT_DROOP    0.5
VOUT_MARGIN_HIGH    1.89
VOUT_MARGIN_LOW     1.71
VOUT_UV_FauLT_LIMIT  1.53
VOUT_UV_FAULT_RESPONSE  0x80
VOUT_OV_FauLT_LIMIT  2.07
VOUT_OV_FAULT_RESPONSE  0x80
OVUV_CONFIG   0x80

IOUT_SCALE    1.13
IOUT_CAL_OFFSET  1.00

IOUT_OC_FAULT_LIMIT   45.0
IOUT_AVG_OC_FAULT_LIMIT   40.0
IOUT_UC_FAULT_LIMIT    -17.0
IOUT_AVG_UC_FAULT_LIMIT   -14.0
MFR_IOUT_OC_FAULT_RESPONSE   0xBF
MFR_IOUT_UC_FAULT_RESPONSE   0xBF

VIN_OV_FAULT_LIMIT     14.0
VIN_OV_WARN_LIMIT      13.5
VIN_OV_FAULT_RESPONSE     0x80

VIN_UV_WARN_LIMIT      4.641
VIN_UV_FAULT_LIMIT     4.50
VIN_UV_FAULT_RESPONSE     0x80

OT_WARN_LIMIT    110.0
OT_FAULT_LIMIT   120
OT_FAULT_RESPONSE  0xBF

UT_WARN_LIMIT   -20
UT_FAULT_LIMIT   -30
UT_FAULT_RESPONSE  0xBF

POWER_GOOD_ON   1.35
POWER_GOOD_DELAY   10.0

TON_DELAY     15
TON_RISE   5
TOFF_DELAY    15
TOFF_FALL     5
DEADTIME   0x3838
DEADTIME_CONFIG   0x0808
MAX_DUTY   96
INDUCTOR   0.56

FREQUENCY_SWITCH  300 # kHz

#CompZL Taps for G=31.596,  Q=0.301,   f=3.506kHz,
fsw=300kHz, Vi=12, Vo=1.8
PID_TAPS   A=7948.25,  B=-14135.50, C=6225.25  # dIo=30-60A
@ 2.5A/us, dVo=+/-3.5%

# Advanced

USER_CONFIG      0x6051 # SYNC Input
MFR_CONFIG       0x82D4
NLR_CONFIG       0xE2010355
INTERLEAVE       0x0000
TEMPCO_CONFIG    0xA8
TRACK_CONFIG   0x00

# Advanced 2
MISC_CONFIG    0x4080
ISHARE_CONFIG  0x0121 # Ishare Group 1, members 2, position
1, CS En
DDC_CONFIG  0x0101 # DDC Rail ID 1, Broadcast Group 1
DDC_GROUP   0x00000000

STORE_DEFAULT_ALL
RESTORE_DEFAULT_ALL
```

Revision History

Date	Rev. #	
Nov 21, 2008	1.0	Initial release
May 1, 2009	1.1	Assigned file number AN2040 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to datasheet content.

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(Rev.4.0-1 November 2017)

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