NLR Configuration for DDC Products

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Introduction

This application note describes the non-linear response loop that is incorporated in Zilker Labs' second generation Digital-DC™ devices. The function and configuration options of this feature are explained to give system designers the capability to make advantageous choices among regulation budgets, power consumption and regulator size.

Overview

The non-linear response (NLR) loop incorporated in Zilker Labs' devices decreases the response time and the output voltage deviation in the event of a sudden output load current step. The NLR loop incorporates a secondary error signal processing path that bypasses the primary error loop when the output begins to transition outside of the standard regulation limits. This scheme results in a higher equivalent loop bandwidth than what is possible using a traditional linear loop.

When a load current step function imposed on the output causes the output voltage to drop below the lower regulation limit, the NLR circuitry will force a positive correction signal that will turn on the upper MOSFET and quickly force the output to increase. Conversely, a negative load step (i.e., removing a large load current) will cause the NLR circuitry to force a negative correction signal that will turn on the lower MOSFET and quickly force the output to decrease. Refer to Figure 1 for an explanation of NLR terms. Additional information and an example for choosing the NLR_CONFIG values can be found in Appendix A.

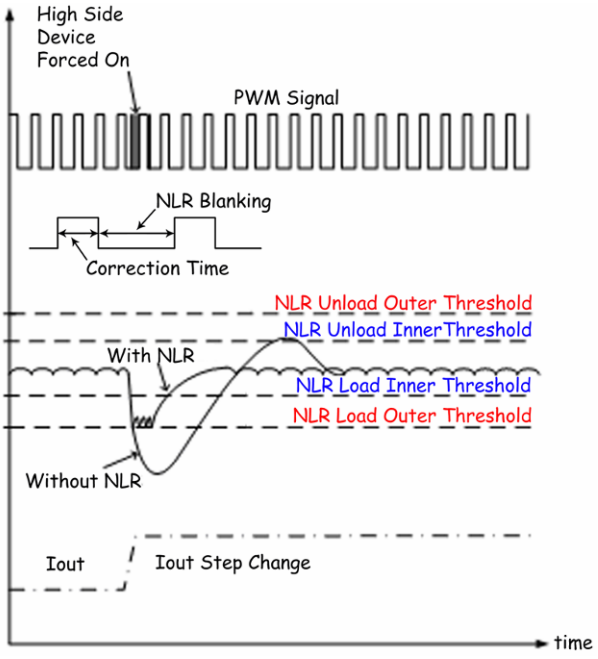

Figure 1. Non Linear Response (NLR)

Configuration Setting Variables

There are three types of configuration setting variables utilized in the NLR subsystem: thresholds, correction times, and blanking. The following paragraphs explain how these settings affect the NLR response and the method for configuring them for optimal performance.

NLR Thresholds

There are four thresholds available in the newer Digital DC series parts that support the DDC bus. The thresholds are referred to as Loading Outer and Inner and Unloading Outer and Inner. The inner thresholds can be set from 0.5% to 4.0% of the nominal output voltage in 0.5% steps. The outer thresholds can be multiples of 2, 3 or 4 times the inner thresholds, or they can be disabled.

Table 1. NLR Parameters

Parameter	Range	Units
Loading or unloading inner Threshold	0.5 to 4.0	% of V_{OUT}
Loading or unloading outer Threshold	0, 2, 3, 4	Times Inner threshold
Loading Correction Time	0 - 15	x $T_{SW}/64$
Unloading Correction Time	0 - 15	x $T_{SW}/64$
Blanking Control	0 - 15	Index into Table 2

Table 2. Blanking Control

Index	Tsw/64 Units
0	0
1	1
2	2
3	4
4	8
5	16
6	32
7	48
8	64
9	80
10	96
11	128
12	160
13	176
14	192
15	224

When the output voltage crosses one of the loading thresholds, the high side (control) MOSFET (QH in Figure 2) is immediately turned on (unless prohibited by the blanking timer or a current sampling interval, as discussed later), and the low side (synchronous) MOSFET (QL) is turned off. This immediate change to the state of a MOSFET is referred to as a “correction.” Since a loading threshold corresponds to an on-time correction to the high side MOSFET, the loading

inner threshold is below the output voltage, and will be activated by a load step in the positive (increasing) direction. Likewise, the unloading inner threshold can be set from 0.5% to 4.0% above the nominal output voltage in 0.5% steps, and is independent of the setting of the loading inner threshold except that the multiplier for the loading and unloading outer thresholds must be the same. In a similar fashion, if the unloading threshold is exceeded, the low side (synchronous) MOSFET is immediately turned on and the high side MOSFET is turned off.

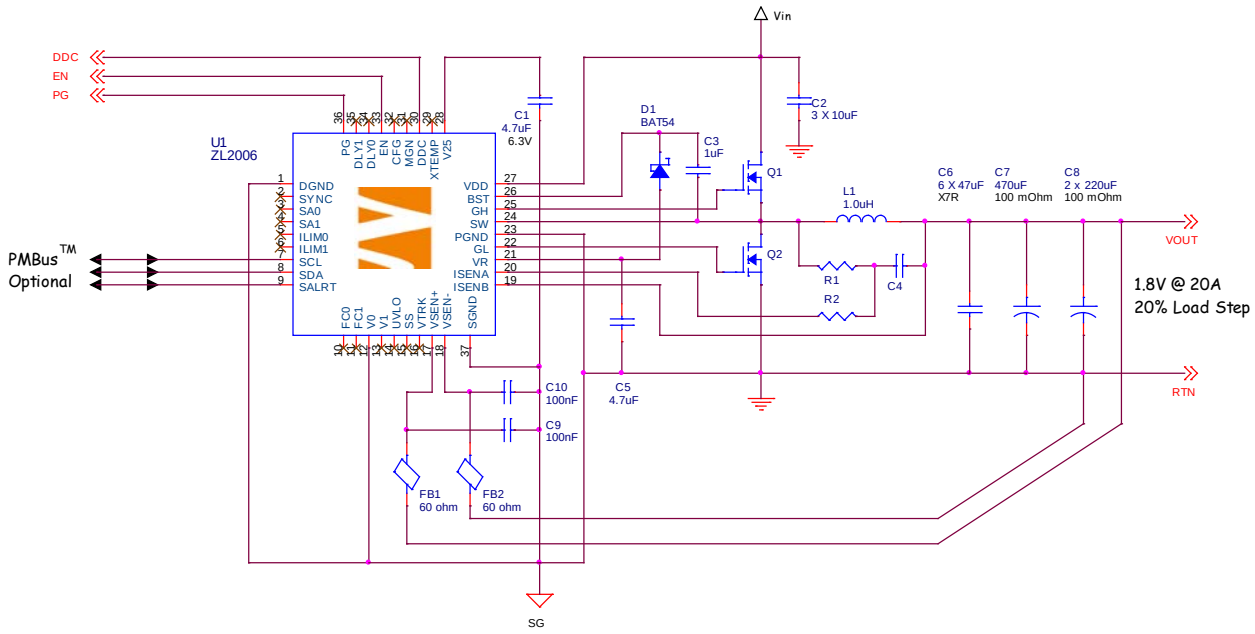

Figure 2. Typical Application Circuit

The NLR thresholds are set with the NLR_CONFIG command (Zilker custom PMBus command 0xD7) and should be set 0.5% to 1.0% above the measured output voltage peak ripple and noise to avoid unintentional activation of NLR.

The use of outer thresholds is optional. The outer thresholds allow the use of other modes of non-linear response as described below. The effectiveness of outer thresholds is evaluated by applying step loads with outer thresholds enabled and disabled and observing the resulting output voltage response on an oscilloscope. When any NLR threshold is exceeded, the correction continues until either the output voltage returns to within 0.25% of the nominal output voltage, called the hysteresis threshold, or the corresponding maximum correction time has expired.

Correction Time

The loading and unloading correction times are expressed as $1/64^{th}$ fractions of the total switching period ($Tsw=1/F_{SW}$). The loading and unloading correction times can be set from 1 to 15 of these $1/64^{th}$ switching period fractions. Each threshold (loading outer, loading inner, unloading inner, unloading outer) has a correction time associated with it which can be set independently of the others.

The correction to the output voltage increases proportional to the square of the applied correction time and inversely proportional to the L x C product in the output filter. Thus, large correction times are seldom needed unless the averaging filter is very large.

For converters with nominal duty ratios near 0 or 1, large correction times may be needed on the unloading or loading thresholds, respectively. This is because the voltage is very small across the averaging inductor to respond to the step in the output current, and additional time is needed to ramp the current to the new value.

Blanking

When an NLR correction has terminated, either due to a hysteresis threshold crossing or expiration of a correction time, a blanking timer is started. During a blanking time, corrections from the NLR are blocked and do not change the state of the high or low MOSFETs. Blanking time is set as an index from 0 to 15 which represents the time units listed in Table 2. The blanking time units are $1/64^{th}$ fractions of the total switching period ($Tsw=1/F_{SW}$). A minimum blanking time is set by the controller IC to accommodate deadtime between MOSFET transitions. Generally, this value ranges from 2-5 x Tsw/64 and is added to the values selected by the user.

NLR Modes

Three different operating modes allow the user the flexibility to choose the mode most useful for the application. Table 3 is a quick reference for choosing an NLR mode based on the damping factor, Q, of the power filter. These modes are:

1) *Single level* (Mode 1) – inner thresholds and inner correction times only. This mode is useful for initial testing, or cases which have relatively modest transient requirements, or cases in which the power filter cannot be designed with optimal damping. See Figure 3 on page 5.

2) *Two level* (Mode 2) – inner and outer thresholds set, inner and outer correction times set. Generally, the inner correction times will be smaller than the outer correction times. The result should be smaller pulses between thresholds, then larger pulses until the output returns below the inner threshold. This mode is useful as a graduated response to large transients. See Figure 4 on page 5.

3) *Hysteretic* (Mode 3) – inner and outer thresholds enabled, correction times set only in outer position, with inner position set to 0. This mode begins an aggressive pulsed correction at the outer threshold and does not cease the correction until the output voltage returns below the inner threshold. This mode is most useful for cases which require tight control of the output deviation in the presence of a large transient and significant switching ripple. The output filter must be overdamped for this mode to succeed. See Figure 5 on page 6.

Table 3. NLR Mode Selection

	$Q \leq 0.7$	**$0.7 < Q \leq 1.2$**	**$Q > 1.2$**
Mode	3	2	1

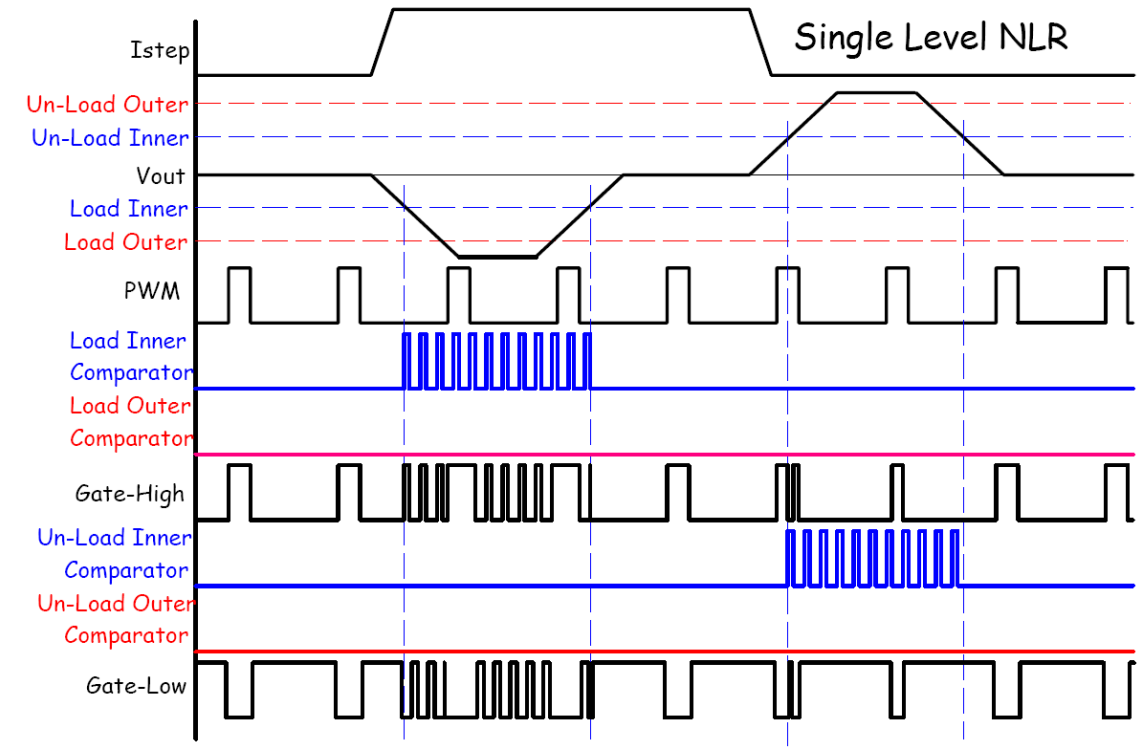

Figure 3. Single Level NLR

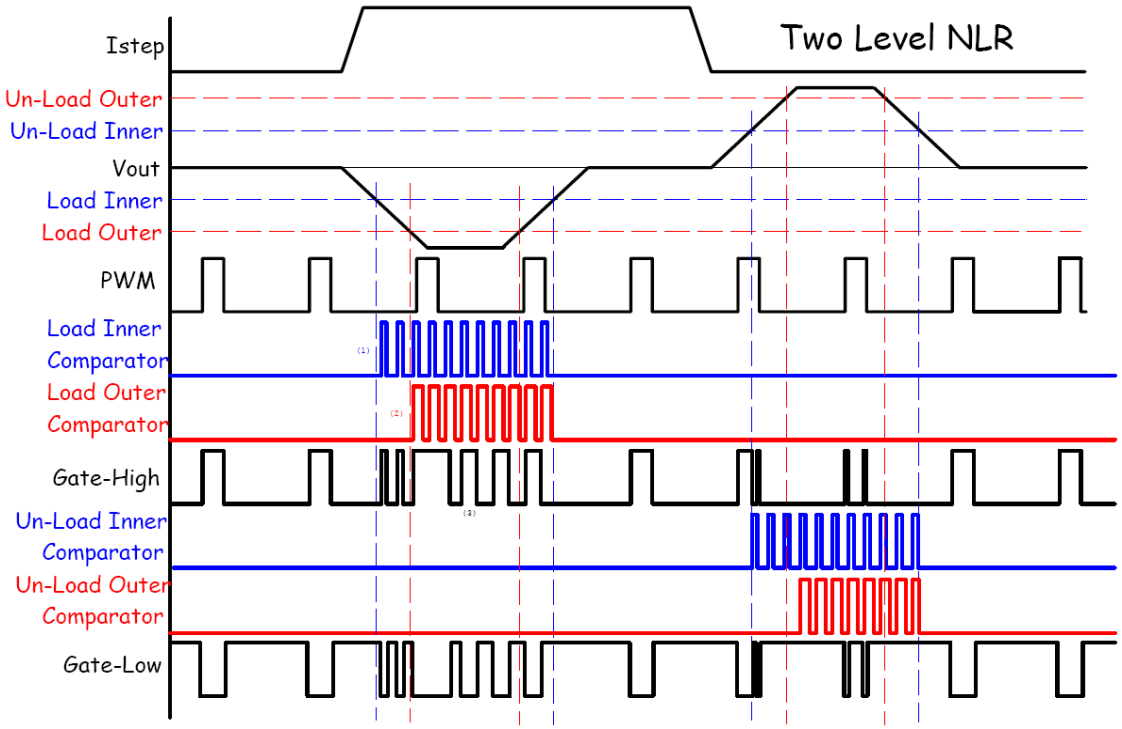

Figure 4. Two Level NLR

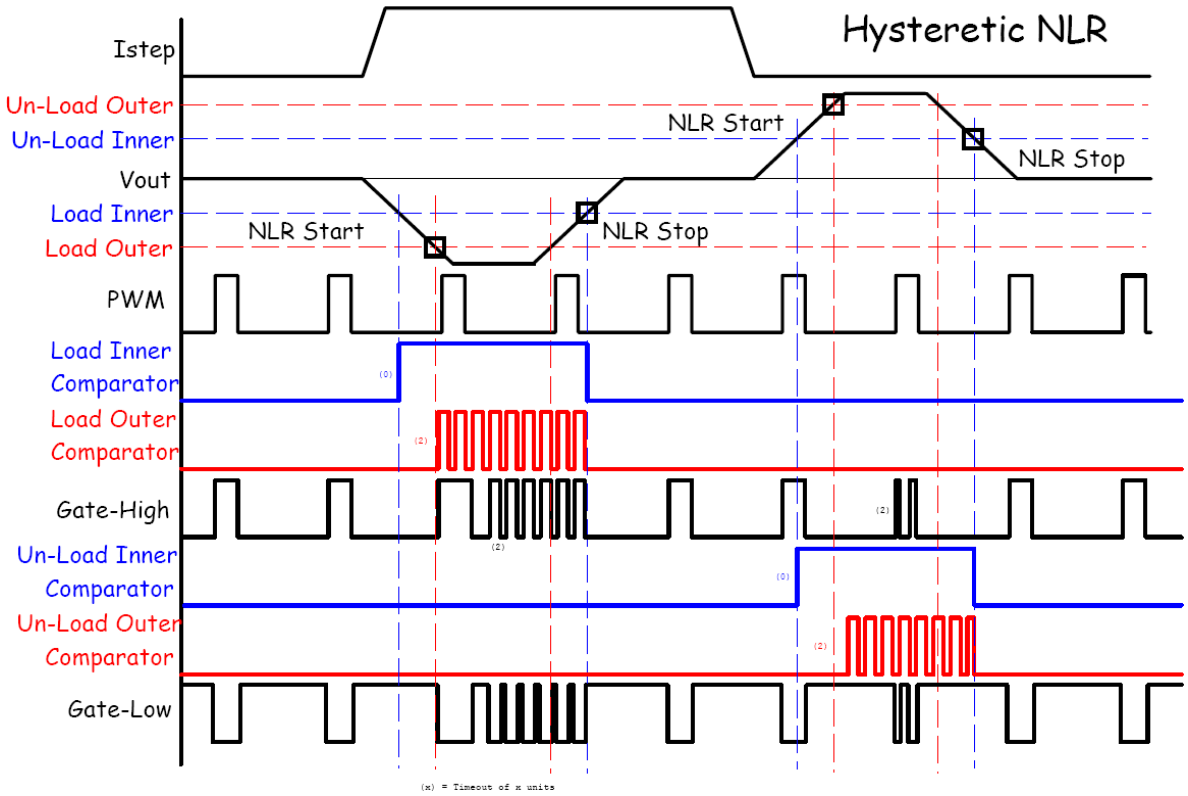

Figure 5. Hysteretic NLR

Setting Correction and Blanking Times

The NLR parameters are set using the NLR_CONFIG command. Figure 6 shows nominal NLR settings for the products in the DDC family.

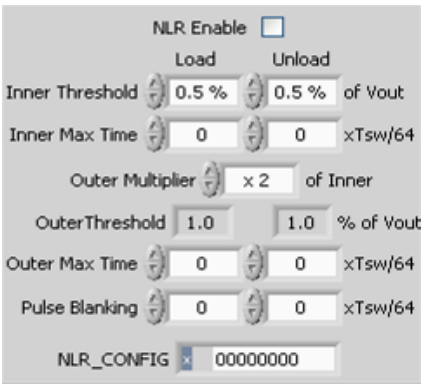

Figure 6. Nominal NLR Settings

The correction times (Max Times) needed can be estimated from the equations for the second order output filter if the damping is not excessive. It can be shown for a second order filter that the change in current needed to cause (or correct) a voltage deviation is

$$\Delta I_L = \Delta Vo / Zo$$

where

ΔI_L is the required correction current

ΔVo is the error in output voltage (here assumed to be equal to the NLR threshold value)

$Zo = \sqrt{L/C}$ is the output filter characteristic impedance.

Once the correction current is established, the NLR correction units N_{load} and N_{unload} can be estimated from these relations:

$$N_{load} = \frac{64 * \Delta I_L * L}{T_{sw} * (V_g - V_o)}$$

$$N_{unload} = \frac{64 * \Delta I_L * L}{T_{sw} * V_o}$$

where

N_{load} is the number of correction time units required for the loading response

N_{unload} is the number of correction time units required for the unloading response

L is the averaging inductor value in Henrys

V_g is the converter input voltage

V_o is the converter output voltage

Combined with the previous relation, this leads to the result

$$N_{load} = \frac{64 \Delta V_o \sqrt{LC}}{T_{sw}(V_g - V_o)}$$

$$N_{unload} = \frac{64 \Delta V_o \sqrt{LC}}{T_{sw} V_o}$$

The correction times should be rounded down to the next lower integer.

A good first estimate for the blanking values N_{bl} can be taken from the relations

$$N_{bl} = N_{load} \frac{V_g - V_o}{V_o} \text{ for loading}$$

$$N_{bul} = N_{unload} \frac{V_o}{V_g - V_o} \text{ for unloading}$$

As with outer thresholds, correction and blanking times are optimized by experimentation.

After setting suitable outer and inner thresholds and correction and blanking times as calculated above, apply the maximum expected load step and observe the output voltage response. The output voltage should settle back within the desired regulation band within two or fewer opposite NLR excursions (in the polarity opposite the initial output voltage deviation), also referred to as overshoot. More than two overshoots will cause an excessive increase in the effective switching frequency and could lead to a reduction in overall power supply efficiency. Continue to increase the correction time with a corresponding increase in blanking until a balance is met between improved transient response and number of overshoots. Likewise, reduce the blanking time to optimize transient response and simultaneously minimize overshoots. Finally, test the NLR settings over input and output voltage and output step current variations to verify that the desired performance has been achieved.

VSEN+, VSEN- Treatment

The NLR circuit employs sampling of the output voltage at high speed (64 x Fsw) for fast response to transients. Therefore, it will respond to perturbations and disturbances that occur at timescales much less than one switching cycle.

Care should be taken in the routing of the connections from the sensed output voltage to the VSEN+ and VSEN- terminals of the controller. These sensing connections should be routed as a differential pair, preferably between signal ground planes which are not carrying high currents. The routing should avoid areas of high electric fields (such as the switching or gate drive nodes in the power stage) or magnetic fields (such as in the vicinity of a power inductor).

In some applications, it may be desirable to employ a small filter on the VSEN+ and VSEN- sensing terminals to reduce spurious ringing and transition noise from the power stage. In order to avoid delaying or diminishing valid regulation signals, the filter should have a corner frequency about 0.5-5 times the switching frequency. A typical filter configuration is shown in Figure 7 below. The loss factor of the filter should be chosen so that there is not a strong resonance at the corner frequency.

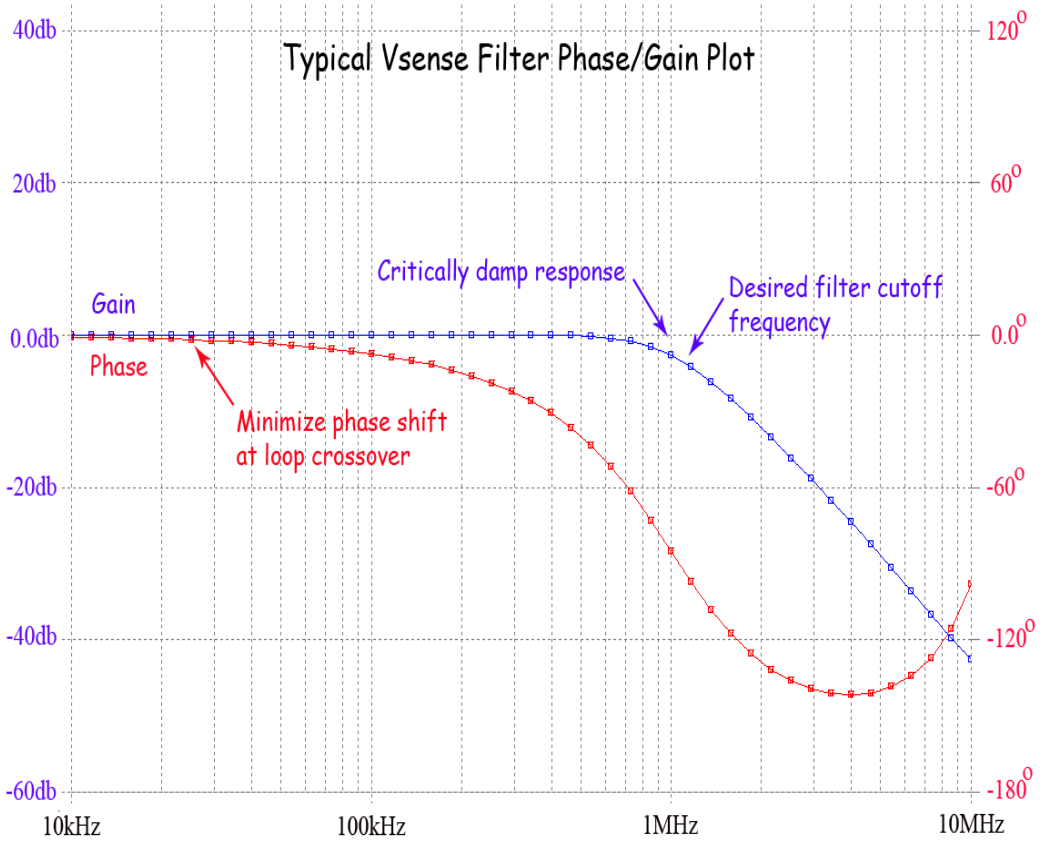

Figure 7. Vsense Filter Phase/Gain (Fsw 500-1400kHz)

Power Stage Damping

For best flexibility in choosing the settings of the NLR function, it is important for the design of the power filter to accommodate optimal damping. A filter which is well damped will respond to a transient stimulus with the most direct and minimal response. Filters with very little damping may limit the useful choices of NLR settings and the overall performance of the NLR feature.

Suitable damping can be incorporated by judicious choice of the capacitors in the power filter. Usually, capacitors with low equivalent series resistance (ESR), such as monolithic ceramic capacitors, are used to filter the switching ripple current. Additional bulk capacitors, usually chosen from several electrolytic types, are added to support the charge storage for transient loads.

If the bulk capacitance is chosen to be greater than about 70% of the total capacitance, the damping can be estimated by the following relationship:

$$Q \approx \frac{1}{R} \times \sqrt{\frac{L}{C}}$$

Where

R is the sum of the bulk ESR and other parasitic losses in the power stage, such as inductor DC resistance (DCR) and duty-ratio weighted average of the MOSFET ON resistance.

C is the total amount of capacitance in the output filter (including the amount at the load)

L is the value of the averaging inductor in the power stage

Q is the resonance factor of the power filter. This value should be kept in the range 0.7 to 1.0 for best results. If the calculated filter Q is greater than this range, bulk capacitors with higher ESR values can be chosen to improve the damping without significantly sacrificing ripple or step response. If there is no bulk capacitance, a small amount of resistance can be placed in series with about 70% of the capacitors to serve a damping function.

PID Compensator Settings

The linear and non-linear portions of the feedback loop coordinate the regulation of the output voltage. Thus, the settings of the linear loop compensator (PID values) influence the performance of the NLR circuit.

The best results are generally obtained with PID settings which give a stable linear loop compensation with high bandwidth and greater than 50 degrees of phase margin. It is not necessary to push for the highest possible bandwidth to achieve good transient response, since the non-linear portion of the loop is intended to address this. A stable loop compensation with a damped recovery and no overshoot is preferred over high bandwidth compensation with oscillatory recovery.

It is also desirable to have the compensation settings well matched to the power stage used. A graphical, intuitive simulation tool called CompZL™ is available to assist with these settings. See AN2027 – CompZL User's Guide for more information.

Current Sense and NLR

The architecture of Digital-DC parts is constructed to guarantee sampling of the output current for overcurrent protection purposes even when NLR activity is occurring. In order to accomplish current sampling, NLR activity will be suspended until a valid current sample is achieved, which can be no later than the third switching cycle after NLR activity begins. Once the current sample is achieved, NLR activity is allowed to resume. This may result in a perturbation of the voltage recovery waveform. In this case, protection from catastrophic fault is given higher priority than the recovery waveform.

Voltage Droop

The Digital-DC parts allow a pre-programmed output resistance characteristic to be configured into the parts. This function decreases the output voltage set-point in proportion to the sensed load current, with the proportionality constant being the droop resistance (See VOUT_DROOP in AN2033 – Zilker Labs PMBus Command Set – DDC Products). This function can be used to improve the transient envelope of the converter by as much as a factor of two.

When a converter utilizing voltage droop is subjected to a step load, a corresponding step in the output voltage regulation target is generated. The NLR thresholds are established relative to this target voltage generated by the droop function. The part's measured output current is used to generate the target; however, there is some delay (on the order of Tsw/16) due to digital filtering of the measured current signal.

The value of the output voltage droop resistance may be determined by a number of factors. It may be prescribed by the specifications of the load being powered, as is the case with many processors and other high-density logic devices. The droop may be defined by the parasitic resistances of the members of a multiphase group in order to achieve good dynamic current sharing. If there is no other constraint on the droop value, the best transient envelope should be achieved with a value given by the following relationship:

$$Vo\_droop = \frac{\Delta Vo\_pp}{Io\_rated}$$

Where

ΔVo_pp is the total transient regulation voltage budget (difference between the maximum and minimum transient regulation bounds), expressed in mV

Io_rated is the rated maximum load current for the total group, expressed in amperes

Vo_droop is the parameter entered into each controller, expressed in mV/A.

Threshold Scaling

When multiple channels are paralleled in a current sharing group, the effective output ripple is divided by the number of active members of the group due to the automatic spreading of the synchronization phases of the group members. Thus, when all members of the group are operating, the NLR thresholds can be set to a small value just above the minimum ripple amplitude. However, the Digital-DC power management capability allows one or more members of the group to be deactivated while maintaining the operation of the other members. When this occurs, the ripple amplitude will increase.

In order to avoid excessive NLR activity in this scenario, the Digital-DC features automatically adjust the NLR thresholds according to the ratio of *active* members of the group to *total* members of the group:

$$Vt\_part = Vt\_all * \frac{Nall}{Nactive}$$

Where

Vt_part is the NLR inner threshold setting used with some group members deactivated

Vt_all is the NLR inner threshold setting configured for the group with all members operating

Nall is the total number of members in the group

Nactive is the number of members active in the group (that is, the number of members not faulted nor deactivated intentionally)

Nall and *Nactive* are determined automatically from the group configuration parameters. No additional programming or configuration is required.

Since the available thresholds are quantized to multiples of 0.5% of the output voltage set-point, the next higher available threshold is used if the result of the above formula is fractional.

When properly configured, the non-linear characteristic of the Zilker Labs integrated controllers allows the flexibility of controlling the response of the regulator to load transients without the penalty of high power consumption or complex coded algorithms in the controller. With simple threshold and correction time parameters, this approach can achieve the regulation requirements of virtually all high-density logic devices. This degree of flexibility can give system designers the capability to make advantageous choices among regulation budgets, power consumption, and regulator size.

Appendices

Additional information on the operation of NLR is available in the following appendices. Also included are some worksheets which may be useful in defining the requirements of a particular application.

Appendix A – Transient Definition Worksheet Example

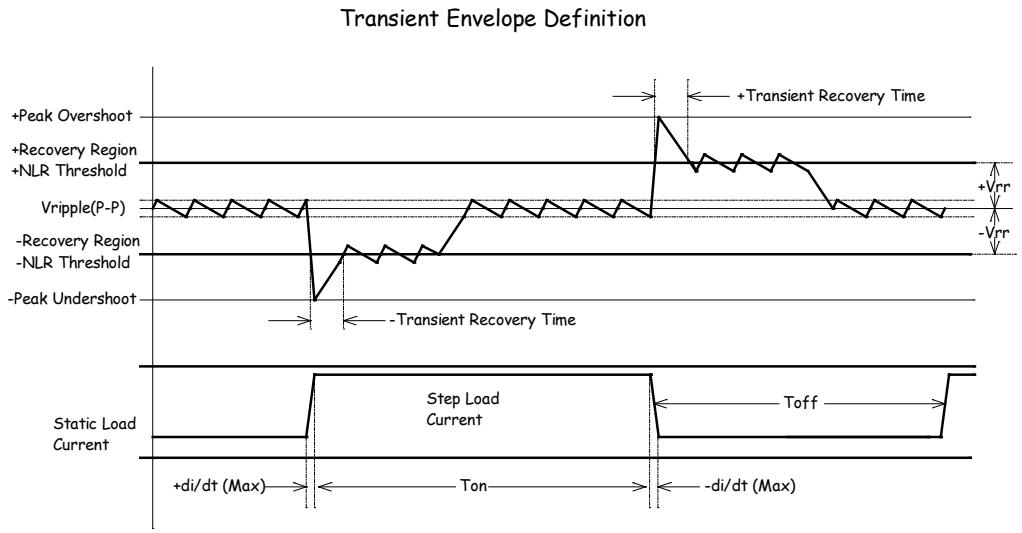

Figure 8. Transient Envelope

Transient Envelope Definitions and Boundary Conditions

Static peak to peak ripple = 1% of rated output voltage unless stated otherwise

Step load current = periodically changing load current (25% of maximum static load current)

Recovery Region (Vrr) = programmed NLR thresholds typically 1.5 to 2% of rated output voltage

Peak overshoot (Vp) = peak output voltage response to the specified dynamic load, 2 to 3% of rated output voltage

Di/dt (Max) = maximum rate of rise and fall of the dynamic load current (2 to 5A/us)

Ton = time that dynamic load dwells at the maximum value (defined by customer)

Toff = time that dynamic load dwells at the minimum value (defined by customer)

NLR Threshold = programmed voltage threshold that causes NLR to activate (1.5 to 2%) of rated output voltage

Transient recovery time (Trr) = time it takes voltage to recover to NLR threshold

Static load current = load current that flows during Toff interval of dynamic load (0 to Imax-25%(Imax)

Table 4. Customer Requirement

Output Voltage			
	Min.	Typ.	Max.
Static Ripple (P-P)			
Iout (Max)			
Di/dt (A/us)			
Ton			
Toff			
Trr			
+Vp			
-Vp			
+Vrr			
-Vrr			

Example – Choosing Transient Settings

The PowerNavigator evaluation software provides access to the NLR_CONFIG command. The available parameters are shown in the following figure.

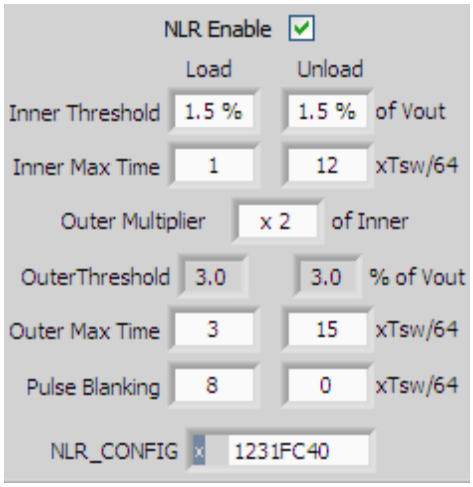

Figure 9. NLR_CONFIG Example

Using the example from AN2027 and AN2035, Parameters: Vg=12V, Vo=1.5V, L=0.68uH, C=2585uF, Tsw=3.33us, Q_{avg}=1.2

1) Determine the output ripple and noise peak to peak envelope. For this example, the noise is 32mVpp. Since the target output voltage is 1.5V, this means that the ripple is about +/-1.07%.

2) Determine the damping of the output filter. For this example, the Q_{avg} is 1.2. This guides the NLR mode to be used. Referring to Table 3, we choose the two-level mode.

3) **Inner Threshold (Load, Unload)** Set the inner thresholds. Since the measured noise and ripple is about +/-1.07%, we should be able to set inner NLR thresholds at 1.5% for both the load and unload levels.

4) **Inner Max Time (Load)** First calculate the expected correction current. For this example, the output filter characteristic impedance is

$$Z_o = \sqrt{L/C} = 16.22m\Omega$$

For the first threshold set at 1.5%, the expected correction current is

$$\Delta I_L = \Delta V_o / Z_o = 1.387A$$

Using

$$N_{load} = \frac{64 * \Delta I_L * L}{T_{sw} * (V_g - V_o)}$$

With ΔI_L=1.387A, we get $N_{load,ic}$=1.727. Round this value down to 1 for best response characteristic.

5) **Inner Max Time (Unload)** Following a similar procedure, we select the unloading inner correction time according to

$$N_{unload} = \frac{64 * \Delta I_L * L}{T_{sw} * V_o}$$

$N_{unload,ic}$=12.08

This value should be rounded down to 12.

6) **Outer Multiplier** Select the outer threshold multiplier. For most applications, a multiplier of 2 will be the best choice, resulting in outer thresholds at 3.0% in this case.

7) **Outer Threshold** The outer threshold is calculated using the Inner Threshold and the Outer Multiplier. In this case, 1.5% is multiplied by 2 for a result of 3%.

8) **Outer Max Time (Load)** Select the outer threshold correction time. Using the method in step 4, we find $N_{load,oc}$=3.454. Round down to 3.**Outer Max Time (Load)** Select the outer threshold correction time. Using the method in step 4, we find $N_{load,oc}$=3.454. Round down to 3.

9) **Outer Max Time (Unload)** The unloading outer correction time is in similar fashion to the Inner Max Time (Load) where $N_{unload,oc}$=15 (the maximum available value).

10) **Pulse Blanking (Load)** Set loading blanking value.

$$N_{bl} = N_{load}\frac{(Vg - Vo)}{Vo} = 1\frac{10.5V}{1.5V} = 7$$

From Table 2, the nearest available value is 8.

11) **Pulse Blanking (Unload)** Set the unloading blanking value.

$$N_{bul} = N_{unload}\frac{V_o}{V_g - V_o} = 12\frac{1.5V}{10.5V} = 1.714\,\mathrm{T}$$

he default blanking value of zero should be used for this voltage step-down ratio, since there is a minimum blanking value of 2-5 to accommodate deadtime.

12) **NLR Enable** Turn on the NLR function. Take the value generated, 0x1231FC40 and store in the device configuration stores as desired.

Refining NLR Settings

During initial development of a converter, NLR should be left OFF until basic aspects of the power system are established. These include regulation voltage, fault thresholds, and sequencing and tracking functions. When the basic regulation and protection measures are in place, then the NLR settings can be introduced and refined.

If the output voltage with the calculated NLR values is found to be oscillatory, there are three options after rechecking the calculations:

1) Reduce the correction time values on the loading or unloading thresholds, or both.

2) Increase the blanking time values to produce a less aggressive recovery.

3) Increase the inner correction thresholds if possible.

The most favorable results are found when the voltage recovery after a load step does not overshoot (or undershoot) the new voltage target (at the new load current).

Appendix B – Non-Linear Response (NLR) Characteristics

As part of the output voltage regulation loop, the Zilker Labs ZL2004, ZL2005, and ZL2006 families of devices utilize a non-linear secondary regulation mechanism for correcting large transients in output voltage without consuming large amounts of power in high-speed digital circuitry.

What is the meaning of "non-linear"?

This secondary regulation loop is, as the name implies, by its nature non-linear. In this implementation, the response of the regulation loop changes dramatically as certain voltage thresholds are reached. The use of predefined thresholds allows very well constrained determination of the voltage deviation when the correction values are properly established and the power filter is properly designed.

Defined threshold characteristic of NLR

The non-linear implementation implies certain characteristics of the response. The first characteristic of the non-linear implementation is that there are defined thresholds which govern the response of the regulation loop. A consequence of this characteristic is that a perturbation in the output voltage which does not cross one of these thresholds has a different result than an identical perturbation which does cross the threshold. As a result, the trajectory of the output voltage while returning to its quiescent value may be different for one deviation versus another.

Individuality characteristic of NLR

Another characteristic of the non-linear implementation is that the resulting waveforms cannot be precisely recreated in a repetitive fashion. This is due to the asynchronous relative timing of small perturbations in the output voltage (such as switching ripple) and large perturbations (such as load steps) in the output voltage signal. These signals are in general asynchronous. When the signals add together differently, the result can be different due to the non-linear thresholds noted in the first characteristic. The result is neither uncontrolled nor unstable; it is just not precisely repeatable.

Successive approach characteristic of NLR

A third characteristic of the non-linear loop is the tendency of the correction to be repeating in nature until the output voltage error is completely removed by a combination of the non-linear and linear loops. In this way, the output voltage never deviates far from its target. Since the circuit is taking successive small piecewise corrections to the output voltage error, the usual measurements applicable to a linear error recovery cannot be used. Instead of measuring the time constant of the recovery using the assumption of an exponential approach to the steady-state voltage, a better measure would be the integral of the absolute voltage deviation from target. The measure of settling time can be changed to be the time required to return to a value within an acceptable ripple range. (See Figure 8.)

The non-linear characteristic of the Zilker Labs integrated controllers allows the flexibility of controlling the response of the regulator to load transients without the penalty of high power consumption or complex coded algorithms in the controller. With simple threshold and correction time parameters, this approach can achieve the regulation requirements of virtually all high-density logic devices. This degree of flexibility can give system designers the capability to make advantageous choices among regulation budgets, power consumption, and regulator size.

References

[1] AN2033 – *Zilker Labs PMBus Command Set – DDC Products*, Zilker Labs, Inc., 2008

[2] AN2027 – *CompZL™ User's Guide*, Zilker Labs, Inc., 2008

Revision History

Date	Rev. #	
May 18, 2008	1.0	Initial release
June 2009	AN2032.0	Assigned file number AN2032 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read "Intersil and it's subsidiaries including Zilker Labs, Inc." No changes to app note content.

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