Unclamped Inductive Switching (UIS) Test and Rating Methodology

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Abstract

This application note will review the basic principles surrounding Unclamped Inductive Switching (UIS). It will examine what it is, the typical UIS ratings reflected on datasheets and how designers can properly use them. The main purpose of this application note then, is to supply designers with useful tools and information needed to appropriately deal with UIS related issues in their circuits.

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The Need for Power MOSFET Avalanche Ruggedness

Power MOSFETs inherently have extremely fast switching speeds. As a result, designers often use them in high speed switching circuits which take advantage of this capability.

Using MOSFETs in high speed switching circuits can lead to device stress not normally encountered in slower switching circuits. In fact, switching speeds may be so fast that at device turn-off, small parasitic inductance in the circuit can lead to significant overvoltage transients (Figure 1). This is due to the fact that when current through an inductor is abruptly turned off, the inductors magnetic field will induce a counter Electromagnetic Force (EMF) resisting the change. If the resulting voltage transient is large enough, the MOSFET may be forced into drain-to-source avalanche, $V_{(BR)DSS}$.

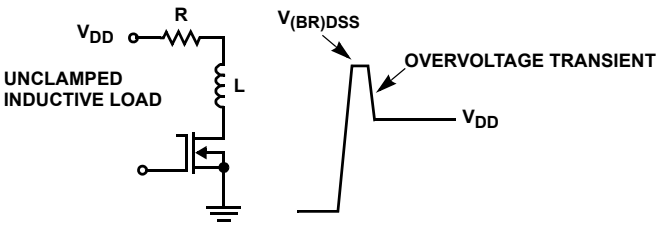

FIGURE 1. DRAIN-TO-SOURCE OVERVOLTAGE TRANSIENT DURING TURN-OFF

The peak overvoltage transient during turn-off can be determined by Equation 1.

$$V_{SPK} = L \bullet di/dt + V_{DD} \quad \text{(EQ. 1)}$$

Where:

V_{SPK} = Peak overvoltage transient voltage
L = Load inductance
di/dt = Rate of change of current at turn-off
V_{DD} = Supply voltage

According to Equation 1, the faster the switching speed and/or the higher the load current the more likely a device is to experience an overvoltage transient. Currents and switching speeds may be so high in some circuits that even low parasitic inductance may be enough to force devices into avalanche and possible device destruction.

Due to their inherently fast switching speeds, it is clear that power MOSFETs need to be designed and manufactured to insure that they have adequate avalanche ruggedness for today's high performance circuits.

Avalanche Ruggedness Test Method

The avalanche ruggedness of a device can be measured using a test circuit that performs an Unclamped Inductive Switching (UIS) function like the one shown in Figure 2. This type of circuit mimics the actual application where unclamped inductive loads are present. A device is considered rugged if it survives the test at the specified test conditions. Intersil “KGF” MOSFETs are 100% avalanche tested.

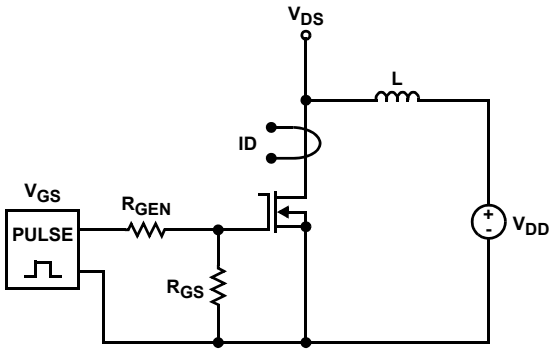

FIGURE 2. UIS TEST CIRCUIT

The operation of this test circuit is as follows:

1. At time zero, the input gate drive is turned on.
2. The MOSFET then switches on and ID current rises to the desired test current at the rate defined by Equation 2.

$$di/dt = \frac{V_{DD}}{L} \quad \text{(EQ. 2)}$$

3. Once the desired test current is reached, the gate drive is switched off, which abruptly turns off the MOSFET. Since the inductive load current cannot change instantaneously, the EMF of the inductor drives the MOSFET into drain-to-source avalanche (Figure 3).

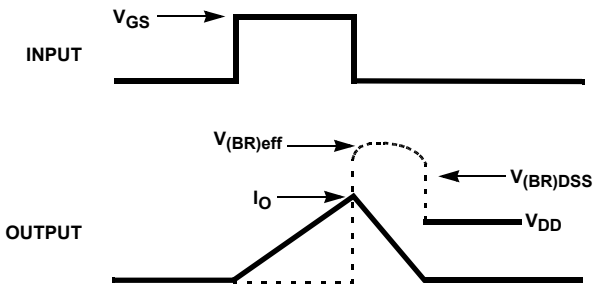

FIGURE 3. UIS WAVEFORMS

The critical equations resulting from this UIS test circuit are shown in Equations 3 through 6:

$$V_{(BR)eff} = 1.3L \bullet \text{Rated } V_{(BR)DSS} \quad \text{(EQ. 3)}$$

$$t(av) = \frac{(I_O \bullet L)}{(V_{(BR)eff} - V_{DD})} \quad \text{(EQ. 4)}$$

$$EAS = 1/2 \bullet I_O \bullet V_{(BR)eff} \bullet t(av) \quad \text{(EQ. 5)}$$

or

$$EAS = 1/2 \bullet L \bullet I_O^2 \bullet \frac{V_{(BR)eff}}{(V_{(BR)eff-VDD})} \quad \text{(EQ. 6)}$$

Where:

$V_{(BR)eff}$ = Effective drain-to-source breakdown voltage at peak discharge current. Note that $V_{(BR)eff}$ is much higher than the device's $V_{(BR)DSS}$ rating found on datasheets. This is because:

1. Device manufacturers guard-band their specifications.
2. The UIS avalanche current is much higher than that specified for $V_{(BR)DSS}$ and $V_{(BR)DSS}$ increases with current.

3. The device heats up during UIS and $V_{(BR)DSS}$ increases with temperature. A value of 1.3 * $V_{(BR)DSS}$ has been found to be a good rule of thumb for $V_{(BR)eff}$.

t(av) = Time in avalanche
EAS = Energy in avalanche, single pulse
I_O = Peak current being discharged
L = Load inductance
V_{DD} = Supply voltage

Another commonly used test circuit for UIS is shown in Figure 4. Its advantage over the previously described test circuit is that it switches out the V_{DD} supply during avalanche by use of a High Speed Switch (HSW).

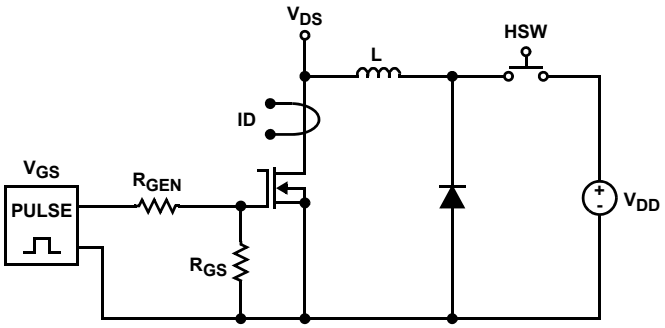

FIGURE 4. MODIFIED UIS TEST CIRCUIT

By switching out the supply voltage during device avalanche, two significant advantages are made available. First, the user can increase the V_{DD} supply beyond the MOSFET's maximum rated V_{DS}. This speeds up the inductors initial charge ramp time leading to overall faster test times as well as less device on-state time and therefore less self heating of the device prior to avalanche. Secondly, the UIS test circuit calculations are simplified to the following in Equations 7 and 8:

$$t(av) = \frac{(I_O \bullet L)}{(V_{(BR)eff})} \quad \text{(EQ. 7)}$$

$$EAS = 1/2 \bullet L \bullet I_O^2 \quad \text{(EQ. 8)}$$

Both test circuits shown in Figures 3 and 4 are industry recognized test circuits for UIS. They conform to both JEDEC standard No. 24-5 and MIL-STD750D method 3470.2.

Due to the advantages noted, Intersil uses the test circuit shown in Figure 4. However, actual application circuits used by designers do not usually switch out the V_{DD} supply during avalanche. Thus, the proper circuit equations to be used by designers are generally those resulting from the test circuit shown in Figure 3.

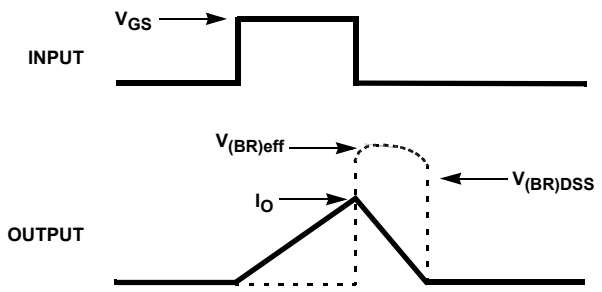

FIGURE 5. MODIFIED UIS TEST CIRCUIT WAVEFORMS

Datasheet Avalanche Ratings

MOSFET manufacturers generally provide some form of UIS avalanche ratings on their datasheets to inform the customer of a devices capability to withstand inductively induced overvoltage spikes. The UIS specifications supplied by Intersil and covered in this application note are as follows:

- Energy in Avalanche, Single pulse (EAS)
- Current in Avalanche, Single pulse (IAS)
- EAS vs starting junction temperature
- Energy in Avalanche, Repetitive pulse (EAR)

Single Pulse Avalanche Ratings

UIS ratings for MOSFETs originated in the mid 1980's and have since taken the form of specifying the amount of energy or Joules a device can safely handle in avalanche resulting from an inductive load. The EAS (Energy in Avalanche, Single pulse) rating was developed and is now displayed on most manufacturers power MOSFET datasheets.

Many manufactures specify EAS at the continuous current rating of the device. Since measured EAS capability of a MOSFET is inversely proportional to the avalanche current (Figure 6), the reasoning is that the continuous current rating of a device is considered the worst case condition. This would, in fact, be the case if designers always use the device at or below this value. The problem with this type of rating however, is it may not be adequate for many of today's circuits.

In high performance circuits, designers routinely push devices to extreme conditions of both current and switching speed. For example, in order to achieve high currents in certain applications, designers will parallel MOSFET devices. The total switched current in this type of arrangement may be many times the continuous current rating of any one single device being paralleled. Having said that, it should be noted that MOSFETs connected in parallel do not equally share current when they are avalanched. This is different than when operating them in a conduction state. In avalanche, the device with the lowest breakdown voltage or with the faster switching time will go into avalanche first and sink most if not all of the total switched current. The resulting stress in avalanche for that particular device is therefore much higher than it would have experienced if it had been avalanched at the lower value of a continuous current rating.

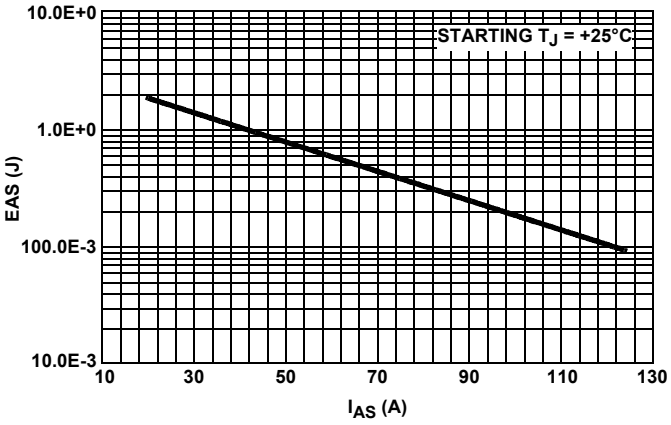

FIGURE 6. MEASURED EAS vs I_{AS}

To provide customers with a usable high current avalanche specification, Intersil includes a high current IAS (Current In Avalanche, Single pulse) rating on datasheets in the Absolute Maximum Ratings table. The I_{AS} value stated on the datasheet is much higher than the continuous current rating. It is the absolute highest current the device can safely handle in avalanche.

To aid the designer in determining a device's EAS or I_{AS} capability over a range of avalanche conditions, Intersil also includes an Avalanche Safe Operating Area (ASOA) curve on datasheets. This allows designers to know under a wide range of currents and inductances whether or not the device is exceeding its avalanche capability (Figure 7). The curve is constructed so as to insure that the device will never exceed its actual EAS capability nor push the device beyond its known reliable and safe mode of operation. The safe area of operation is the area under the curve.

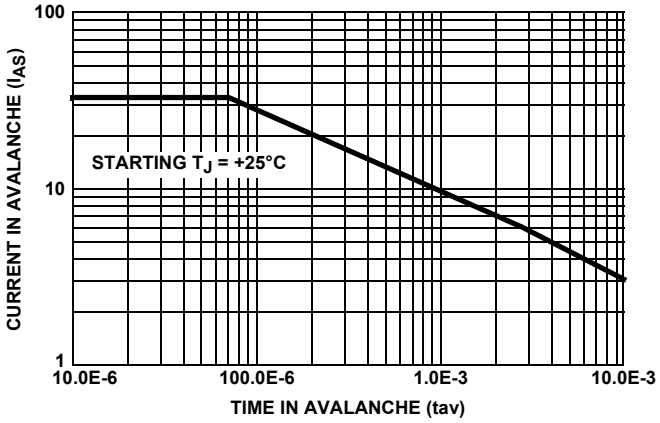

FIGURE 7. AVALANCHE CURRENT vs TIME

There are several ways a designer can use the ASOA curve.

1. The designer can directly measure the current and time in avalanche and compare it to the ASOA curve shown on the datasheet.
2. Based on known load inductance, V_{DD} supply voltage and the current being switched, the designer can use Equation 2 on page 2 and solve for time in avalanche (dt). Then simply compare the IAS and tav values to the ASOA curve provided on the device's datasheet to insure safe operation.
3. The designer can use I_{AS} and tav points from the ASOA curve line to calculate EAS vs I_{AS} capability using Equation 5.

EAS vs Starting Junction Temperature

Another critical component to a complete UIS rating is the devices starting junction temperature. Actual EAS capability is inversely proportional to a devices starting junction temperature. Measured UIS device failure has been shown to generally occur when the devices silicon has reached its intrinsic temperature, typically around +380°C. During a UIS failure, some location on the silicon has reached this intrinsic temperature and a short occurs at that location, which destroys the device. Since the power generated by UIS pulse raises the devices junction temperature, any starting junction temperature above +25°C will reduce its EAS capability.

Even though actual UIS failure occurs at a silicon temperature of roughly +380°C, the devices junction temperature should always be kept at or below its rated T_{JMAX} as shown on the device's datasheet. This insures good long term reliability. To help the designer insure this, Equation 9 is provided. This equation allows a designer to derate a devices EAS capability from starting junction temperatures of +25°C up to the devices rated T_{JMAX}.

$$EAS(T_{JSTART}) = EAS(+25°C) \bullet \left[\frac{(T_{JMAX} - T_{JSTART})}{(T_{JMAX} - 25°C)}\right]^2 \quad \text{(EQ. 9)}$$

Using this equation, you will find that the devices EAS capability is derated to zero when the starting junction temperature reaches T_{JMAX}. This is done to insure good reliability over time. Operating the device at higher junction temperatures may reduce the long term reliability of the device.

Energy in Avalanche, Repetitive Pulse (EAR)

Some power switching circuits are designed such that they avalanche the MOSFET repetitively. Therefore, device manufacturers need to be able to provide designers with a way to know if they are exceeding device capability and reliability in such cases or not. The industry term established for this capability is called Energy in Avalanche Repetitive pulse (EAR).

The EAR capability of a MOSFET is basically a transient thermal parameter and can be calculated using the devices own transient thermal response curve.

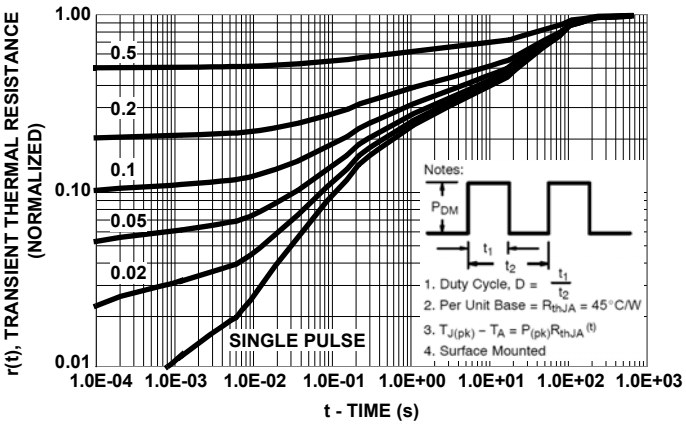

FIGURE 8. TRANSIENT THERMAL RESPONSE CURVE

A Transient Thermal Response curve like the one shown in Figure 8 is derived using rectangular power pulses. A UIS power pulse however, is not a rectangular power pulse, it is triangular (see Figure 9). Therefore, this difference must be dealt with in order to properly use a transient thermal response curve for EAR calculations.

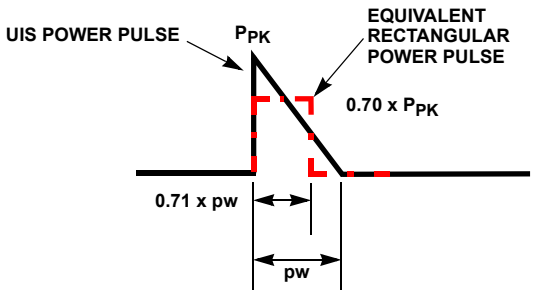

FIGURE 9. POWER PULSE CONVERSION

The well established method to convert a triangular power pulse into to a rectangular one is as follows:

$$P(rect) = 0.7 \bullet P_{PK} \quad \text{(EQ. 10)}$$

$$pw(rect) = pw \bullet 0.71 \quad \text{(EQ. 11)}$$

Where:

P(rect) = Equivalent rectangular power

pw(rec) = Equivalent rectangular pulse width

P_{PK} = Peak triangular power

pw = Triangular pulse width

The key to such a conversion is that the energy of the pulse in both the triangular and equivalent rectangular pulse is roughly the same.

With this understanding in mind, an EAR can be determined for the MOSFET at any pulse width and duty cycle such that the device does not exceed its T_{JMAX} as shown on the datasheet. Equation 12 is used to make this determination:

$$EAR = \left[\frac{(T_{JMAX} - T_X)}{(r(t)eff \bullet R_{\theta JX})}\right] \bullet pw(rect) \quad \text{(EQ. 12)}$$

Where:

T_X = Reference temperature (i.e., ambient or ball)

r(t)eff = Normalized transient thermal resistance at an equivalent rectangular pulse width of pw • 0.71

R_{THJX} = thermal resistance junction to reference point (i.e., ambient or ball).

For example, under the following conditions what is the devices EAR capability?

Max T_J = +150°C
Ambient Temperature = +25°C
$R_{\theta JA}$ = +45°C/W
pw = 200µs
DT = 20%

The r(t)eff would be the r(t) for a pw(rect) of 142µs (200µs • 0.71) with a duty cycle of 20%. Using the Transient Thermal Response curve shown in Figure 8 for this example, r(t)eff = 0.2.

Therefore, the devices EAR capability under these conditions is:

EAR = [(150°C - 25°C)/(0.2 • 45°C/W)] • 142µs
= 19.72mJ

If by using Equations 5 or 6 you find that the devices single pulse avalanche energy exceeds the calculated EAR capability, then the devices junction temperature during repetitive pulsing of this pulse will exceed T_{JMAX} as shown on the datasheet and therefore device reliability cannot be guaranteed.

Conclusion

This application note has covered basic UIS principles and examined typical UIS ratings reflected on Intersil datasheets. The necessary equations along with examples have been provided in order to show designers how to properly deal with UIS related issues in their circuits and to maintain good device reliability.

The following conditions must be satisfied in order to insure Intersil devices are operated within their safe area for UIS.

1. The devices IAS rating must never be exceeded.
2. The MOSFET must never operate outside the bounds of the ASOA curve.
3. The devices rated T_{JMAX} must never be exceeded.

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