

Reflow and PC Board Assembly Effects on Intersil FGA References

Introduction and Background

The Intersil Floating Gate Analog (FGA) technology utilizes a robust stored charge technology borrowed from a standard EEPROM process to produce a precise reference voltage. The stored voltage is the heart of a highly accurate precision voltage reference product. The resulting voltage reference has excellent characteristics which are unique in the industry; very low temperature drift (3ppm/°C), high initial accuracy, and extremely low supply current (<1µA). Also, the reference voltage is not limited to "magic" voltages obtained from Bandgap references or buried Zener diodes to achieve temperature drift cancellation

The floating gate storage cell requires two tunnel diodes to inject charge into a storage capacitor (see Figure 1). The tunnel diodes require high voltage, >10V, to turn on and when unbiased have extremely high impedance and essentially zero charge leakage.

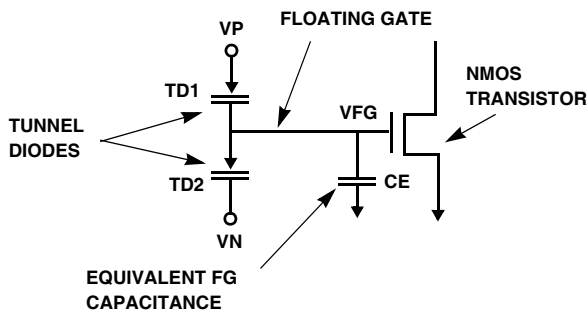


FIGURE 1. FLOATING GATE CELL

The actual voltage reference circuit contains two of the floating gate capacitors and an op amp (see Figure 2). One capacitor sets the common mode voltage and the other sets the output reference voltage. The switches shown in Figure 2 are the tunnel diodes and the V_{CM} and V_{REF} shown are external voltages applied to program the cell at factory test. The output reference voltage is the difference between the common mode and reference capacitors, which allows output voltage flexibility and adds temperature compensation.

The resulting circuit is highly stable, and the supply current is entirely dependent on the op amp, which can be extremely low current (<1µA) for low power or higher current for low noise applications.

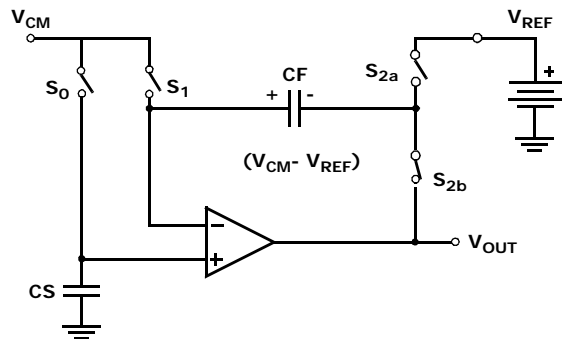


FIGURE 2. FLOATING GATE REFERENCE CIRCUIT SHOWN IN STABLE V_{OUT} STATE

Thermal Considerations

FGA references have thermal hysteresis, similar to bandgap or other reference technologies. As the packaged device goes through a temperature cycle, the package and die will permanently change shape, very slightly, but enough to affect the electrical properties. Multiple cycles will result in different shifts, and after a few cycles the overall change from the initial voltage stabilizes. The data sheet provides a thermal hysteresis specification for temperature excursions within the absolute maximum temperature range. For the ISL21009, for example, there is a typical 50ppm drift over the specified range (-40°C to +125°C), (see Figure 3). There is no maximum specified since the device cannot be tested over multiple cycles at the factory.

The amount of hysteresis shift can be controlled by PC board mounting. It has been proven experimentally that placing the voltage reference package near the PCB edge, especially the shortest edge, or in a corner, will minimize hysteresis effects due to the increased stiffness of the board. A PC board cutout will greatly reduce package stress and hysteresis shift as well.

Board Assembly Considerations

FGA reference PC board mounting exposes the device to temperatures that are outside the recommended operating range and absolute maximum sustained temperature exposure, but within the maximum temperature for the package. The resulting temperature cycle is more extreme than the normal thermal hysteresis stated on the data sheet, and therefore the output voltage shift can exceed the typical thermal hysteresis as well.

To characterize this effect, Intersil tested the ISL21009-50 (5V output) for reflow shift. 10 devices were placed on a 2-sided FR-4 PC board and then exposed to multiple assembly reflow cycles. The results

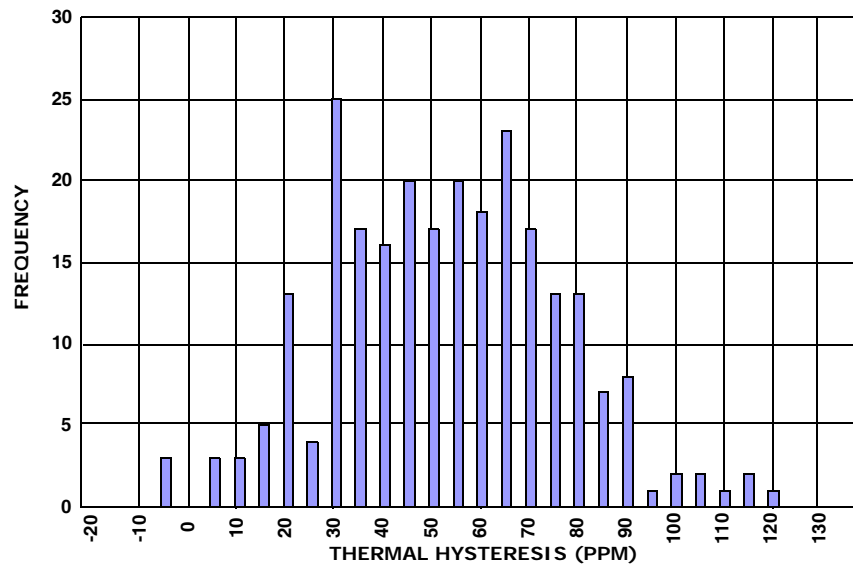


FIGURE 3. ISL21009 TYPICAL THERMAL HYSTERESIS

are shown in Table 1. The average reflow drift is approximately 300 μ V after the first reflow and 400 μ V at each successive reflow. This indicates the thermomechanical effects reach a maximum at some point, with an upper limit on the amount of shift. Although this data shows a consistent positive overall shift, it is possible at any cycle to have the V_{REF} voltage shift negative as well. It should be noted that any shift in the V_{REF} output voltage can place it outside of the specified accuracy range as stated on the data sheet.

TABLE 1. SHIFT AFTER MULTIPLE REFLOW CYCLES (μ V)

| UNIT | AFTER 1 REFLOW | AFTER 2ND REFLOW | AFTER 3RD REFLOW | AFTER 4TH REFLOW |
|------|----------------|------------------|------------------|------------------|
| 1 | 50 | 209 | 204 | 274 |
| 2 | 365 | 521 | 458 | 414 |
| 3 | 320 | 459 | 408 | 410 |
| 4 | 273 | 430 | 397 | 418 |
| 5 | 295 | 430 | 360 | 349 |
| 6 | 437 | 579 | 574 | 507 |
| 7 | 378 | 558 | 574 | 521 |
| 8 | 300 | 451 | 481 | 468 |
| 9 | 295 | 416 | 366 | 376 |
| 10 | 187 | 324 | 326 | 318 |

Intersil guarantees that the FGA reference meets the data sheet specification when shipped to the customer, which is consistent with other semiconductor suppliers. Exposure to assembly thermal cycles are outside what can be covered by the data sheet. Note that this is true for all voltage references of various technologies. Intersil has tested other precision voltage references from various suppliers and the results indicate that output voltage shift after reflow is a common trait. Test results are shown in Figure 4.

See Table 2 for a summary of initial accuracy and thermal hysteresis specifications and two-pass reflow test results for these precision reference devices. The right-most column compares the final tested voltage versus the data sheet specification. One device is clearly out of spec and others are very close. Design engineers must take this into account when considering the reference voltage accuracy after assembly.

To minimize assembly reflow shift, reduce the peak reflow temperature below +260°C if possible. Also, a customer may wish to hand solder the voltage reference to the PC board after the assembly process. Careful hand soldering will greatly reduce the peak temperature and exposure time for the package and thus reduce the post-assembly voltage shift. An additional advantage of hand soldering is that, if X-ray inspection is required, the FGA reference will not be subjected to that source of output voltage shift (see the related application note at www.intersil.com).

If there are no physical ways to reduce assembly shift, the customer still has the option of trimming the voltage reference after assembly and at final test. The ISL21007 and ISL21009 devices have a trim pin that allows $\pm 2.5\%$ trim range which is plenty to compensate for these shifts. Please refer to TB473, "Adjusting the ISL21007, ISL21009 V_{OUT} Using the ISL95810", for more information on FGA reference trimming.

Conclusions

The FGA voltage reference provides excellent low power performance and accuracy. The design engineer must be aware of all the thermal aspects of device shift during assembly and normal operation, and plan their design accordingly. With proper planning and design the FGA can yield a highly accurate and stable reference voltage.

TABLE 2. PRECISION VOLTAGE REFERENCE ACCURACY AND HYSTERESIS SPECS AND REFLOW RESULTS

| PART | V _{OUT} | INITIAL ACCURACY | | THERMAL HYSTERESIS | | OUTPUT VOLTAGE RANGE | | TWO PASS REFLOW RESULTS | | ERROR FROM IDEAL VALUE AFTER REFLOW |
|----------|------------------|------------------|-----|--------------------|-------|----------------------|--------|-------------------------|--------------------|-------------------------------------|
| | | % | mV | ppm | mV | MIN | MAX | V _{INITIAL} | V _{FINAL} | mV |
| Mfr X1 | 5.0 | 0.05% | 2.5 | N/A | N/A | 4.9975 | 5.0025 | 4.999365 | 4.999245 | -0.755 |
| Mfr X2 | 5.0 | 0.05% | 2.5 | N/A | N/A | 4.9975 | 5.0025 | 4.999742 | 4.999614 | -0.386 |
| Mfr Y1 | 5.0 | 0.04% | 2.0 | 20 | 0.100 | 4.9980 | 5.0020 | 5.000663 | 5.002391 | 2.391 |
| Mfr Y2 | 5.0 | 0.04% | 2.0 | 20 | 0.100 | 4.9980 | 5.0020 | 5.000445 | 4.999643 | -0.357 |
| Mfr Z1 | 2.5 | 0.01% | 0.5 | 15 | 0.038 | 2.4995 | 2.5005 | 2.500451 | 2.500225 | 0.225 |
| Mfr Z2 | 2.5 | 0.01% | 0.5 | 15 | 0.038 | 2.4995 | 2.5005 | 2.500297 | 2.499862 | -0.138 |
| Mfr W | 5.0 | 0.02% | 1.0 | 75 | 0.375 | 4.9990 | 5.0010 | 5.000790 | 5.000978 | 0.978 |
| ISL21009 | 5.0 | 0.01% | 0.5 | 50 | 0.250 | 4.9995 | 5.0005 | 4.999945 | 5.000396 | 0.396 |

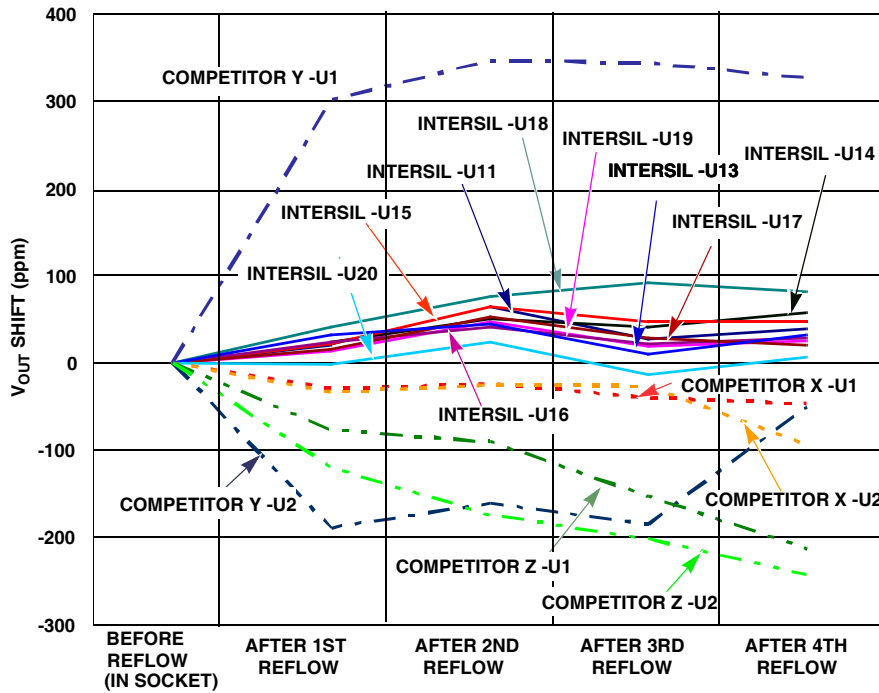


FIGURE 4. REFLOW SHIFT RESULTS FOR INTERSIL FGA AND OTHER REFERENCE TECHNOLOGIES

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