**Introduction**

As high-efficiency ultra-bright white LEDs come down in cost, they are approaching cost parity with conventional mercury vapour, HID quartz metal halide and high/low pressure sodium lighting on a cost per lumen basis. They are becoming viable replacements in industrial and commercial lighting applications. However, there are significant differences between conventional lighting sources and LEDs in terms of voltage and current operating requirements. In particular, LEDs require a constant current source from a low DC voltage source, but they must also operate from the AC mains. Just as conventional lighting sources require a ballast, LED lighting sources have an analogous circuit. This Application Note discusses techniques for powering LEDs directly from the AC mains, not only to develop the requisite voltage and current, but also to deliver power from the AC mains with near unity power factor while using off-the-shelf constant frequency PWM controllers. The major difference in the control circuitry between a conventional DC/DC converter and the LED ballast is that the output current, rather than the output voltage, is the controlled parameter.

**Requirements**

To achieve light intensity comparable to conventional commercial and industrial lighting, multiple LEDs must be used. The LEDs may be connected in parallel or series, or a combination of both. Depending on the light intensity required, the number of required LEDs could range from a few to hundreds. Each LED may require, depending on its characteristics, between 300mA and 1000mA of DC current at 3V to 4V to provide up to 175 lumens of light output\(^1\). A typical high pressure sodium street lamp bulb consumes 150W and produces about 15,000 lumens\(^2\). Using presently available LEDs, an equivalent intensity LED "bulb" would require up to 150 LEDs and consume somewhat more power.

We desire a simple low cost power supply (LED ballast) that converts the AC mains input to a constant current DC source. Furthermore, the power must be delivered from the source with near unity power factor*. 

**The LED Ballast**

Fortunately, there are many power supply topologies suitable for this application. Virtually any topology having a series inductor is suitable. This would include Boost, Buck-Boost, SEPIC, CUK, and Flyback converters, to name a few. The only requirements being that the inductor current must reduce to zero during a portion of the switching cycle, i.e., the converter must operate in either discontinuous conduction mode (DCM) or critical conduction mode (CrCM), and the converter must be operated with a constant On-Time control. The reason for the restrictions is to achieve unity power factor from the AC mains. When operated as described, the peak (and average) inductor current will track the input voltage waveform. The input current will be sinusoidal and in-phase with the AC input voltage.

From Faraday’s Law and the definition of inductance, we have Equation 1:

\[
V = L \frac{di}{dt}
\]

(EQ. 1)

Since the switching period of the converter is very short compared to the AC line frequency, we can assume the voltage applied to the inductor is constant during a single switching cycle. If \(V\) and \(L\) are constant, then \(\Delta I\) and \(\Delta T\) may be substituted for \(di\) and \(dt\), respectively. Furthermore, since this is a constant On-Time control law, \(T_{ON}\) may be substituted for \(\Delta T\). Rearranging and solving for \(\Delta I\) yields Equation 2:

\[
\Delta I = \frac{V}{L} \cdot T_{ON}
\]

(EQ. 2)

Since \(T_{ON}\) and \(L\) are constant, \(\Delta I\) varies in proportion to the applied voltage, \(V\). The AC input voltage is applied to the inductor, and as it varies, \(\Delta I\) varies in proportion. Since the converter is operated in either DCM or CRCM, the inductor current always starts each switching cycle at zero current. Therefore, \(\Delta I\) is the peak inductor current. Each switching cycle of the converter generates a triangular inductor current waveform that conforms to the envelope of the rectified AC input voltage waveform.

*Power factor is the ratio of real power to apparent power (W/VxA, where W = watts, V = RMS voltage, A = RMS current). Unity power factor implies that the load has no reactive (inductive or capacitive) component and appears purely resistive.
Figure 1 depicts the input voltage and current waveforms for a converter operating in DCM with constant On-Time control. The switching frequency of the converter has been reduced to 2kHz to illustrate the input current waveform on a time scale appropriate for viewing both waveforms simultaneously.

One consequence to achieving near unity power factor is the energy delivered from the AC mains is not constant, but varies with the sinusoidal AC input voltage. The LED load, however, requires a constant DC current and voltage. Some LED driver solutions address this problem by using a second DC/DC converter to regulate the current. This is entirely unnecessary. A single stage converter is fully capable of meeting the requirements. The only penalty is a small amount of rectified line frequency ripple on the output voltage of the converter, the magnitude of which is inversely proportional to the value of output capacitance. This topic will be further discussed later.

We have established that the converter must be operated using a constant On-Time control law, but how is the current through the LEDs regulated to achieve the desired intensity and/or color temperature? The answer is the On-time is not truly constant.

If the On-time is modulated slowly, the On-time over an AC half-cycle will be virtually constant, but can still be slowly changed over time to regulate the current through the LEDs. This requires that the LED current control loop have a bandwidth significantly less than the frequency of the rectified AC input, or about 20Hz to 30Hz.

Three of the many converter topologies suitable for LED driver applications will be discussed in detail. The methods discussed are easily adapted to other topologies as the actual control circuitry is not topology dependent. One control circuit can be used for all single stage LED driver topologies.

The Boost Converter

The simplest LED ballast is based on a conventional boost converter, depicted in Figure 2.

The boost converter is useful for driving a large series string of LEDs. The only requirement being that the voltage applied to the LEDs must be higher than the peak of the AC input voltage. A boost converter cannot produce an output voltage lower than its input. For example, if the input voltage is the nominal 120VAC common in North America, it has an operating range of 90VAC to 140VAC and a maximum peak voltage of 198V (\(\sqrt{2} \times 140\)). The LED string must have a sufficient quantity of LEDs in series such that the voltage drop across the string is greater than the peak voltage of 198V. A typical forward voltage drop for a white LED is 3.5V, suggesting a minimum string of 58 LEDs. Once variation of forward voltage drop with temperature and other factors is taken into account, the actual quantity of LEDs required may be somewhat higher. If too few LEDs are used, the converter will not be able to regulate the LED current.

The critical components of the boost converter are the inductor, L, the primary power switch, Q, the rectifier D, and the output capacitance, COUT.
capacitor, C_{OUT}. Each of these components must be selected for the current and voltage stress experienced in the application.

The inductor must be selected for both peak current and RMS current rating to avoid saturation and excessive power dissipation.

The voltage and current waveforms for a boost converter operating in DCM are illustrated in Figure 3.

The switching period $T_s$ is divided into three subintervals known as $T_{ON}$, $T_{OFF1}$, and $T_{OFF2}$. $T_{ON}$ is the time period that switch Q is conducting, also known as the On-time. $T_{OFF1}$ is the time period during which the inductor current ramps down to zero after switch Q is turned off, and $T_{OFF2}$ is the remainder of the switching period where the inductor current is zero.

The peak inductor current can be estimated from Equation 3.

$$I_{pk} = \frac{\pi}{2} \sqrt{\frac{2(V_{OUT} - V_{IN})T_{ON}L}{V_{OUT} - V_{IN}}}$$  \hspace{1cm} (EQ. 3)

where $V_{OUT}$ is the output voltage, $V_{IN}$ is the peak input voltage, $T_s$ is the switching period, $I_{OUT}$ is the output current, and $L$ is the boost inductor value. Equation 3 assumes the inductor current remains discontinuous (DCM operation). The power switch, Q, and diode, D, are treated as ideal elements. The RMS current through the inductor can be calculated from Equations 4 through 6.

$$I_{rms} = \frac{2}{\pi} I_{pk} \sqrt{\frac{T_{ON} + T_{OFF1}}{3T_s}}$$  \hspace{1cm} (EQ. 4)

where:

$$T_{ON} = \sqrt{\frac{2T_{S}I_{OUT}L(V_{OUT} - V_{IN})}{V_{IN}}}$$  \hspace{1cm} (EQ. 5)

and:

$$T_{OFF1} = \sqrt{\frac{2T_{S}I_{OUT}L}{V_{OUT} - V_{IN}}}$$  \hspace{1cm} (EQ. 6)

where $\overline{V_{IN}}$ is the average rectified input voltage. Equations 5 and 6 represent the average values of $T_{ON}$ and $T_{OFF1}$, respectively. While $T_{ON}$ is essentially constant during an AC half-cycle, $T_{OFF1}$ will vary considerably over the same time period. The instantaneous value of $T_{OFF1}$, $T_{OFF1}'$, may be calculated from Equation 7.

$$T_{OFF1}' = \frac{V_{IN} \cdot T_{ON}}{V_{OUT} - V_{IN}}$$  \hspace{1cm} (EQ. 7)

The inductor value must be correctly sized so that the converter remains in DCM operation over all operating conditions. This criteria can be met provided the combined duration of $T_{ON}$ and $T_{OFF1}$ are less than the switching period, $T_s$. Summing Equations 5 and 6 and setting the result to be less than $T_s$ yields Equation 8.

$$L < \frac{T_{S}(V_{OUT} - V_{IN})}{2I_{OUT}^2 V_{IN}^2}$$  \hspace{1cm} (EQ. 8)

The value of inductance determined by Equation 8 is the maximum allowed inductance and must be calculated using the minimum output voltage, the maximum instantaneous input voltage, and maximum output current over a complete AC half-cycle.

The RMS current through switch Q is shown in Equation 9:

$$I_{Q(RMS)} = \frac{2}{\pi} I_{pk} \sqrt{\frac{T_{ON}}{3T_s}}$$  \hspace{1cm} (EQ. 9)

The factor of $2/\pi$ averages the RMS value over a complete AC half-cycle. The voltage ratings of the power switch, Q, diode D, and output capacitor, C_{OUT}, must be at least as high as the converter output voltage plus allowance for transients and design margin. The peak currents through Q and D are the same as was obtained for the inductor. The average current through diode D is the output current $I_{OUT}$. The ripple current rating for C_{OUT} is an involved calculation. There is a high frequency component at the switching frequency, a low frequency component at the rectified AC frequency, and a DC component due to the load. An estimate may be calculated using Equation 10.

$$I_{RMS(C_{OUT})} \approx \sqrt{\frac{T_{OFF1}}{T_s}} \left(\frac{\Delta I_L^2}{3} - I_{OUT} \Delta I_L\right) + I_{OUT}^2$$  \hspace{1cm} (EQ. 10)

where:

$$\Delta I_L = \frac{V_{IN} T_{ON}}{L} = \frac{V_{OUT} - V_{IN}}{L} T_{OFF1}$$  \hspace{1cm} (EQ. 11)

Evaluating $\Delta I_L$ at the maximum instantaneous input voltage will result in a conservative estimate of the ripple current.
Evaluating $\Delta I_L$ at the average or RMS input voltage will somewhat underestimate the ripple current.

The input capacitor, $C_{IN}$, must be sufficiently small so that it tracks the (unfiltered) rectified AC voltage. It must completely charged and discharged in-phase with the rectified AC input during each half-cycle. If this requirement is not met, the input current waveform will be distorted and power factor quality will be compromised.

The boost topology provides better power factor performance when operated in critical conduction mode (CrCM) rather than discontinuous conduction mode. Since the inductor current ramps from $I_{pk}$ to zero in proportion to the difference between the input voltage and the output voltage, the average inductor current does not track the input voltage as well. This behavior becomes obvious if the output voltage is nearly equal to the peak of the AC input voltage. The inductor current ramps down more slowly as the instantaneous difference between the input and output voltage decreases. As the output voltage is further increased above the peak input voltage, the distortion is reduced. Figure 4 shows this effect. Operating in CrCM eliminates the distortion because there is no $T_{OFF2}$ period.

The SEPIC converter is more complicated than the boost converter, and therefore requires some discussion of its operation.

Referring to Figure 5, components L1 and L2 cannot have a steady state DC voltage impressed across them, or saturation would occur. Therefore, the average voltage across each inductor must be zero. This result implies the voltage across C1 must be equal to the rectified AC input, $V_{IN}$. Likewise, the DC current through C1 must be zero for steady state operation. Since the DC current through C1 must be zero, the output current, $I_{OUT}$, can only result from current flowing in L2. Therefore, the average current through L2 must be equal to the output current, $I_{OUT}$. Therefore:

$$\bar{V}_{L1} = 0 \ V_{DC} \quad (EQ. 12)$$
$$\bar{V}_{L2} = 0 \ V_{DC} \quad (EQ. 13)$$
$$\bar{I}_{C1} = 0 \ A_{DC} \quad (EQ. 14)$$
$$\bar{V}_{C1} = V_{IN} \ V_{DC} \quad (EQ. 15)$$

In DCM operation, there are three time periods in each switching cycle designated as $T_{ON}$, $T_{OFF1}$, and $T_{OFF2}$ corresponding to the state of the inductor currents. In the SEPIC topology, the inductors are considered to be discontinuous when the sum of their currents is zero rather than when either inductor has zero current. This occurs when the voltages across the inductors collapse to zero.

During $T_{ON}$, the switch, Q1, is closed and the inductor currents ramp linearly to $I_{pk}$. ($I_{pk}$ will be different for L1 and L2 unless they have equal inductance.) $T_{OFF1}$ starts when switch Q1 opens and the inductor currents decrease in magnitude. $T_{OFF2}$ begins when the inductor currents sum to zero and ends when the next switching cycle begins.
During TON, the main switch is closed. The input voltage, \( V_{\text{IN}} \), is applied across L1. Since C1 has a steady state voltage equal to \( V_{\text{IN}} \), L2 also has \( V_{\text{IN}} \) applied across it during TON. Diode, D1, is reversed biased and blocking. The load current, I\(_{\text{OUT}}\), is entirely supplied by the output capacitor C\(_{\text{OUT}}\).

It should be noted that C1 is sufficiently large that the AC currents through it produce a negligible voltage change and the voltage across it remains essentially equal to \( V_{\text{IN}} \). During TON, when Q1 is conducting, both inductors have \( V_{\text{IN}} \) applied to them.

During TON, the voltage across each inductor is:

\[
V_{L1(\text{TON})} = L_1 \frac{\Delta I_1}{T_{\text{ON}}} = V_{\text{IN}} \quad \text{(EQ. 16)}
\]

\[
V_{L2(\text{TON})} = L_2 \frac{\Delta I_2}{T_{\text{ON}}} = V_{\text{IN}} \quad \text{(EQ. 17)}
\]

V\(_{\text{OUT}}\) appears across both inductors during TOFF\(_1\) so their flux-linkage (volt-second) change is again equal. Since the flux-linkage (volt-second) change for both inductors is identical during both TON and TOFF\(_1\), the inductor currents will ramp and decay at the same rate and become discontinuous at the same time.

Although the inductor currents may not be zero during TOFF\(_2\), there is no inductor current flowing to the output. I\(_{\text{OUT}}\) is supplied entirely by C\(_{\text{OUT}}\).

As noted earlier, the output current I\(_{\text{OUT}}\) is equal to the average current in inductor, L2. However, since current only flows to the output during TOFF\(_1\), the output current is also the sum of the average inductor currents during TOFF\(_1\). The output current, I\(_{\text{OUT}}\), can be expressed as Equation 20:

\[
I_{\text{OUT}} = \frac{V_{\text{OUT}} T_{\text{OFF1}}^2}{2 T_s} \left( \frac{1}{I_1} + \frac{1}{I_2} \right) \quad \text{(EQ. 20)}
\]

Solving for T\(_{\text{OFF1}}\) yields Equation 21:

\[
T_{\text{OFF1}} = \sqrt{\frac{2 T_s I_{\text{OUT}}}{\left( \frac{1}{I_1} + \frac{1}{I_2} \right) V_{\text{OUT}}}} \quad \text{(EQ. 21)}
\]

It should be noted that the value of T\(_{\text{OFF1}}\) in Equation 21 is the average value during an AC half-cycle.

Since the inductors are operating in steady state, \( \Delta I \) during T\(_{\text{ON}}\) and T\(_{\text{OFF1}}\) must be equal and opposite in magnitude for each
inductor. Equating $\Delta I$ during periods $T_{ON}$ and $T_{OFF1}$ yields Equation 22:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} T_{OFF1}$$  
(EQ. 22)

where $V_{IN}$ is the average input voltage since $T_{ON}$ is virtually constant over an AC half-cycle (to achieve high power factor). Since the switching frequency, $T_S$, is constant, $T_{OFF2}$ can be calculated from Equations 21 and 22, yielding Equation 23.

$$T_{OFF2} = T_S - T_{ON} - T_{OFF1}$$  
(EQ. 23)

When selecting the values of inductors $L1$ and $L2$, it is important to realize that they must operate in the discontinuous mode to maintain high power factor. Discontinuous operation occurs when $T_{ON} + T_{OFF1} \leq T_S$. Using this information combined with Equations 21 and 22 shows that the parallel combination of $L1$ and $L2$ must be less than the value indicated in Equation 24 for discontinuous operation to occur.

$$\frac{L1 L2}{L1 + L2} \leq \left(\frac{V_{IN}}{V_{IN} + V_{OUT}}\right)^2 T_S V_{OUT}$$  
(EQ. 24)

where $V_{IN}$ is the average minimum input voltage, $V_{IN}$ is the instantaneous maximum value of the minimum input voltage, and $V_{OUT}$ is the minimum output voltage.

Referring to Figure 6, the DC offset current that flows is the result of maintaining charge balance on the series capacitor, $C1$. By summing the charge into the capacitor during the three intervals $T_{ON}$, $T_{OFF1}$, and $T_{OFF2}$, the value of the DC offset current, $I_{DC}$ can be calculated. The average current $I_{C1}$ through the series capacitor, $C1$, must be zero.

$$\bar{I}_{C1} = 0 = \frac{V_{OUT} T_{OFF1}}{2 L1 T_S} - \frac{V_{IN} T_{ON}}{2 L2 T_S} + I_{DC}$$  
(EQ. 25)

Substituting for $T_{ON}$ and $T_{OFF1}$ using Equations 21 and 22, and solving for $I_{DC}$ yields Equation 26:

$$I_{DC} = \frac{L1 I_{OUT}}{L1 + L2} \left(\frac{V_{IN} V_{OUT}}{V_{IN}^2} - \frac{L2}{L1}\right)$$  
(EQ. 26)

where $V_{IN}$ is the average minimum input voltage, $V_{IN}$ is the instantaneous maximum value of the minimum input voltage, and $V_{OUT}$ is the minimum output voltage. It should be noted that $V_{IN}$ is not the instantaneous input voltage, but the input voltage corresponding to the peak of the AC input. This equation was derived using values averaged over an AC half-cycle, not from an individual switching cycle. The average value of the inductor currents during $T_{OFF1}$ does equal $I_{OUT}$ when averaged over an AC half-cycle, but this is generally not true for an individual switching cycle.

As can be seen from Equation 26, the magnitude and polarity of $I_{DC}$ is dependent on the ratio of $L2$ to $L1$ and the product of $V_{OUT}$ and $V_{IN}$ to $V_{IN}$. Equation 26 becomes invalid when $V_{IN}$ falls below the voltage where maximum duty cycle would occur.

As long as Equation 24 is satisfied, the inductors will operate in discontinuous mode. Within this limitation, the determination of inductance values for $L1$ and $L2$ is somewhat arbitrary. However, there is an advantage in keeping $I_{DC}$ positive over a complete AC half-cycle. Otherwise, if $I_{DC}$ is negative, current will flow into the input capacitor ($C_{IN}$, Figures 5, 7 and 8). Since $C_{IN}$ is deliberately a low value to accurately track the rectified AC line voltage, its voltage can change significantly due to $I_{DC}$. This behavior can impair power factor performance.

Setting Equation 26 equal to zero and solving for the ratio of $L2$ to $L1$, and substituting the result into Equation 24 yields upper limit values for $L1$ and $L2$. Examining Equation 26 further, it is apparent that if $L1 >> L2$, $I_{DC}$ will be positive for most practical operating conditions.

As previously determined, the average value of current in $L2$ is the output current, $I_{OUT}$. The average current through $L1$ is shown in Equation 27:

$$\bar{I}_{L1} = \frac{V_{OUT}}{V_{IN}} I_{OUT}$$  
(EQ. 27)

where $V_{IN}$ is the average minimum input voltage during an AC half-cycle. The change in inductor currents is shown in Equations 27 and 28:

$$\Delta I_{L1} = \frac{V_{IN}}{L1} T_{ON} = \frac{V_{OUT}}{L1} T_{OFF1}$$  
(EQ. 28)

$$\Delta I_{L2} = \frac{V_{IN}}{L2} T_{ON} = \frac{V_{OUT}}{L2} T_{OFF1}$$  
(EQ. 29)

The peak value of inductor current is the change in inductor current, $\Delta I_{LX}$ plus the offset DC current, $I_{DC}$.

$$I_{PK(L1)} = \frac{V_{IN}}{L1} T_{ON} + I_{DC} = \frac{V_{OUT}}{L1} T_{OFF1} + I_{DC}$$  
(EQ. 30)

$$I_{PK(L2)} = \frac{V_{IN}}{L2} T_{ON} - I_{DC} = \frac{V_{OUT}}{L2} T_{OFF1} - I_{DC}$$  
(EQ. 31)

where $V_{IN}$ is the maximum instantaneous input voltage, $V_{OUT}$ is the minimum output voltage, and $I_{DC}$ is determined from
Equation 26. The RMS currents for each inductor are shown in Equations 32 and 33:

\[
I_{\text{RMS}(L1)} = \sqrt{\frac{I_{\text{ON}} + I_{\text{OFF1}}}{T_S} \left( \frac{\Delta I_{L1}^2}{3} + I_{DC} \Delta I_{L1} + I_{DC}^2 \right) + I_{DC}^2}
\]

(EQ. 32)

\[
I_{\text{RMS}(L2)} = \sqrt{\frac{I_{\text{ON}} + I_{\text{OFF1}}}{T_S} \left( \frac{\Delta I_{L2}^2}{3} - I_{DC} \Delta I_{L2} + I_{DC}^2 \right) + I_{DC}^2}
\]

(EQ. 33)

The ripple current through the series capacitor, \(C1\), may be calculated from the RMS currents during each of the portion of the switching cycle, \(T_{\text{ON}}\), \(T_{\text{OFF1}}\), and \(T_{\text{OFF2}}\).

\[
I_{\text{RMS}(C1)} = \frac{2}{\pi} \left[ I_{C1(\text{RMS})T_{\text{ON}}} + I_{C1(\text{RMS})T_{\text{OFF1}}} + I_{C1(\text{RMS})T_{\text{OFF2}}} \right]
\]

(EQ. 34)

where:

\[
I_{C1(\text{RMS})T_{\text{ON}}} = \sqrt{\frac{I_{\text{ON}}}{T_S} \left( \frac{\Delta I_{L2}^2}{3} - I_{DC} \Delta I_{L2} + I_{DC}^2 \right)}
\]

\[
I_{C1(\text{RMS})T_{\text{OFF1}}} = \sqrt{\frac{I_{\text{OFF1}}}{T_S} \left( \frac{\Delta I_{L1}^2}{3} + I_{DC} \Delta I_{L1} + I_{DC}^2 \right)}
\]

\[
I_{C1(\text{RMS})T_{\text{OFF2}}} = \sqrt{\frac{I_{\text{OFF2}}}{T_S} I_{DC}^2}
\]

The individual RMS values must be evaluated using the maximum instantaneous input voltage, which occurs at the peak of the rectified input AC voltage. The factor of \(2/\pi\) averages the RMS value over a complete AC half-cycle.

The RMS current through switch, \(Q1\), is shown in Equation 35:

\[
I_{\text{RMS}(Q1)} = \frac{2}{\pi} \left( \Delta I_{L1} + \Delta I_{L2} \right) \sqrt{\frac{T_{\text{ON}}}{3T_S}}
\]

(EQ. 35)

where \(\Delta I_{L1}\) and \(\Delta I_{L2}\) are evaluated at the maximum instantaneous input voltage. Ignoring voltage transients, the voltage stress on \(Q1\) is equal to \(V_{\text{IN}}\) plus \(V_{\text{OUT}}\) plus \(V_{D1}\).

The ripple current rating for \(C_{\text{OUT}}\) is an involved calculation. There is a high frequency component at the switching frequency, a low frequency component at the rectified AC frequency, and a DC load current component. An estimate of the RMS ripple current rating for \(C_{\text{OUT}}\) can be approximated from Equation 36.

\[
I_{\text{RMS}(C_{\text{OUT}})} \approx \sqrt{\frac{T_{\text{OFF1}}}{T_S} \left( \frac{\left(\Delta I_{L1} + \Delta I_{L2}\right)^2}{3} - \left(\Delta I_{L1} + \Delta I_{L2}\right)I_{\text{OUT}} \right) + I_{\text{OUT}}^2}
\]

(EQ. 36)

The Flyback Converter

If the difference between the average input voltage and the output voltage is large, the SEPIC topology discussed earlier may not be appropriate due to the extremely low duty cycle required for steady state operation. A transformer coupled topology may be required to step the voltage down to a more manageable level. Transformer coupled topologies can also provide isolation between the input and output as may be required in some applications.

The simplest transformer coupled topology is the Flyback converter. Depending on the application requirements, the converter can be isolated or not. Figure 9 shows a non-isolated configuration where the primary and secondary grounds are common, and the control loop has no isolation component.

The Flyback converter operates in a similar fashion as the Boost and SEPIC converters discussed earlier. Like those
topologies, the main considerations are to operate at a nearly constant duty cycle and in Discontinuous Conduction Mode (DCM).

DCM operation must be confirmed for peak minimum input voltage \((V_{\text{RMS(min)}} \times \sqrt{2})\), maximum output current, and minimum output voltage. Given a constant load and output voltage, the average input voltage will determine the duty cycle. The maximum duty cycle occurs at the minimum average input voltage. Since power transfer from the primary to the secondary tracks the magnitude of the instantaneous AC voltage, the power transferred to the secondary is less than required when the instantaneous voltage is less than the average value for an AC cycle, and more than is required when the instantaneous voltage is greater than the average voltage. The highest currents occur when the instantaneous voltage reaches its maximum \((V_{\text{RMS(min)}} \times \sqrt{2})\). It is at this operating condition that DCM operation must be maintained in order to achieve acceptable power factor. Even though the duty cycle is determined by the average input voltage, the designer must establish DCM operation at the instantaneous peak input voltage.

The transformer design is the critical component in achieving the desired performance. The primary inductance, the secondary inductance, and the energy storage capability of the core structure must all be considered in the design. These are the same considerations present in any DCM flyback design, except it is complicated by the time-varying nature of the rectified AC input voltage.

The following discussion assumes that the output power, \(P_O\), the maximum desired operating flux density, \(B_{\text{max}}\), the maximum duty cycle, \(D_{\text{MAX}}\), and the switching frequency, \(f\), are pre-established quantities. The first step is to determine the energy storage requirement of the transformer core.

\[
\Delta W = \frac{P_o}{\eta \cdot f} \quad \text{(EQ. 37)}
\]

where \(\Delta W\) is the energy stored in the core structure in joules, \(P_o\) is the output power, \(\eta\) is the expected conversion efficiency, and \(f\) is the switching frequency of the converter. The output current, \(I_O\), can be expressed using Equation 38:

\[
I_O = \frac{P_o}{\eta \cdot V_o} \quad \text{(EQ. 38)}
\]

where \(V_o\) is the output voltage. The efficiency, \(\eta\), is included in Equation 38 to approximate the equivalent output current the converter must process. \(I_O\) is the (equivalent) average output current that must be delivered to the load under the worst case operating conditions while operating in DCM. It is also the average current flowing in the secondary of the transformer. The desired operating behavior is to have the switching cycle terminate just as the current in the secondary winding becomes discontinuous. Furthermore, this condition must occur when operating at maximum duty cycle (minimum \(V_{\text{RMS}}\)) while the input AC voltage is at the peak of its sinusoidal waveform. Equation 39 defines the change in secondary current, \(\Delta I_S(\text{min})\), that must occur to maintain DCM operation.

\[
\Delta I_S(\text{min}) = \frac{\pi \cdot I_O}{1 - D_{\text{MAX}}} \quad \text{(EQ. 39)}
\]

where \(D_{\text{MAX}}\) is the duty cycle that occurs at the minimum input RMS input voltage, and \(I_O\) is the average output current. \(\Delta I_S(\text{min})\) is scaled by \(\pi/2\) because the duty cycle is determined by the average input voltage, not the peak.

The maximum secondary inductance, \(L_S\), that allows the current to completely decay during the off time for DCM operation is shown in Equation 40:

\[
L_S = \frac{V_o (1 - D_{\text{MAX}})}{f \cdot \Delta I_S(\text{min})} = \frac{V_o (1 - D_{\text{MAX}})^2}{f \cdot \pi \cdot I_O} \quad \text{(EQ. 40)}
\]

The transformer turns ratio, \(N_s/N_p = N_{\text{sp}}\), may be calculated as follows.

\[
N_{\text{sp}} = \frac{V_o}{V_{\text{IN(min, pk)}}} \cdot \frac{(1 - D_{\text{MAX}})}{D_{\text{MAX}}} \quad \text{(EQ. 41)}
\]

where \(V_{\text{IN(min, pk)}}\) is the peak value of the minimum AC voltage input.

The primary inductance, \(L_p\), is easily calculated from the turns ratio and secondary inductance value.

\[
L_p = \frac{L_S}{N_{\text{sp}}^2} \quad \text{(EQ. 42)}
\]

The peak secondary current during a switching cycle is:

\[
I_{s, \text{peak}} = \frac{V_{\text{IN(min, pk)}} \cdot D_{\text{MAX}}}{f \cdot L_p \cdot N_{\text{sp}}} = \frac{V_o (1 - D_{\text{MAX}})}{f \cdot L_S} \quad \text{(EQ. 43)}
\]

Up to this point, the design procedure has been independent of the core geometry and material characteristics. To proceed, these parameters must be considered. For this discussion, a E-E core with an effective cross-sectional area \(A_e\) and having discrete air gap \(I_g\) will be considered. Furthermore, the core has a residual flux density of \(B_r\) and a recommended maximum flux density of \(B_{\text{MAX}}\). The number of secondary turns, \(N_s\), is expressed in Equation 44:

\[
N_s = \frac{I_{s, \text{peak}} \cdot L_s}{A_e \cdot (B_{\text{MAX}} - B_r)} \quad \text{(EQ. 44)}
\]

The required air gap in the core, \(I_g\), can be found using Equation 45:

\[
I_g = \frac{\mu_0 \cdot A_e \cdot N_{s}^2}{L_S} \quad \text{(EQ. 45)}
\]
where \( \mu_0 \) is the permeability of free space (4\( \pi \) \( \times \) 10\(^{-7} \)) and the result is in meters (mks units). The number of primary turns can be found using Equation 46.

\[
N_p = \frac{N_S}{N_{s/p}} \quad \text{(EQ. 46)}
\]

The capacity of the core to store sufficient energy needs to be verified. Since all of the stored energy occurs in the air gap, the volume of the air gap determines the energy storage capacity.

\[
\frac{A_e \cdot l_g}{\mu_0} \geq \frac{2 \cdot \Delta W}{(B_{\text{max}} - B_r)^2} \quad \text{(EQ. 47)}
\]

where \( \Delta W \) is defined in Equation 37. If the inequality of Equation 47 is not satisfied, the air gap must be increased, or the maximum flux density, \( B_{\text{max}} \), must be increased.

The worst case RMS winding currents are expressed in Equations 48 and 49:

\[
I_{P,\text{rms}} = \frac{2}{\pi} \frac{V_{\text{IN(min, pk)}}}{f \cdot L_P} \left( \frac{V_O}{3} \left( \frac{1}{N_{s/p} \cdot V_{\text{IN(min, pk)}} + V_O} \right) \right)^{\frac{1}{2}} \quad \text{(EQ. 48)}
\]

\[
I_{S,\text{rms}} = \frac{2}{\pi} \frac{V_{\text{IN(min, pk)}}}{f \cdot L_P \cdot N_{s/p}} \left( \frac{V_O}{3} \left( \frac{1}{N_{s/p} \cdot V_{\text{IN(min, pk)}} + V_O} \right) \right) \quad \text{(EQ. 49)}
\]

The output current, \( I_{\text{OUT}} \), is equal to the average current in the secondary winding of the transformer. Since current only flows in the secondary winding during \( T_{\text{OFF1}} \), the output current can be expressed as:

\[
I_{\text{OUT}} = \frac{V_O \cdot T_{\text{OFF1}}}{2T_s \cdot L_S} \quad \text{(EQ. 50)}
\]

Solving for \( T_{\text{OFF1}} \) yields:

\[
T_{\text{OFF1}} = \frac{\sqrt{2I_O \cdot T_s \cdot L_s}}{V_O} \quad \text{(EQ. 51)}
\]

The change in current, \( \Delta I \), during \( T_{\text{ON}} \) and \( T_{\text{OFF1}} \) scaled by the turns ratio must be equal. Equating the change in amp turns (\( \Delta I^*N_p = \Delta I^*N_S \)) during \( T_{\text{ON}} \) and \( T_{\text{OFF1}} \), respectively, and solving for \( T_{\text{ON}} \) yields:

\[
T_{\text{ON}} = \frac{V_O \cdot N_p}{V_{\text{IN}}} \cdot T_{\text{OFF1}} \quad \text{(EQ. 52)}
\]

where \( V_{\text{IN}} \) is the average input voltage. Equations 51 and 52 represent the average values of \( T_{\text{OFF1}} \) and \( T_{\text{ON}} \), respectively. While \( T_{\text{ON}} \) is essentially constant during an AC half-cycle, the instantaneous value of \( T_{\text{OFF1}} \) will vary considerably over the same time period. The instantaneous value of \( T_{\text{OFF1}}, T_{\text{OFF1}}' \), may be calculated from Equation 53.

\[
T_{\text{OFF1}} = \frac{N_S}{N_p} \cdot V_{\text{IN}} \cdot T_{\text{ON}} \quad \text{(EQ. 53)}
\]

where \( V_{\text{IN}} \) is the instantaneous value of the input voltage.

**The Output Capacitor**

Each of these converters operates from the AC mains with high power factor. Power delivery from the AC mains is sinusoidal and at a low frequency, so either the power to the load must be delivered as received from the source or there must be a provision to store the energy in the converter. The output capacitor performs this function. It not only filters the converter switching currents, but must also provide sufficient energy storage to maintain the output during the AC nodes with an acceptable level of ripple voltage. The allowed ripple voltage is determined by how much ripple current is acceptable in the LED load. Due to the non-linear behavior of the LED diode junction, the ripple current will be higher than might be expected from a given ripple voltage. Although higher ripple currents, even as much as 50-70%, do not produce observable flicker, some LED manufacturers suggest limiting the amount of ripple current to keep peak currents within ratings. Ultimately, the designer must evaluate the trade-offs between capacitance value and ripple current.

**The Control Loop**

Figures 12, 13, and 14 show detailed schematics for boost, SEPIC, and flyback converters, respectively. These converters are based on the Intersil ISL6745 double-ended PWM controller. The control loop is not topology dependent. The same loop configuration can be used in virtually all off-line AC LED applications. It consists of an operational amplifier in a low bandwidth integrator configuration. Referring to Figure 10, resistor \( R_S \) converts the LED current into a voltage that is compared to \( V_{\text{REF}} \). The operational amplifier integrates the difference and creates an error voltage output used to control the PWM.

The critical requirement for the control loop is that its bandwidth be limited to about 30Hz. The crossover frequency, \( f_C \) of the control loop is shown in Equation 54:

\[
f_C = \frac{1}{2\pi R C_{FB}} \quad \text{(EQ. 54)}
\]

Setting \( f_C \) equal to 30Hz and solving for the RC time constant \( \tau \) yields Equation 55:

\[
\tau = R C_{FB} = \frac{1}{60\pi} \quad \text{(EQ. 55)}
\]

For example, selecting \( C_{FB} = 0.1 \mu F \), yields a value of 53k\( \Omega \) for \( R \).

The LED current is set by \( V_{\text{REF}} \) and \( R_S \), but the current may also be dynamically modulated using the \( I_{\text{ADJ}} \) input to vary the...
Using Multiple Parallel LED Strings

The previous discussion centered on a single string of LEDs in series for the sake of clarity. For many applications, a single string may be acceptable, but other applications may require more light intensity than can be practically delivered by a single string of LEDs. In these applications, additional LEDs strings may be added in parallel.

Since the LED driver provides a single output, it cannot control the current through each LED string. Unless there is a mechanism to force equal currents through each LED string, the currents will not be balanced. The magnitude of the imbalance depends on the cumulative variation of forward voltage drop across each LED in the string. If the forward voltage distribution for each LED is random, then the differences in the cumulative variation among the LED strings tends to zero out as the number of LEDs in each string increases.

The forward voltage drop across each LED may be represented as a temperature dependent voltage in series with a resistor. Fortunately, the resistance is rather large for the LEDs under consideration. CREE XLamp 7090 LEDs, for example, has an equivalent series resistance of approximately 1.9Ω. The resistance tends to linearize the V-I relationship of the LED so that variations in the voltage drop due to temperature and process variation have a reduced impact. Adding a discrete series resistor in each LED string will further enhance current balance, but at the expense of increased power dissipation.

However, depending on the application, just paralleling LED strings may cause unacceptable color temperature and/or intensity variation among the LED strings. Additional circuitry to force current balancing may be required.

Figure 11 shows a technique of paralleling LED strings with current balancing. The method consists of a master LED string and multiple slave strings in parallel. The LED driver control loop regulates the current in the master LED string, and the slave LED strings are individually regulated to match the current through the master LED string. Diode D is present only in the master LED string so that the linear pass elements, Q, in the slave LED strings have sufficient voltage across them to allow regulation. Alternatively, an extra LED in the master string accomplishes the same result.

References

Application Circuits (Continued)

FIGURE 13. DETAILED SEPIC CONVERTER SCHEMATIC

NOTES: Unless otherwise specified
1) All components are 0805
2) All capacitors are ceramic 10%, 50V
3) All resistors are 1%
4) DNP = May not be required, depending on power level and layout
5) TBD component values depend on quantity and type of LEDs used.

FIGURE 13. DETAILED SEPIC CONVERTER SCHEMATIC
Application Circuits (Continued)

1) All Resistors are 1% 0805 unless otherwise specified.
2) All capacitors are 10% 50V 0805 X7R ceramic unless otherwise specified.
3) TBD values are dependent on the type and quantity of LEDs used.

FIGURE 14. DETAILED FLYBACK CONVERTER SCHEMATIC
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement of any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersize repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failures or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high quality product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations and that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

http://www.renesas.com

© 2018 Renesas Electronics Corporation. All rights reserved.

Colophon 7.0