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Introduction

LDMOS transistors are used for RF Power Amplification in numerous applications from point-to-multipoint communications to Radar. The most pervasive application is in cell phone basestations. These RF Power Amplifiers (RFPA) provide from 5W to over 200W of output power per channel, and require very good linearity to maximize the data throughput in a given channel. The main point to consider is that linearity is the DC biasing of the LDMOS transistor for optimal drain current for a given power output. This bias needs to be held constant over temperature and time. Typically the target accuracy for bias current over temperature is ±5% but ±3% is much more desirable for a high performance design.

A simplified circuit of an LDMOS amplifier bias circuit is shown in Figure 1. The DC Bias on these amplifiers is set by applying a DC voltage to the gate (V_{GS}) and monitoring the Drain current (I_{DD}). Ideally, this I_{DD} will be constant over temperature, but since the V_{GS} of LDMOS amplifier devices varies with temperature, some type of temperature compensation is required. One method of setting this DC bias involves using an adjustable reference, DAC, or Digital potentiometer combined with a temperature compensation source, such as a transistor V_{BE} multiplier. This solution can work well, but getting tight temperature compensation can be problematic since the V_{BE} junction temperature characteristic for production transistors will vary. Also, the V_{GS} tempco for LDMOS amplifiers will vary with I_{DD}. The result is that there are variations in V_{BE} junction characteristics as well as the LDMOS characteristics. For optimal temperature compensation, in-circuit adjustments need to be made for both the temperature compensation as well as the V_{GS} bias itself.

A new way to bias an LDMOS amplifier is presented in the following, which involves digitally converting temperature information.

The ISL21400 Programmable Output Temperature Sensor IC

The ISL21400 is an analog output temperature sensor, which is programmable for both DC output voltage and temperature slope (see Figure 2). Two voltage reference blocks produce both temperature compensated and proportional to temperature outputs. There are two DACs inside the device which are programmed via the I²C bus interface. One DAC is for the voltage reference, the other is for the temperature sensor, and they provide 8-bit control to scale either output. The resulting output is summed and then a variable gain stage provides for a gain of 1, 2 or 4.

The DC voltage reference output is 1.20V nominal, and considering the DAC scaling and the gain available, this gives a DC output range of 0V to 4.8V (with a 5.0V supply). The nominal temperature slope is -2.1mV/°C, and this is scaled for both positive and negative slopes by the DAC. Including the gain stage, this provides for up to ±8.4mV/°C temperature slope.
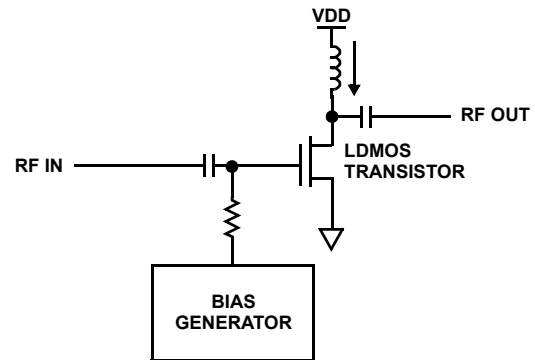

FIGURE 1. RFPA SIMPLIFIED SCHEMATIC

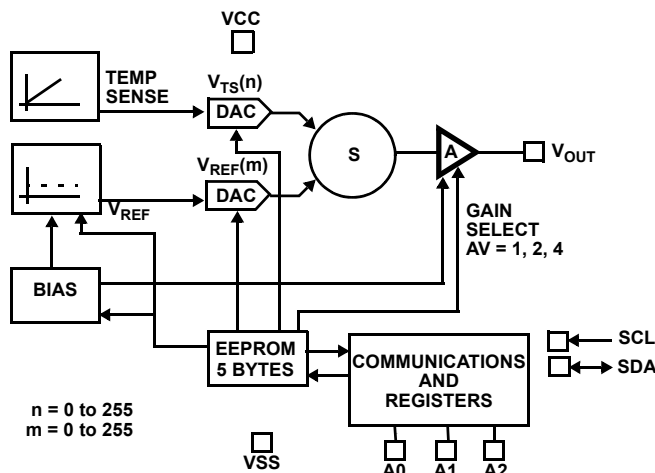**FIGURE 2. ISL21400 BLOCK DIAGRAM**

The ISL21400 is especially suited to temperature compensation functions due to the slope programmability and 2% accuracy of the temperature sensing function. The bias voltage produced by the device has both a programmable DC component and a temperature slope component. The voltage output is capable of driving nominal resistive loads with up to 0.5mA of DC output current, and can handle up to 500pF of capacitive loads. These characteristics are well suited to LDMOS applications where the output voltage is isolated from any capacitive load with a small resistor, and the bias current required is negligible.

Hardware Design using the ISL21400

RFPA bias control using the ISL21400 is very straightforward. The dashed rectangle highlights the RFPA circuit using an MRF9080 from NXP (formerly Freescale)[1].The basic schematic is shown in Figure 3. The maximum supply voltage for the ISL21400 (U2) is 5.5V and U1 drops the LDMOS V_{DD} supply from +26V to +5.0V for the U2 V_{CC} supply. An LC filter is added to the U2 V_{CC} supply to insure no RF energy is present on that supply line.

The ISL21400 output is connected to the LDMOS gate (V_{GG}) through a lowpass filter, which blocks any RF energy from reaching the ISL21400. A series 100Ω output resistor (R_2) isolates the filter capacitor from the VOUT pin to insure stability. Also, R_2 allows a simple shutdown circuit to be added with Q_2 and R_3, which will provide a soft V_{GG} clamp when the gate of Q_2 is brought high (>2V). An open drain gate can be used as well as long as the leakage current at high temperatures is not excessive.

The ISL21400 SCL and SDA lines can be tied to a local microcontroller or to an I/O connector for external PC control and programming. The A0, A1, A2 pins are all tied to ground giving an I2C slave address of 0101000x, where x is the read/write bit.
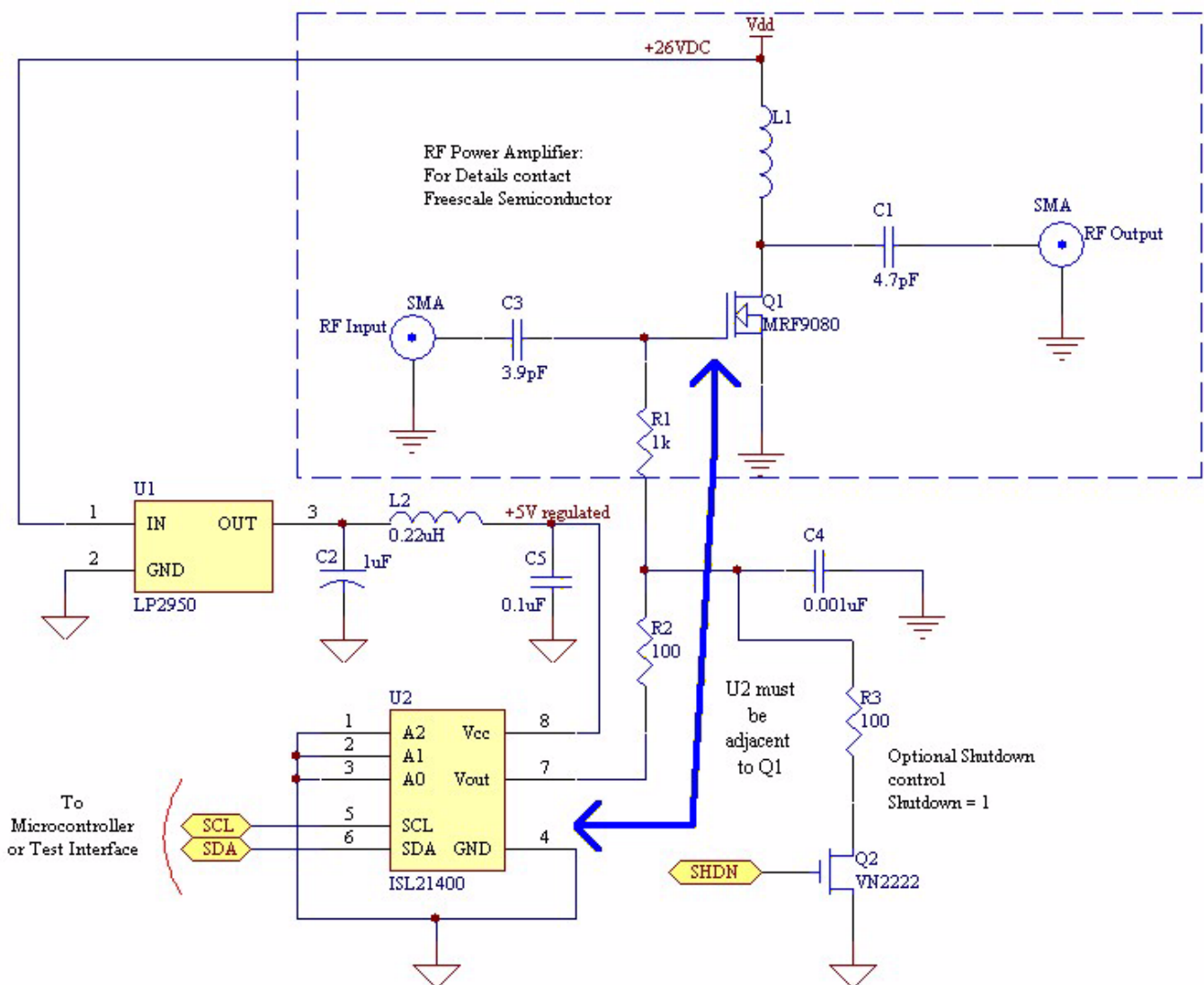

FIGURE 3. RFPA BIAS CONTROL WITH THE ISL21400

This entire circuit was implemented on the RFPA evaluation board with the MRF9080. The ISL21400 is placed adjacent to the LDMOS device to get best temperature tracking. The register programming is done using a LabVIEW PC tool for software control and parallel port interface board, which has lines for SCL/SDA. The board is disconnected for testing in a temperature chamber.

Calculating the ISL21400 Register Values

The ISL21400 data sheet[2] contains guidelines for calculating temperature slope using the three control registers: Offset, Slope and Gain control. We will use the equations given in the following sections to calculate the register values for this design.

In this circuit, the N-channel LDMOS transistor gate has approximately a -2.8mV/°C temperature coefficient from -10°C to +85°C. A constant bias drain current is desired, with a target V_{GS} range derived from the data sheet of 2.5V to 3.5V at +25°C.

OFFSET SETTING

Using Equation 1 for setting V_{OUT} offset and targeting V_{OUT} = 3.0VDC:

$$V_{OUT(DC)} = A_V \bullet V_{REF} \bullet A_{REF} = 3.00V \qquad \text{(EQ. 1)}$$
$$V_{REF} = 1.20V$$
$$A_V \bullet A_{OS} = 2.50$$

Note that A_{REF} varies from 0 to 1, so to get 2.40, $A_V = 4$, use Equation 2.

$$A(REF) = \frac{2.50}{4} = 0.625 = \frac{n}{255} \qquad \text{(EQ. 2)}$$
$$n = 159 \text{ decimal}$$
$$= 9F \text{ hex}$$

The variable n corresponds to register address 0h, and the variable A_V is the gain register, which is address 02h.

TEMPERATURE SLOPE SETTING

Using Equation 3 for temperature slope, we can solve for Slope directly:

$$V_{OUT}(TS) = A_V \bullet K \bullet A_{PTAT} = -2.8mV/°C$$

$$A_{PTAT} = \frac{-2.8}{4 \bullet -2.1}$$

$$A_{PTAT} = 0.333 = \frac{(2 \bullet m) - 255}{255} \qquad \text{(EQ. 3)}$$
$$m = 170 \text{ decimal}$$
$$= A9 \text{ hex}$$

The variable m corresponds to address 01h.

The ISL21400 device is then programmed with these parameters for initial testing. Temperature chamber testing is then performed to verify performance, and if needed, adjustments to the register settings are implemented to optimize performance.

Note that since V_{GS} drift is not perfectly linear with temperature, that the I_{DS} bias error will increase at the temperature extremes due to this nonlinearity.

Results

The amplifier platform was powered up with the V_{GG} voltage clamped in shutdown mode until the ISL21400 was powered up and programmed. The initial setting for V_{GS} = 3.0V was too low for the target value of I_{DD} = 600mA so the value for n was increased until a suitable I_{DD} close to the target was reached. The final register setting was n = B0h.

The amplifier platform including the ISL21400 bias control circuit was placed in a temperature chamber and tested from -10°C ambient to +65°C. This resulted in board temperatures from -10°C to +90°C. The bias current was monitored (RF power OFF and input/output terminated in 50Ω) and results are shown in Figure 4. V_{GG} bias voltage was monitored with a voltmeter tied to the drain of Q_2 to limit parasitic effects on the LDMOS gate. The result is plotted in Figure 4 as well. Error from Ideal is shown in Figure 5.

Figure 5 includes ±5% range, and the amplifier stays within these limits fairly consistently, meeting the design goals. The initial setting for bias appears somewhat high at 620mA (compared to target of 600mA) but this is limited by the resolution of the ISL21400 at the gain = 4 setting. The next lowest offset level results in a bias of 568mA, which is too low.
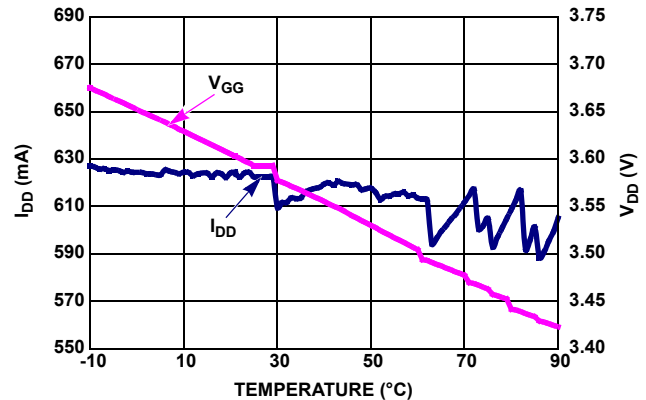

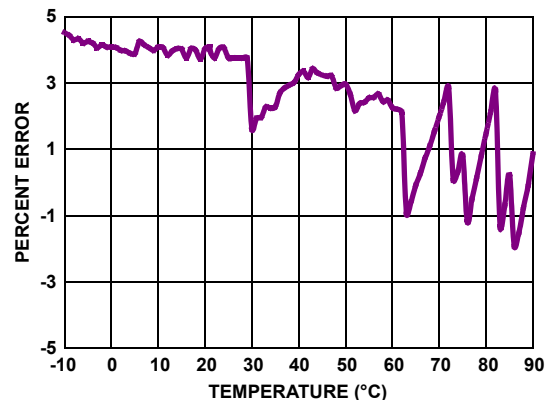**FIGURE 4. MEASURED DRAIN CURRENT vs TEMPERATURE**

FIGURE 5. I_{DD} BIAS ERROR VS TEMPERATURE

One thing to note in this design or any that requires temperature compensation is the mechanical properties of the board mounting and the cooling system. In this example, airflow over the LDMOS device and the temperature sensor was limited, which enhanced the resulting compensation. Also, the sensor was surface mounted with conductive grease next to the LDMOS device. In many designs, precise control over placement and airflow is not possible, but since calibration takes place *after* the assembly of the unit, these effects can be minimized as long as the final installation is similar to the calibration conditions.

LDMOS amplifiers also have a characteristic I_{DD} drift over time (drain current reduces for a given V_{GS}), as well as temperature. This can be addressed with either recalibration or purposely setting the I_{DD} bias high, knowing the drift will be in the negative direction.

References

1. NXP (formerly Freescale) Wireless Infrastructure Division
   2100 East Elliot Road
   Tempe, AZ 85284
   (800) 521-6274
   http://www.nxp.com/

2. Intersil Corporation
   1001 Murphy Ranch Road
   Milpitas, CA 95035
   http://www.intersil.com/

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