Putting Analog On The Bus

The objective of this application note is to (1) illustrate the idea of 'computerizing analog functions' and (2) provide the design engineer with reference designs for controlling the key parameters of analog circuits using digitally controlled potentiometers connected to a computer bus.

Basic Ideas

The computer has extended the capabilities of electronics products and systems by adding the power of high speed control, computation, and programmability at a very low cost. There are, however, applications where the compact, continuous signal analog circuits are still the preferred design approach. We can, however, have the best of both worlds if we combine the advantages of the computer with the advantages of the analog circuits. This can be done through *a Intersil digitally controlled potentiometer (XDCP); a system level control device performing a component level function.* Figure 1 is a caricature depicting the idea of 'putting analog on the bus'. Figure 2 illustrates the idea of computerizing an analog function in block diagram form. If parameters of an analog function are varied using a potentiometer and if the potentiometer is computer controlled, then the parameters of the analog function are controlled using the computer's bus. The idea of 'putting analog on the bus' refers to varying one or more of an analog circuit's parameters through the use of the digitally controlled potentiometer connected to the computer bus. Any analog circuit whose parameters depend on a resistance is a candidate for application of a digitally

controlled potentiometer. The potentiometer can be configured as a two-terminal variable resistance or a three-terminal voltage divider. The mixed signal *XDCP provides variability through its analog potentiometer and programmability through its computer interface and bus.*

The key analog functions are amplification, regulation, filtering, oscillation, and conversion and the circuits which implement these functions are amplifiers, regulators, filters, oscillators, and converters. Representative examples of each of these circuits will illustrate the computerization of the analog functions.

- **Amplifiers:** *Customized Potentiometers Advance Amplifier Design*
- **Regulators:** *Programmable System-Level Voltage Regulator*
- **Filters:** *Tunable Bandpass (IGMF) Filter*
- **Oscillators:** *Digitally Controlled Potentiometer Programs the 555,Phase Shift Sinusoidal Oscillator*
- **Convertors:** *I to V Convertor*

These basic analog circuits are used as universal building blocks in the design of analog systems and they also serve as models for more specialized analog functions. The following collection of *independent articles and circuits* are examples of 'putting analog on the bus'. All of them have been breadboarded and tested.
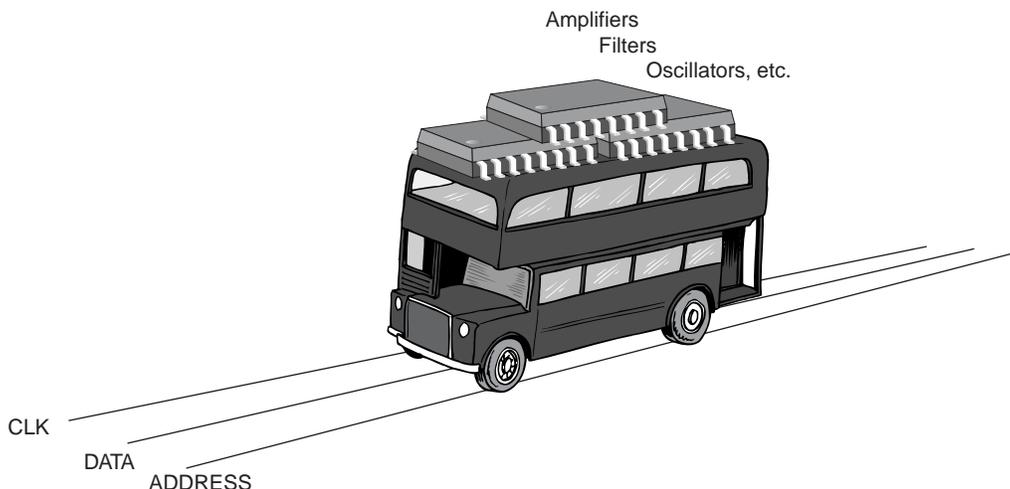

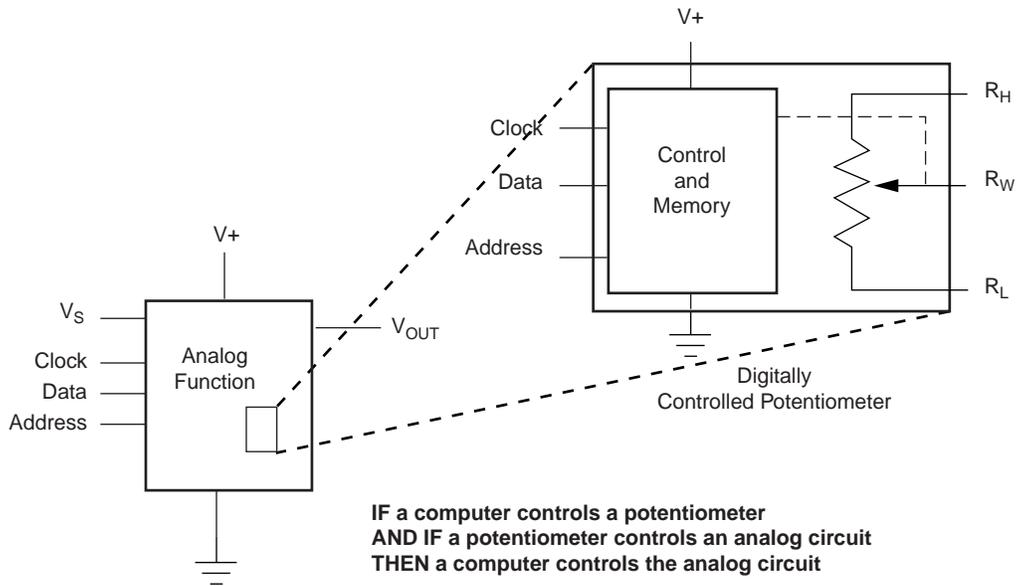**FIGURE 1. CARICATURE OF THE IDEA OF "PUTTING ANALOG ON THE BUS"**

FIGURE 2. BLOCK DIAGRAM OF "COMPUTERIZING AN ANALOG FUNCTION"

IF a computer controls a potentiometer
AND IF a potentiometer controls an analog circuit
THEN a computer controls the analog circuit

Customized Potentiometers Advance Amplifier Design

The circuit in Figure 3 is a model of an amplifier circuit whose cutoff frequency and gain are changed using variable resistors. The cutoff frequency is established by a first-order, RC low pass filter and the gain is established by a traditional noninverting operational amplifier circuit. Variability and programmability are added to the circuit if digitally controlled potentiometers (XDCPs) are used to implement the variable resistors. The circuit in Figure 4 shows the implementation of the frequency and gain controls. The potentiometer R is configured as a pseudo-tee network and along with capacitor C establishes the upper cutoff frequency f_C. Potentiometer R_2 is used as a three-terminal device and establishes the voltage gain G_0.

The voltage gain for the circuit has the form of

$$\frac{V_o}{V_s} = \frac{G_o \omega_c}{j\omega + \omega_c}$$

G_0 is the programmable closed-loop passband gain

$$G_0 = \frac{R_1 + R_2}{R_1 + k_2 R_2} \qquad 0 \le k_2 \le 1$$

where k_2 reflects the proportionate position of the wiper from one end of the pot (0) to the other end of the pot (1). The gain is programmable from 1 to $(R_1+R_2)/R_1$. The fixed resistor R_1 limits the circuit's maximum voltage gain, a condition usually necessary for accuracy and bandwidth purposes.

The upper cutoff frequency f_C is established by the input R-C network

$$f_c = \frac{\omega_c}{2\Pi} = \frac{1}{2\Pi(k_1 R)C} \qquad 0 \le k_1 \le 1$$

where k_1 (like k_2) reflects the proportionate position of the wiper from one end of the pot (0) to the other end of the pot (1). The dual versions of the XDCPs use the same serial bus with, of course, different addresses for the individual potentiometers.

For high frequency amplifiers, the high end-to-end resistance of 10kΩ (R_{TOTAL}) of the X9418 creates time constants limiting the bandwidth of the circuit. The effective end-to-end resistance of the potentiometers can be reduced using two techniques shown in the high frequency amplifier circuit of Figure 5. If the wiper of the potentiometer is connected to a high impedance, shunting R_{TOTAL} directly with an external resistor reduces the effective end-to-end resistance. Resistor R_3 changes the effective end-to-end resistance of potentiometer R_2 from 10kΩ to .909kΩ. If the wiper of the potentiometer is *not* connected to a high impedance, the effective end-to-end resistance can be reduced by adding external, equal valued resistors (R_4 and R_5) from the wiper to the high terminal and from the wiper to the low terminal. This technique, however, creates a potentiometer whose taper is pseudo-linear and whose end-to-end resistance varies with wiper position by about 20%. For most applications, these conditions are acceptable. The gain of the amplifier circuit in Figure 5 is programmable from 1 to 2 and the cutoff frequency is programmable from 130kHz to over 1MHz. The principle of computerizing an amplifier is shown in Figure 6 where the amplifier is a functional block and the gain and cutoff frequency are controlled through a serial bus connected to a digitally controlled potentiometer.

The design of high frequency circuits requires low value and sometimes odd value resistances. The two techniques shown in this circuit allow the designer to customize the values of a potentiometer's end-to-end resistance to fit the design requirements.
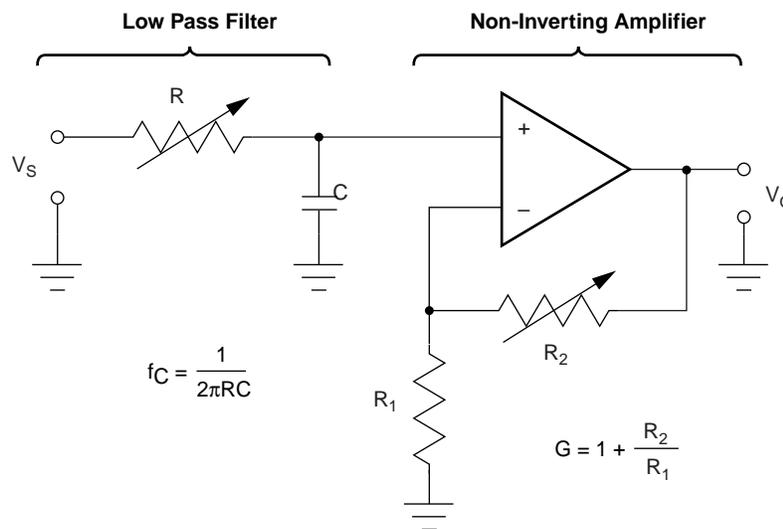

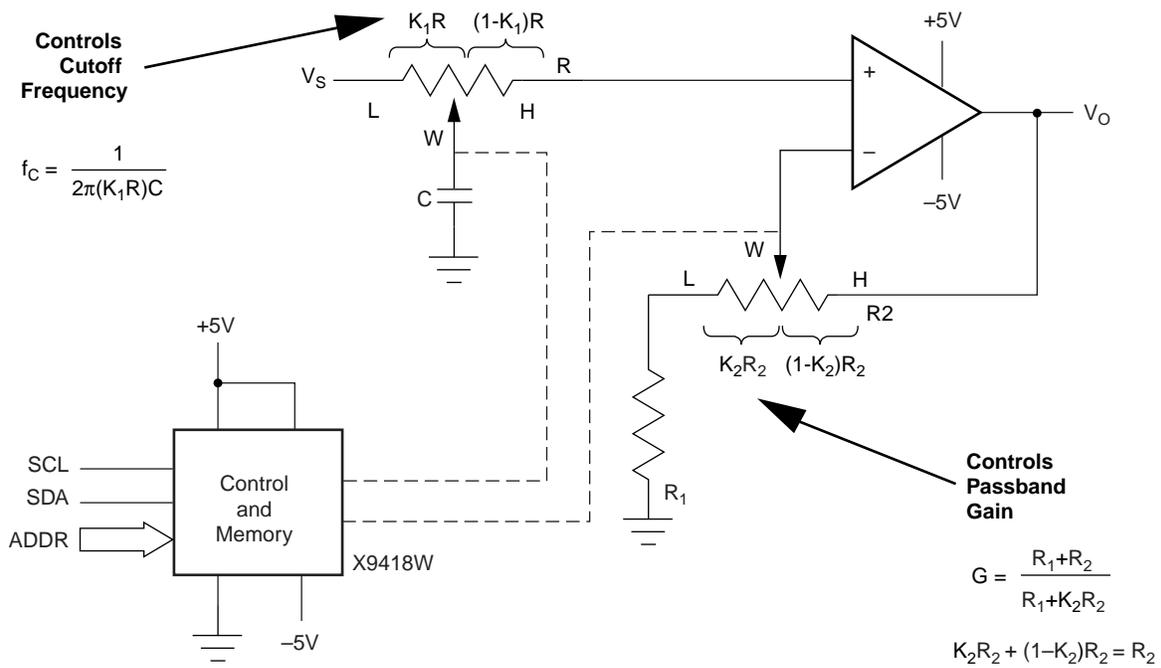**FIGURE 3. MODEL OF AMPLIFIER CIRCUIT**

Controls Cutoff Frequency

$$f_C = \frac{1}{2\pi(K_1R)C}$$

Controls Passband Gain

$$G = \frac{R_1+R_2}{R_1+K_2R_2}$$

$$K_2R_2 + (1-K_2)R_2 = R_2$$

FIGURE 4. GAIN AND FREQUENCY CONTROL

$$1 \le G_O \le 2$$

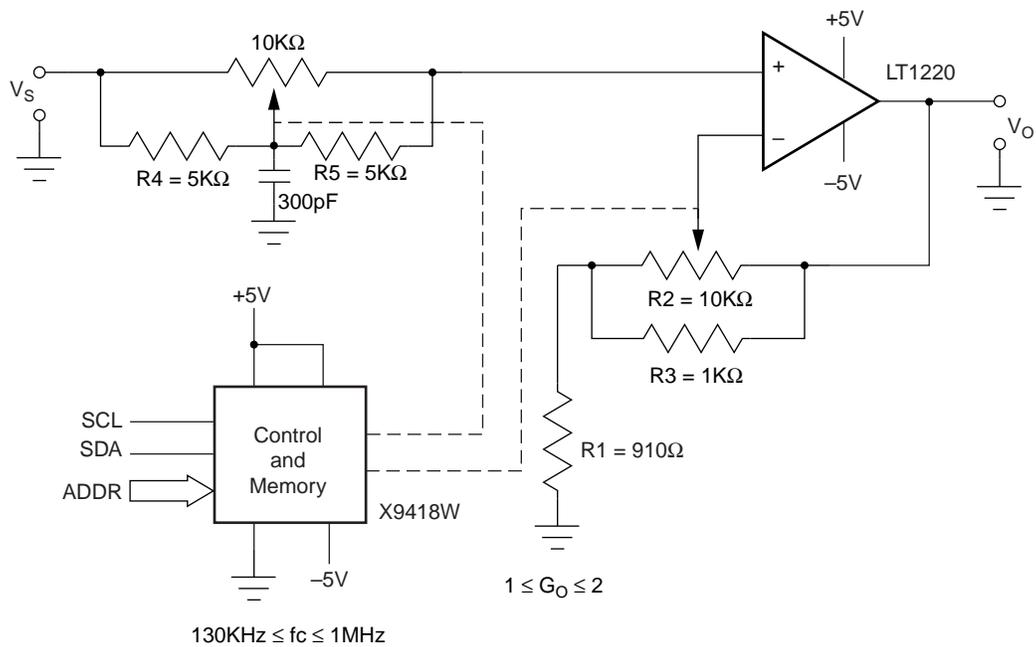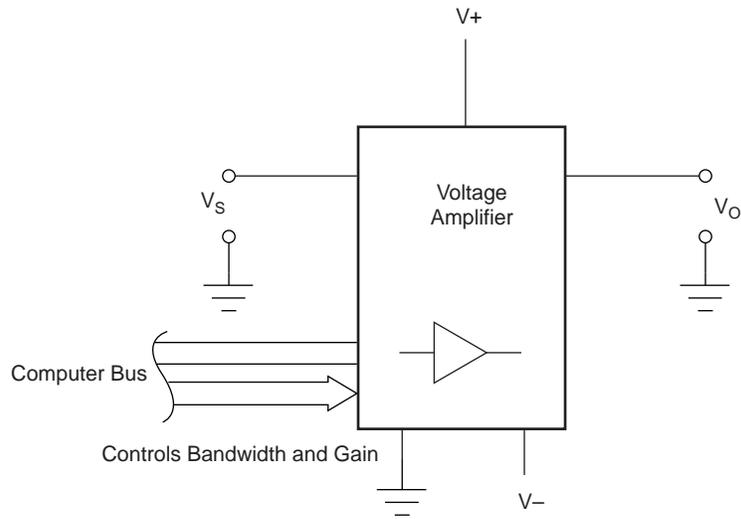$$130KHz \le fc \le 1MHz$$

FIGURE 5. HIGH FREQUENCY AMPLIFIER

FIGURE 6. PUTTING AN AMPLIFIER ON THE BUS

Programmable System-Level Voltage Regulator

Power consumption and failing batteries are key issues in battery operated applications. Features in the new generation of series voltage regulators address these concerns. For example, National Semiconductor's LP2951 is a micropower voltage regulator which provides a logic-level output signal detecting a low regulated output voltage and has a logic-level input to shutdown the regulator to conserve power. These signals are digital and hence compatible with processor based systems. With these type regulators, system designers can now use the basic device to provide voltage regulation and use the digital signals to address the power and low voltage concerns. But what about the programming or control of the regulator's output voltage? Surely a mechanical potentiometer or resistor selection is not the solution. We can complete the so-called computerization or digitizing of the voltage regulator by adding a digitally controlled potentiometer to program the regulator's output voltage.

The circuit in Figure 7 is wide-range, computer controlled voltage regulator whose nominal output voltage varies from 1.235V to 14.8V. The regulator is programmed using a Intersil digitally controlled potentiometer (XDCP) which, with its 100 taps or steps, can program the regulator output voltage with a resolution of .136V per step. The output voltage is given as

$$V_O = 1.235V\ (1 + kR/910\Omega)$$

where k is a number that varies from 0 to 1 and reflects the proportionate position of the wiper from one end of the pot (0) to the other end of the pot (1). R is the end to end resistance of the potentiometer and is also called R_{TOTAL}.

The XDCP is programmed using a 3-wire bus and the potentiometer is configured as a two-terminal variable resistor. The regulator output signal */ERROR* warns of a low output voltage and may be used as a power-on reset. The logic compatible *SHUTDOWN* input signal enables the regulator to be switched on and off to conserve power. These signals along with the ones required to program the XDCP are typically connected to the I/O port of the processor or controller.

The potentiometer adds variability to the regulator circuit and its digital controls attached to a computer controlled bus provides programmability. An automated closed-loop calibration procedure to program the regulator saves manufacturing test time and provides enhanced performance and security. The circuit can be used as a bias supply, voltage reference, or as a programmable, high output current, voltage source in test and measurement applications.

The stability of the regulator makes it a potential candidate for applications as a voltage reference. The low-power circuit in Figure 8 is a programmable voltage reference whose output voltage varies from 4.73V to 5.10V in 3.7mV steps. The output voltage is given as

$$V_O = 1.235V\ [1 + (kR + 100k\Omega)/\ 34k\Omega)]$$

The electronic potentiometer adds variability to the regulator circuit and its digital controls, through its computer controlled bus, provides programmability. An automated closed-loop calibration procedure to program the regulator saves test time and provides enhanced performance and security.
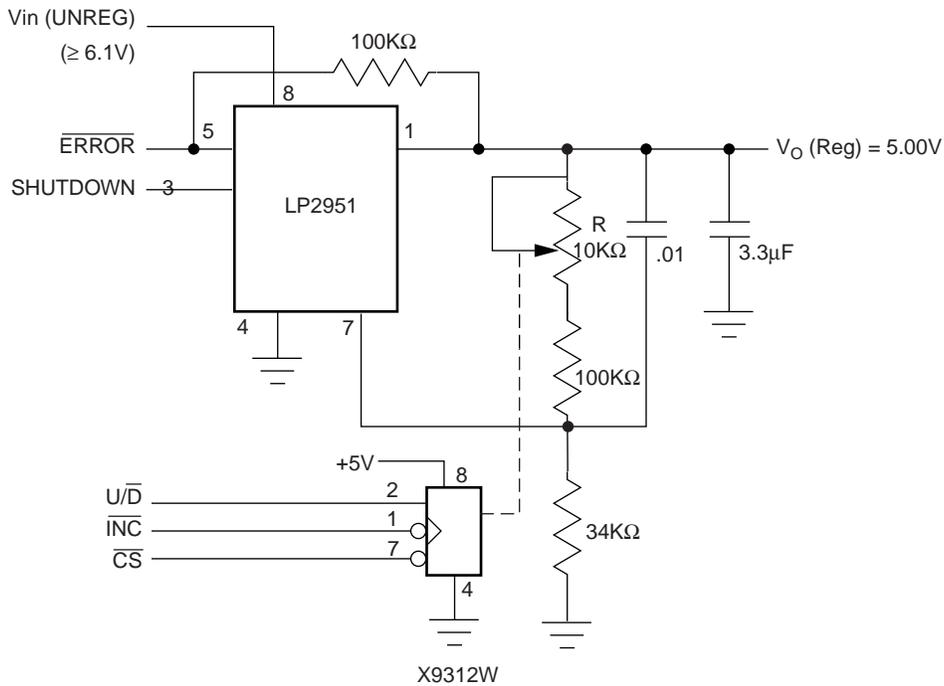
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$$V_O \text{ (Reg)} = 1.235V \ (1 + KR/910\Omega)$$
$$1.235V \leq V_O \text{ (Reg)} \leq 14.8V$$
$$\text{Resolution} = .136V/\text{Step}$$
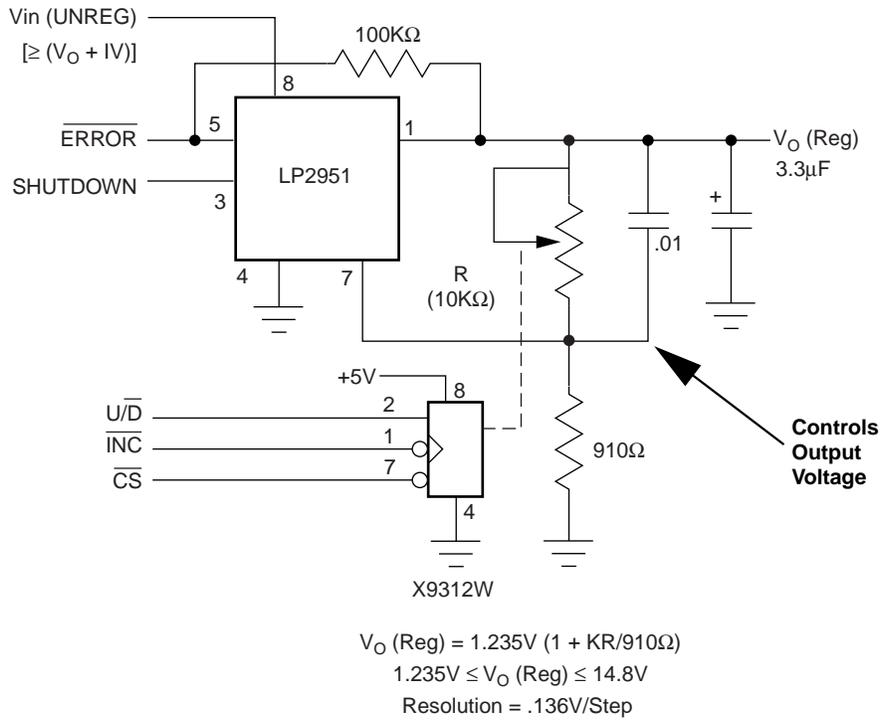
FIGURE 7. PROGRAMMABLE VOLTAGE REGULATOR

FIGURE 8. PROGRAMMABLE VOLTAGE REGULATOR

$$f_0 = \frac{1}{2C}\sqrt{\frac{(R_1+R_2)}{R_1+R_2R_3}} \ , \ 2.5\text{KHz} \le f_0 \le 12.5\text{KHz}$$

$$A_0 = -\frac{R_3}{2R_1} = -1$$

$$BW = \frac{1}{\pi R_3 C} = 796 \text{ Hz}$$
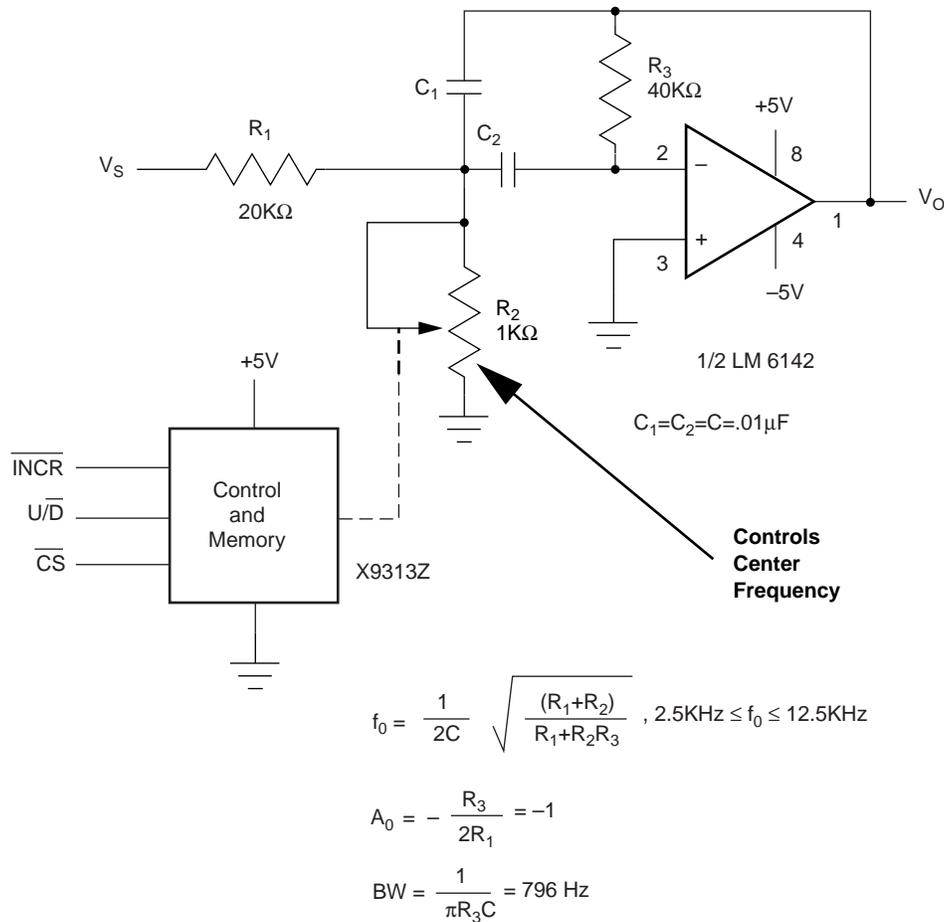
FIGURE 9. TUNABLE BAND PASS (IGMF) FILTER

Tunable Bandpass (IGMF) Filter

The circuit in Figure 9 is a tunable bandpass filter that falls in the Infinite Gain Multiple Feedback (IGMF) class. IGMF type filters are characterized by a fixed five-component configuration. For the circuit in Figure 9, the gain expression is

$$\frac{V_o}{V_s} = \frac{-s/R_1C}{s^2 + (2/R_3C)s + (R_1+R_2)/R_1R_2R_3C^2} = \frac{A_o s(\omega_o/Q)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

where A_O, ω_O, and Q represent the passband gain, characteristic frequency, and figure of merit respectively.

From the gain expression,

$$A_0 = -\frac{R_3}{2R_1},$$

$$f_0 = \frac{1}{2\Pi C}\sqrt{\frac{(R_1+R_2)}{R_1R_2R_3}},$$

and

$$Q = (1/2)\sqrt{\frac{(R_1+R_2)R_3}{R_1R_2}}$$

A problem common to most second order, active filters is the dependence of each of the filter's parameters on the values of all or most circuit components. Ideally, of course we would like to have one component control one parameter only. The equations above show that f_O can be varied by changing R_2 without changing the gain A_O.

The filter's bandwidth BW

$$BW = \frac{f_o}{Q} = \frac{1}{\Pi R_3 C}$$

is also independent of R_2. Hence varying R_2 will change the center frequency f_O but not the gain nor the bandwidth of the filter. If R_2 is a Intersil digitally controlled potentiometer (XDCP) connected as a variable resistor, the bandpass filter is digitally tunable and programmable.

For the circuit values shown, the passband gain is minus one, the bandwidth is 796Hz, and the center frequency can be varied from 2.5kHz to 12.5kHz. The circuit can be modified for self-tuning operation.

Digitally-Controlled Potentiometer Programs The 555

The use of the digitally-controlled potentiometer in the circuit of Figure 10 represents a new twist to controlling the heavily used 555 timer IC. The replacement of discrete resistors R_A and R_B in the traditional oscillator application of the 555 circuit with a programmable solid-state potentiometer introduces a degree of freedom that allows the computer control of both the frequency of oscillation and the duty cycle. The potentiometer adds variability to the analog circuit and its digital controls, through its computer-controlled serial bus, provides programmability.

For discrete values of R_A and R_B, the frequency and duty cycle are given as

$$f_o = \frac{1.44}{(R_A + 2R_B)C} \quad \textbf{and} \quad DC = \frac{R_A + R_B}{R_A + 2R_B}$$

If R_A and R_B are replaced by kR (wiper resistance to one end) and (1-k)R (wiper resistance to the other end) of the potentiometer, the frequency and duty cycle are given as

$$f_o = \frac{1.44}{(2-k)RC} \quad \textbf{and} \quad DC = \frac{1}{2-k}$$

k is a number that varies from 0 to 1 and reflects the proportionate position of the wiper from one end (0) of the potentiometer to the other end (1). As the wiper is programmed from one end of the potentiometer to the other, the frequency of oscillation will vary from

$$1.44/2RC < f_o < 1.44/RC$$

and the duty cycle will vary from

$$.5 < DC < 1$$

For the circuit values shown, the frequency will vary 725Hz to 1450Hz. The circuit uses Intersil's X9315W which is a 10kΩ potentiometer with 32 taps and a three-wire interface. The number of taps represents the number of programmable wiper positions or frequency and duty cycle values and R (or R_{TOTAL}) is equivalent to $R_A + R_B$. For the Intersil digitally-controlled (XDCP) potentiometers, the number of taps vary from 32 to 256, R_{TOTAL} varies from 1kΩ to 1MΩ, and potentiometers are also available with SPI and I2C interfaces. A wiper setting can be stored in the XDCP's nonvolatile memory permitting the circuit to return to a predetermined frequency and duty cycle value on power-up. The circuit can be used in control, test and measurement, and signal processing applications.
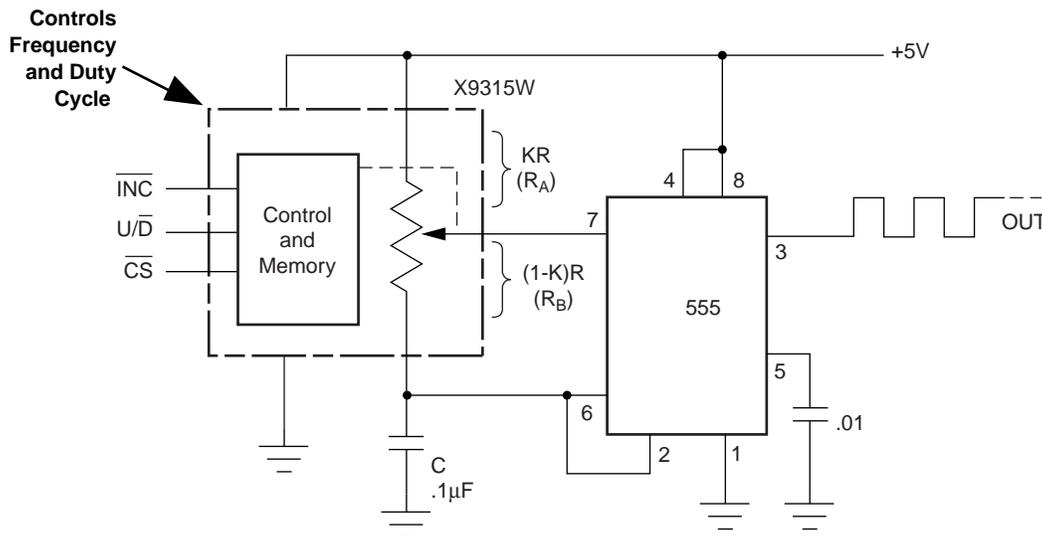
$$f_0 = \frac{1.44}{(2-K)RC} \, , \; 725 \text{ Hz} \leq f_0 \leq 1450 \text{ Hz}$$

$$DC = \frac{1}{2-K} \, , \; .5 \leq DC \leq 1$$

FIGURE 10. 555 RECTANGULAR OSCILLATOR

Phase Shift Sinusoidal Oscillator

The sinusoidal oscillator in Figure 11 is implemented with two all pass filters, A_2 and A_3, and inverting amplifier A_1. The magnitude of the gain for each of the circuits A_1, A_2 and A_3 ($R_3 = R_2$) is ideally one. Hence the magnitude of the loop gain is ideally one. The phase shift of the loop gain is dependent on the phase shift through the all pass filters and it is a function of R, R_1, and C. The frequency where the phase shift of the loop gain is 360° (or 0°) satisfies the condition for oscillation and hence is the frequency of oscillation. An advantage of this configuration is that the frequency of oscillation can be directly controlled by resistances R or R_1 and no gang tuning of elements is necessary like in many popular oscillator circuits.

The ideal loop gain for this configuration is given by

$$AF = G_{A1}G_{A2}G_{A3} = \left(-\frac{R_3}{R_2}\right)\left(\frac{1-sR_1C}{1+sR_1C}\right)\left(\frac{1-sRC}{1+sRC}\right)$$

whose magnitude is

$$|AF| = \frac{R_3}{R_2}$$

and whose phase shift is

$$\phi = -2\tan^{-1}\omega RC$$

The frequency of oscillation can be found by solving for the value that results in 360° phase shift or

$$\omega_o = 2\Pi f_o = \frac{1}{C}\left[\frac{1}{RR_1}\right]^{1/2}$$

The closed loop gain of A_1 ($R_3 > R_2$) is set to greater than one to compensate for the finite values of open loop gain of the amplifiers and to ensure startup. R or R_1 or both resistors can be used to vary the frequency of oscillation. For the values shown, the programmable frequency range is from 1.5kHz to 9kHz. Zener or reference diodes D_1 and D_2 control the amplitude of the signal.
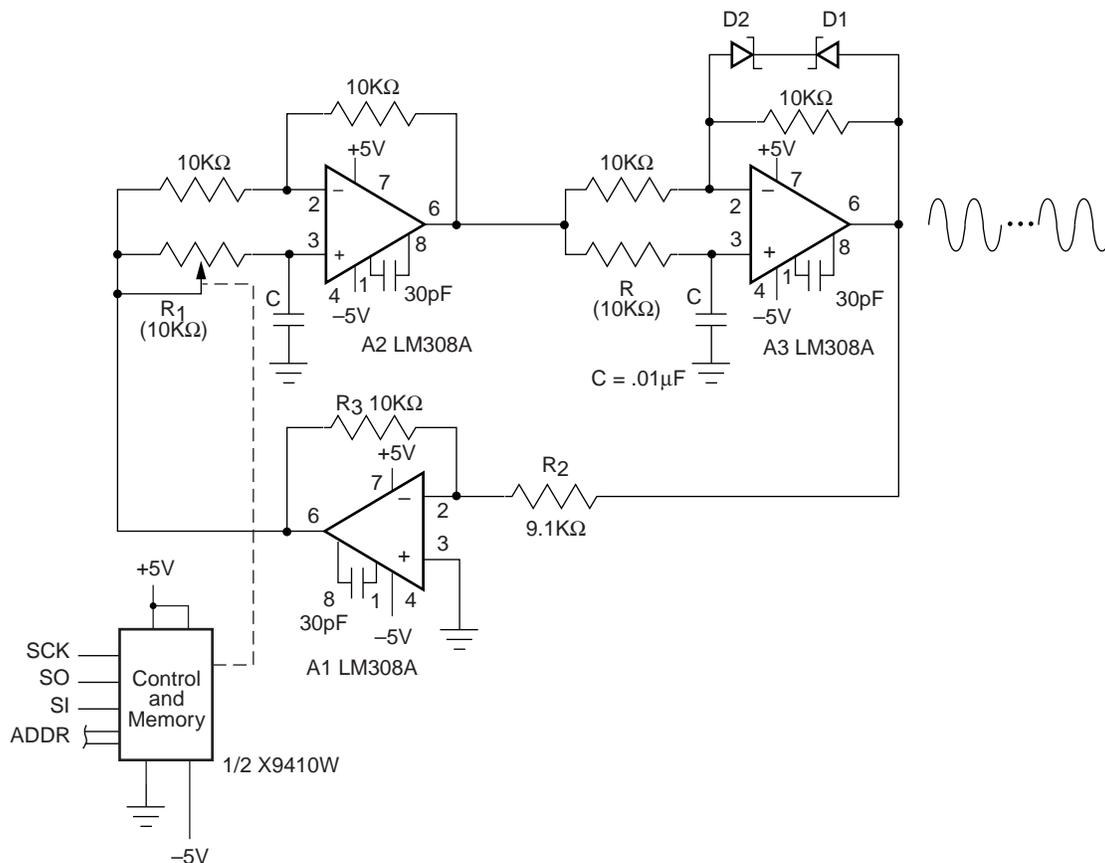
FIGURE 11. PHASE SHIFT SINUSOIDAL OSCILLATOR

I to V Convertor

The circuit in Figure 12 is an input current (I) to output voltage (V) convertor. The feedback portion of the circuit is a tee network of resistive elements consisting of a digitally controlled potentiometer and a fixed resistor R_1(=R). The input–output relationship for the I to V convertor is

$$\frac{V_o}{I_s} = -R\frac{(1 + k - k^2)}{k}$$

where k is a number that varies from 0 to 1 and reflects the proportionate position of the wiper from one end (0) of the potentiometer to the other end (1). The programming of the location of the wiper changes the scale factor between the input current and output voltage without changing the values of any of the resistances and avoids the use of high value resistors in measuring low values of current. As k goes from 1 to 0, the scale factor goes from -R (1) to a theoretical -R(∞). The high impedance output of many transducers, like photodiodes and photovoltaic cells, is modeled as a current source.

The programming of the 100 tap potentiometer provides for a two-decade change in effective resistance thus allowing the circuit to measure at least four decades of current. For the values shown, the circuit can measure current from 1µA to 1mA.
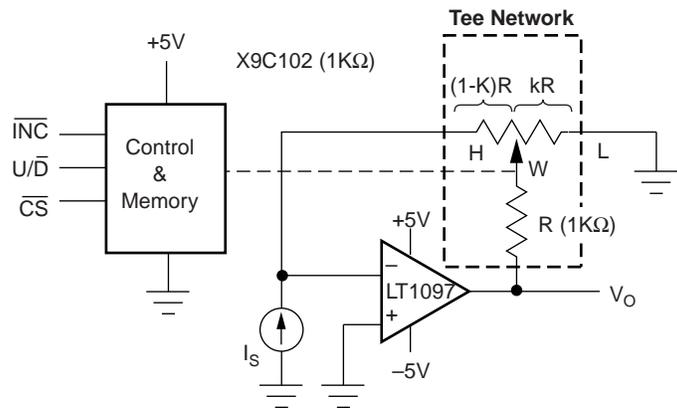
$$\frac{V_o}{I_s} = -R\frac{1 + k - k^2}{k} \qquad (1 - k)R + kR = R = 1K$$

$$1\mu A < I_s < 1mA$$

FIGURE 12. I TO V CONVERTOR

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