AN1101
Rev X.00
March 24, 1998

Designing a High Efficiency DC-DC Converter with the EL75XX

Since the beginning of the digital revolution, the speed of a microprocessor has been governed by Moore's law postulated in 1968 by Intel's co-founder Gorden Moore. Moore suggested that the speed of a microprocessor would double in every 18 months. However, the principle of conservation of energy, more scientific in nature, will eventually dominate and limit the rate at which the speed of a microprocessor is increasing. The equation $P = CV^2F$, a derivative of the principle of conservation of energy, dictates that the power dissipated in a device is linearly proportional to its clock frequency and distributed capacitance. Microprocessor manufacturers have made great advances in reducing the amount of power dissipation in the device. The popular Pentium microprocessor, for example, employs a combination of heat-sink/fan to extract heat from the package. To further combat the power dissipation problem, a new generation of low voltage CMOS fabrication processes have been developed. The low voltage processes have a smaller transistor geometry that results in lower parasitic capacitance, reducing C in the above equation. Smaller transistor size also allows for a increase in the number of transistors in a given die area, and as a result, the lifetime of Moore's law is extended. However, technical problems are being passed onto the shoulders of power supply designers. Lower microprocessor supply voltages and higher supply currents mean that the linear DC-DC regulator is no longer a viable solution. Power supply designers are forced into using switching regulator techniques. Lower output voltage, higher output current, and smaller output voltage ripple requirements have greatly increased the difficulty of the power supply design. To further burden the problem, power saving “stop-clock” modes have demanded faster and more stable transient response from the DC-DC converter.

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Introduction

The purpose of this Application Note is to demonstrate the operation of the EL7560 in an 12.4A output current mode DC-DC converter module for powering Intel's latest microprocessor, the Pentium-Pro. The EL7560 is the world's simplest, most integrated, and most cost effective switcher. It incorporates the PWM functions, current sense resistor, high current synchronous FETs, precision DAC for output voltage programming, and over-voltage and over current protection features. In addition, the advanced control loop design controls the load regulation of the DC-DC converter to meet the P6 DC-DC converter output load transient specification with low cost and readily available Aluminum Electrolytic capacitors.

Lower output current versions of the device are also available. The EL7560 requires an external reference. This gives the application more flexibility and accuracy. A precision ±1/2% reference is incorporated in the EL7561 to reduce component count. The EL7556 is the 6A output current version. The power supply design considerations presented in this Application Note are applicable to all devices in the EL75XX family.

In the component selection sections, all calculations are based on the worst case specification limits in the Intel P6 DC-DC Converter Design Specifications.

EL7560 Theory of Operations

The EL7560 is a current mode switcher which means that the power switch duty cycle is determined by comparing the output inductor current and the error amplifier output voltage. Current mode control offers a number of advantages over the traditional voltage mode control. First, because the inductor current ramp is proportional to the input voltage level the converter can respond quickly to line variations. Second, it greatly simplifies the over-all loop design. The pole introduced by the output inductor is taken out of the loop and replaced by a high output impedance current source which is regulated by an inner current control loop. Lastly, it allows automatic pulse by pulse current limiting which protects the power switches when the output is overloaded or shorted.

The negative input of the error amplifier is brought out to sense the output voltage. The output of the error amplifier is compared with the current ramp from the current sense amplifier. (The current ramp is modified by slope compensation circuitry in order to prevent noise and oscillation problems.) The output of the comparator then resets a flip-flop which terminates the “on” time of an internal power NMOS FET. The error amplifier reference voltage is programmed by a 4-bit DAC with 100mV resolution.

The EL7560 also includes a number of house keeping functions. In the case of overheating, the power switches can be shut off by properly configuring Otbar, pin 13/OT. When the output voltage is within regulation, the power good signal pin will go high. The device can be disabled by pulling output enable (pin 14) low, putting the device in a lower power state. During start-up, the switching duty cycle is limited by the internal soft-start circuit to generate a smooth power converter output response.

The oscillator frequency can be easily set by an external capacitor. The oscillator is designed to operate up to 1MHz switching frequency. External adjustable slope compensation is provided to obtain the best system performance.

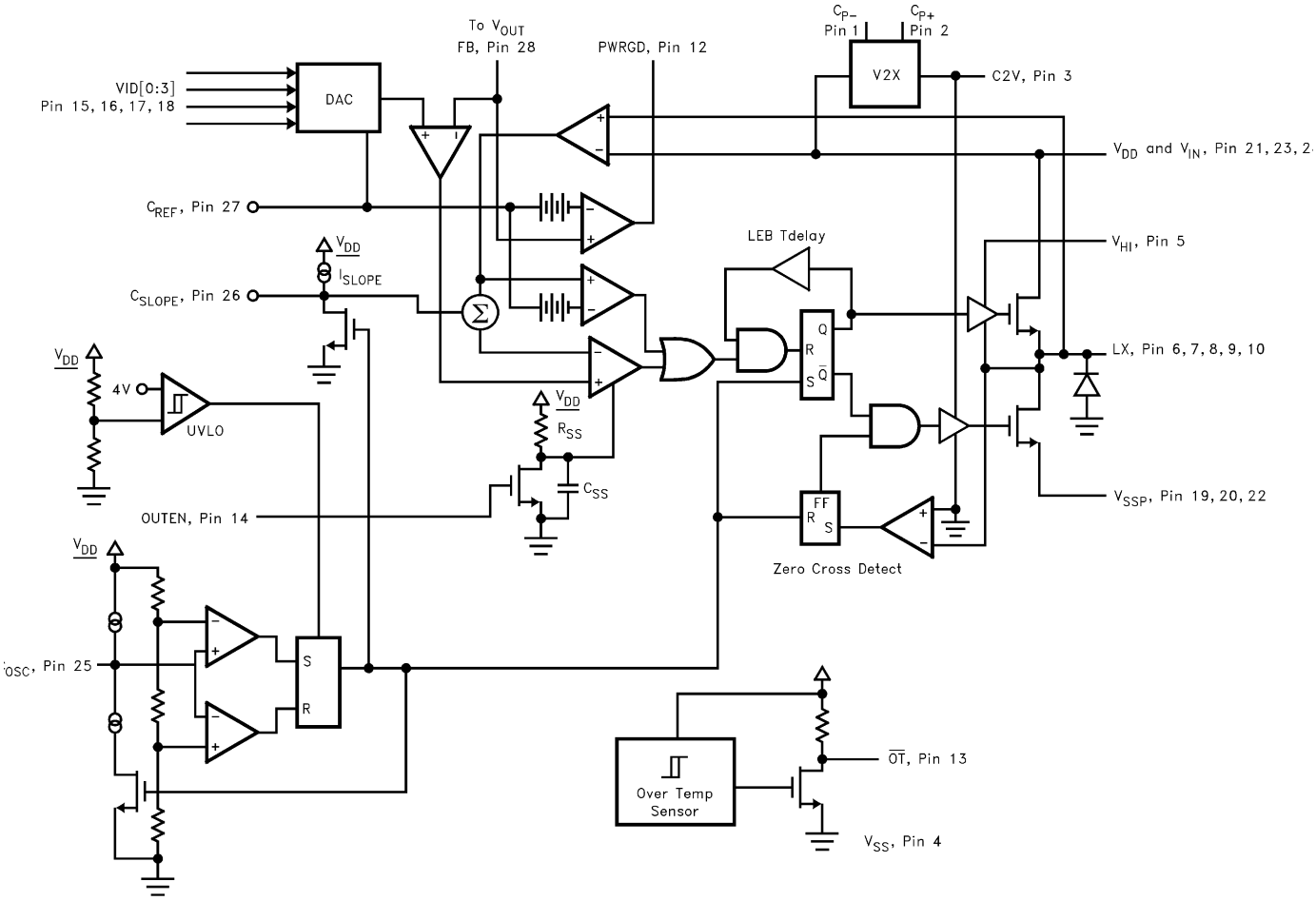


FIGURE 1. EL7560 FUNCTIONAL BLOCK DIAGRAM

Pin Descriptions

PIN #	DESCRIPTION
1, C-	Negative terminal for the charge pump bootstrap capacitor. This pin oscillates from V_{DD} to V_{SS} at one half the clock frequency.
2, C+	Positive input for the charge pump bootstrap capacitor. This pin oscillates from V_{DD} to twice V_{DD} at one half the clock frequency.
3, C2V	Voltage doubler input. A 100Ω resistor is used to limit current into this pin. A 1µF capacitor is also needed to sustain the voltage doubler output. The 1µF capacitor should be returned to the power ground node. The voltage on this pin will be 8V–10V depending on the load.
4, V_{SS}	This pin is the ground input for the control circuitry. It must be separated from the high current power ground. This pin should be connected directly to the ground point of the output capacitors.
5, V_{HI}	This pin is the positive supply for the high side driver. It is bootstrapped from the LX pin with a 0.1µF capacitor.
6, 7, 8, 9, and 10, LX	This is the halfway point between the two large internal FETs. It drives the inductor of the buck regulator circuit. High switching current is seen at this pin.
11, TEST	This pin is used to test the internal power FETs during the final test at the factory. It must be connected to any convenient ground in the application.
12, PWRGD	This pin outputs a high signal (Logical “1”) to signify power good when the FB pin is within 7% of its programmed value.
13, OTbar	This pin pulls low (Logic “0”) when the die temperature exceeds 135°C. It is normally a high impedance output. It has 15°C of hysteresis. To turn off the FETs in the event of an over-temperature condition, simply connect this pin to the OUTEN pin and a 10kΩ resistor to V_{DD}.
14, OUTEN	A high input signal applied to this pin enables the switching regulator. The reference, oscillator, and voltage doubler operate whenever the power supply is above its UVLO threshold regardless of the state of this pin.
15, 16, 17, and 18 $V_{ID3, 2, 1, and 0}$	These are the DAC input pins used to program the output voltage.
19, 20, and 22, V_{SSP}	These pins are the ground returns to the buck regulator. They are internally connected to the source of the low side synchronous NMOS FET.
21 and 23, V_{IN}	These pins are the positive power supply input to the buck regulator. They are internally connected to the drain of the high side synchronous NMOS FET.
24, V_{DD}	This pin supplies power to the internal control circuitry. It typically draws 30mA when operating.
25, C_{OSC}	A capacitor connected from this pin to ground sets the frequency of the PWM oscillator. The oscillator frequency is approximately $F_{OSC} = 0.001/C_{OSC}$. The maximum duty cycle is fixed at 96%.
26, C_{SLOPE}	A capacitor connected from this pin to ground sets the amount of slope compensation. A 30µA current flows out of this pin. The voltage at this pin is reset to the reference voltage whenever the high side NMOS FET is off.
27, C_{REF}	This is the external reference input pin. A minimum of 1.0µF to ground is recommended.
28, FB	This is the voltage feedback input pin for the buck regulator. It is internally connected to a resistor divider.

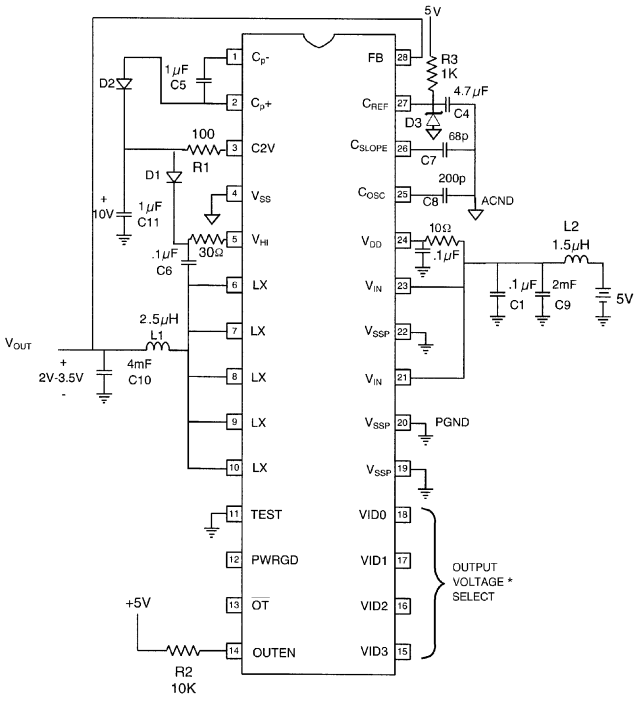


FIGURE 2. P6 DC-DC CONVERTER CIRCUIT

Basic Buck Regulator Topology

Figure 3 shows the basic buck regulator topology. When Q1 turns on the voltage across L1 is V_{IN} - V_{OUT} and current flows from V_{IN} to V_{OUT}. When Q1 turns off, the inductor current continues to flow, and as a result the cathode of D1 gets pulled below ground by the back EMF of the output inductor, L1, and starts to conduct. The voltage across L1 is $-V_{OUT}$ and output current flows through D1 and L1 to V_{OUT}. Under steady-state conditions, the voltage across L1 must average to zero. If T1 is the time Q1 is closed, and T2 is the time Q1 is open, then the relationship between V_{IN} and V_{OUT} is:

$$(V_{IN}-V_{OUT})T1-(0-V_{OUT})T2 = 0 \quad (1)$$

Equation (1) can be simplified to

$$V_{OUT} = V_{IN} \bullet D \quad (2)$$

Where D is the duty cycle, D = T1/(T1 + T2)

Equation (2) tells us a great deal about switching mode converters. First, it suggests that the output voltage is solely a function of V_{IN} and the duty cycle of the switch. Secondly, it is not a function of the output inductor, capacitor or switching frequency. Lastly, it is not a function of the magnitude of the output load current.

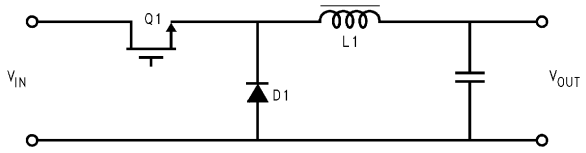


FIGURE 3. BASIC BUCK CONVERTER TOPOLOGY

Synchronized Rectification

The diode in Figure 3 may be replaced by a switch to further improve efficiency. As an example, if I_{OUT} is 12.4A and the forward bias voltage of the diode is 0.6V, and the duty cycle is 60%, the total power dissipation of the diode is 0.6V • 12.4A •(1 - 0.6) = 2.97W. This represents 8% of the efficiency loss in a 3V output converter. If the diode is replaced with a low “on” resistance power FET(Q2) as depicted in Figure 4, the power loss is determined by the “on” resistance of Q2. The “on” resistance of the power FETs in the EL7560 is typically 20mΩ, at 12.4A and 60% duty cycle the power loss is 12.4A • 12.4A • 20mΩ • (1 -0.6) = 1.23W which is a 1.69W efficiency improvement over the diode configuration. A Schottky doide, D3 in the PC DC-DC coverter schematic, in parallel with drain-source terminals of Q2 is often required to provide the inductor current path during the transient when both Q1 and Q2 are turned off. With this Schottky diode, the body diode of Q2 will never forward bias, thereby improving the reliability of the converter.

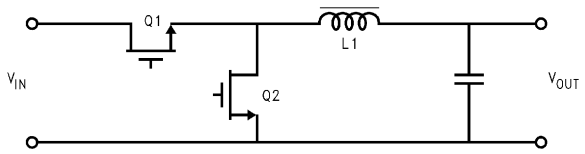


FIGURE 4. BUCK CONVERTER WITH SYNCHRONIZED SWITCHES

Continuous Mode Operation

The preceding discussion describes the situation where the inductor current never reaches zero. This form of operation is called “continuous” mode. Figure 5 depicts Q1 and Q2 gate drive waveforms, Q1 drain and Q2 source current waveforms, and the output inductor currents.

During T1, Q1 is turned “on” and Q2 is turned “off”, inductor current IL1 and $I_{SOURCE1}$ increase from the initial value which is not zero. The slope of the current ramp is dictated by

$$\frac{\Delta ID(Q1)}{\Delta T} = \frac{V_{IN} - V_{OUT}}{L1} \qquad (3)$$

In this cycle, energy is stored in the inductor for use during the off cycle and current flows from input to the output.

During T2, Q1 is turned “off” and Q2 is turned “on”, inductor current IL1 continues to flow to the output via Q2. Inductor current declines to the initial value and gives up energy to the output.

Discontinuous Mode Operation

Normally, a converter designed for the continuous mode operation stays in continuous current mode under all load conditions. However, the converter can go into discontinuous current mode momentarily when the output load is changed from its maximum to minimum level. The mode of operation where the inductor current falls to zero is called discontinuous operation. The waveforms in Figure 6 are synchronized gate drive waveforms, power FET source current and output inductor current waveforms. During T1, Q1 turns “on” and Q2 turns “off”, the inductor current starts from zero and rises to the peak value I_P. Energy, $P = LI^2/2$, is stored in the inductor. During T2, Q1 turns “off” and Q2 turns “on”, inductor voltage reverses and its stored energy is delivered to the output. The inductor current decreases linearly to zero. When the inductor current reaches zero, Q2 must turn “off” to prevent inductor current flow from the storage capacitor to ground. Thus, during T3, both Q1 and Q2 are turned “off”.

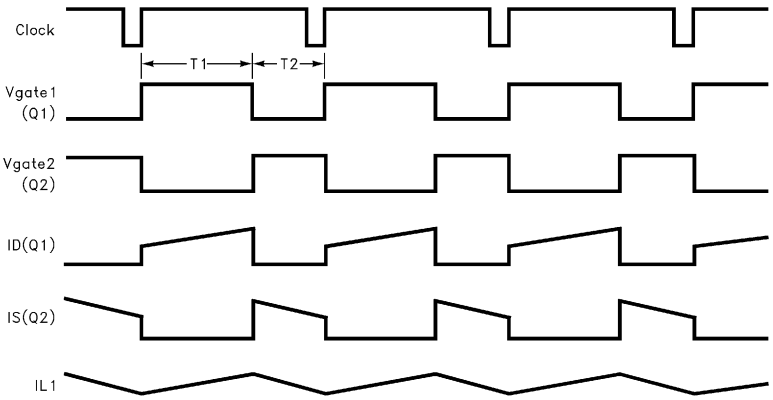


FIGURE 5. GATE DRIVE AND CURRENT WAVEFORMS UNDER CONTINUOUS MODE

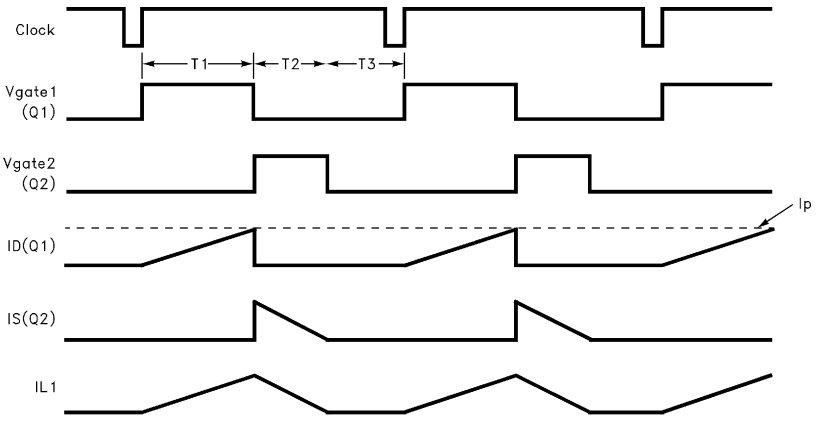


FIGURE 6. GATE DRIVE AND CURRENT WAVEFORMS UNDER DISCONTINUOUS MODE

Current Mode Control

The advantages of current mode control were discussed in an earlier section. It basic block diagram is shown in Figure 7. The duty cycles of the power FETs are generated by comparing the error amplifier output voltage with a sawtooth ramp. This sawtooth ramp is provided directly from the power switching circuit inductor current waveform through a current sense resistor, R_{SENSE}. The fact that the slope of the current ramp is a function of V_{IN}, V_{OUT}, and the output choke inductance, $V_{IN} - V_{OUT} = L\ \Delta I/\Delta T$, suggests an inherent voltage feed forward characteristic with instantaneous open loop response to any input voltage changes. The output inductor pole is included in the current loop, and as a result, it is eliminated from the outside voltage loop. This reduces the output filter from a two pole network to a simple single pole. The outer loop is a voltage loop where the output voltage, V_{OUT}, is compared with a reference voltage, V_{REF}, and produces an error voltage output for the PWM comparator. An interesting aspect of the current mode control scheme is that the error amplifier output voltage programs the inductor current which causes the output voltage to rise or fall and the error amplifier output voltage is derived from comparing V_{OUT} with V_{REF}. The result is that the PWM duty cycle maintains the inductor current such that V_{OUT} is equal to V_{REF}.

Slope Compensation

While current mode control has a number of desirable characteristics, it also carries a flaw which, if not treated properly, can cause severe output oscillation. As described in the previous sections, current mode control regulates the peak inductor current via the inner current loop. However, in a buck converter, the output current is the average inductor current.

Figure 8 graphically represents the output inductor current using two different input voltages. When in regulation, the error amplifier output voltage, V_E, should not change. A constant V_E (V_E sets the peak output inductor current level) implies that the average output current for the higher input voltage level (duty cycle = D1) is slightly higher than the output current associated with the lower input voltage (duty cycle = D2). This will result in a higher output voltage which the voltage loop will correct by changing V_E, which in turn will result in a different duty cycle, which results in different average current levels. This effect has been dubbed sub-harmonic oscillation and can be evidenced by output voltage oscillation at one half the switching frequency.

One method of maintaining constant output current is to add a voltage ramp on the current sense output as depicted in Figure 9. This has the effect of lowering the error amplifier voltage as a function of T_{ON}.

Slope compensation also improves noise immunity. Figure 10 demonstrates how a small perturbation in the inductor current can result in an unstable condition. For a duty cycle less than 50%, the perturbation is suppressed quickly each cycle ($dI'1 \leq dI1$). For greater than 50% duty cycle, a small perturbation is amplified ($dI'2 \geq dI2$) each cycle and causes an unstable condition.

Figure 11 shows the inductor current perturbation problem being corrected with slope compensation. With slope compensation, inductor current perturbation is attenuated each cycle at all times even when the duty cycle is greater than 50%.

In the EL7560, a slope compensation ramp is created with a 30µA current source charging an external capacitor, C_{SLOPE}.

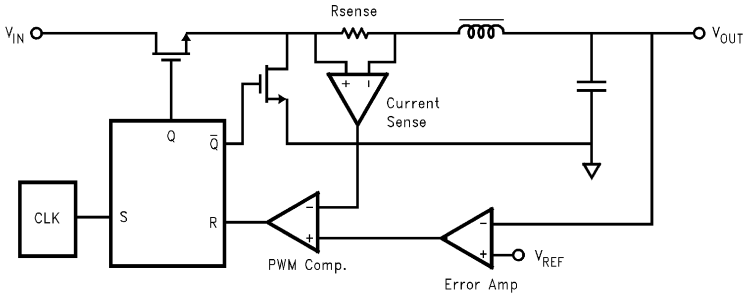


FIGURE 7. CURRENT MODE CONTROL

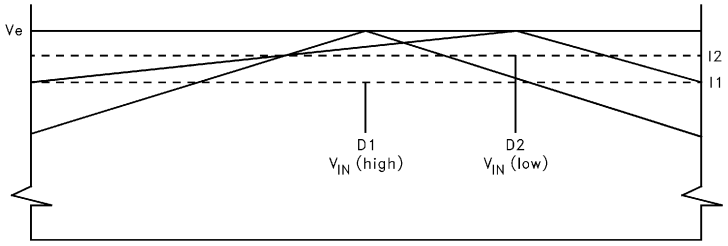


FIGURE 8. PEAK CURRENT MODE CONTROL ERROR

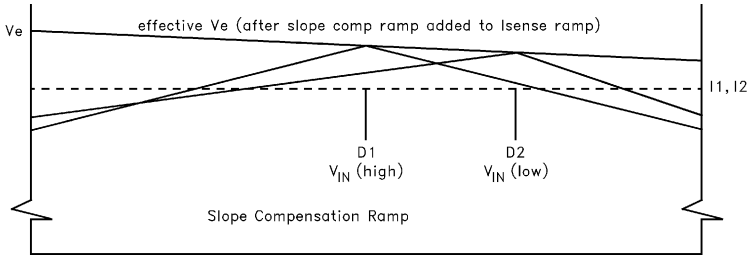


FIGURE 9. CONSTANT AVERAGE OUTPUT CURRENT

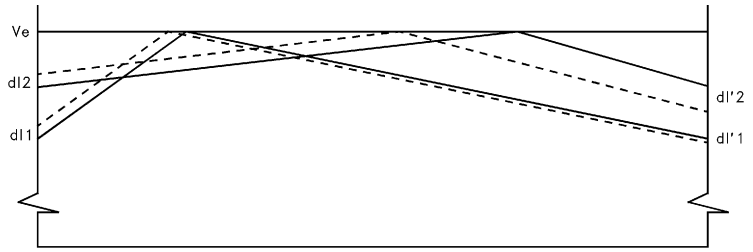


FIGURE 10. INDUCTOR CURRENT ERROR

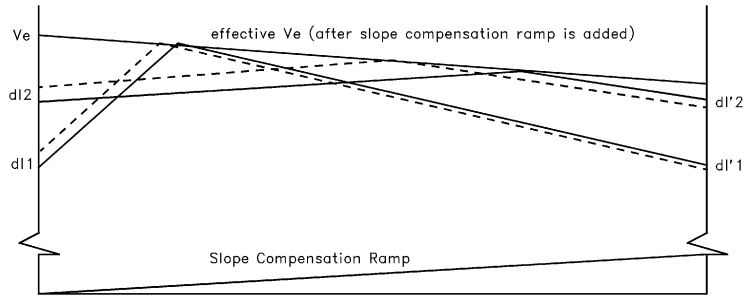


FIGURE 11. INDUCTOR CURRENT RAMPS WITH SLOPE COMPENSATION

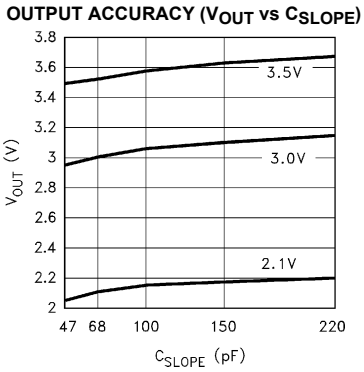


FIGURE 12. a

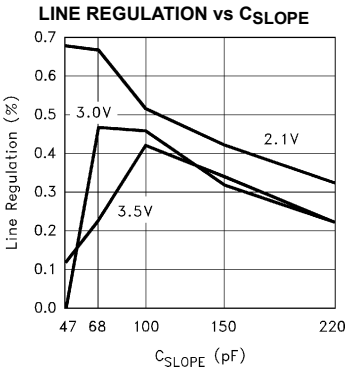


FIGURE 12. b

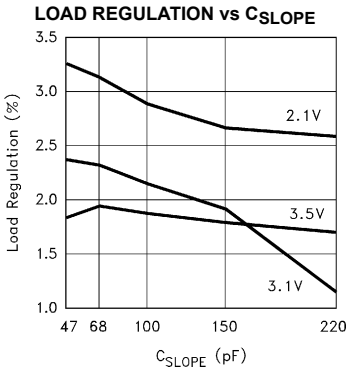


FIGURE 12. c

The voltage on C_{SLOPE} is reset to the reference voltage whenever the internal high side NMOS FET is off.

Note 1: Figure 12 shows the experimental test results of the effects of the amount of slope compensation on the output voltage accuracy, output load regulation, and line regulation. The fact that slope compensation limits the duty cycle becomes apparent in Figure 12a. A C_{SLOPE} is decreased, the slope of the current ramp increases as a result the duty cycle is decreased and thus the decrease in output voltage.

PWM Comparator

In the heart of the EL7560 PWM section is a direct summing comparator. The regulator output is first compared with a reference (DEC output) voltage. The resultant error voltage is then compared with current sense signal and slope

compensation ramp. PWM duty cycle is then adjusted according to the summing comparator output. The direct-summing scheme enables cycle by cycle control of the output voltage. This scheme also eliminates the traditional feedback compensation integrator. The dominant pole is set by the output capacitor and the equivalent output resistive loading.

Output Inductor, L1

The output inductor serves two purposes, it stores energy and filters output ripple current. Trade-offs often have to be made between the physical size of the inductor and the maximum energy storage. The primary criterion for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode operation under all line and load conditions. To maintain the conditions of continuous mode operation under the minimum load and maximum line condition (duty cycle is at its minimum) at 500kHz switching frequency, the minimum inductance can be calculated with the following equation:

$V = L \bullet \Delta I/\Delta T$

where

V is the voltage across the inductor,

$V = 5.25–3.07 = 2.13V$

(The Worst case P6 DC-DC converter specifications are used in all calculations.)

L is the inductance required to maintain continuous mode operation

ΔI is the peak ripple current,

$\Delta I = 2 \bullet I_{OUT(min)} = 0.6A$

ΔT is the duration at which the current is ramping up in the inductor, or the “on” time of the PWM,

$\Delta T = (3.07/5.25)/500kHz = 1.17e\text{-}6$

$L = V \bullet \Delta T/\Delta I = 2.13 \bullet 1.17e\text{-}6/0.6 = 4.15\mu H$

One inductor which meets this criterion is the Pulse Engineering PE-53681. Its inductance is 4.2µH at minimum output current. The saturation effect of the magnetic core causes the inductance to decrease. At the maximum output current of 11.4A, the inductance of the PE-53681 decreases to 2.5µH. As a result the ripple current will increase at high output current,

$I = V \bullet \Delta T/\Delta L = 2.13 \bullet 1.17e\text{-}6/2.5e\text{-}6 = 1A.$

When selecting the output filter capacitor, the worst case 1A ripple current must be used when calculating the output ripple voltage.

There are two important criteria in selecting an output inductor:

1. The minimum inductance at zero DC current must be greater than the inductance required to maintain continuous mode operation.
2. The core size and wire gauge must be sufficient to handle the maximum output DC current.

Output Capacitor, C10

The output capacitor filters the output inductor ripple current; thus, it must be low ESR type electrolytic capacitor. One must carefully decide between cost, size, and quality (ESR) of different types of capacitors. Names of capacitor manufacturers are listed at the end of this Application Note. The calculations shown below are done with the low cost United Chemi-Con LXF series Aluminum Electrolytic capacitors. The module layout available in the appendices of this document can accommodate both the high quality OS-Con capacitors or the inexpensive United Chem-Con capacitors.

As stated previously, the output capacitors must be low ESR type for two reasons: 1) to ensure lower ripple voltage 2) to meet the load transient specifications.

1. The Intel P6 DC-DC converter specification calls out for a maximum of ±1% output voltage ripple. For a 3V output that corresponds to 60mV peak to peak. The previous inductor calculation section shows the ripple current to be 1A at the maximum load, thus, the maximum ESR allowed is 60mΩ. For this example we have chosen 6 pieces of 680µF United Chemi-Con series LXF aluminum electrolytic capacitors (part # LXF16VB681M10X12FT). The total capacitance is 4mF and their combined ESR is 10.33mΩ. The resultant peak to peak ripple voltage under full load condition is 10.33mV.
2. When the output is stepped from minimum to the maximum level, the full output current load step will initially be supplied from the output capacitor C_o (I_C), as shown below,

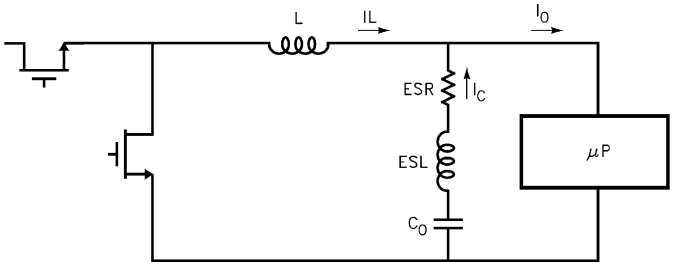


FIGURE 13. OUTPUT CURRENT PATH DURING TRANSIENT

The initial voltage droop will be:

$$\Delta V_{OUT} = ESR \bullet I_{TRANSIENT} + ESL\frac{\Delta I}{\Delta T} \qquad (4)$$

Cylindrical aluminum electrolytic capacitor typically has 5nH of ESL. The combined effective equivalent series inductance is

5/6nH. The change in output voltage due to ESR and ESL during the initial output current transient is,

ΔV_{OUT} = 10.33mΩ • (12.4-0.3) + 5/6nH • 30A/µs = 153mV

Immediately after load transient, C_o will continue to supply current to the output load until the inductor current ramps to the maximum 12.4A output current level. The internal FET will be switching at 96% duty cycle until the output voltage gets back to within regulation. The amount of time for the inductor to ramp up to 12.4A is,

$$\Delta T = \frac{L \bullet \Delta I}{V_{IN} - V_{OUT}} = \frac{2.5\mu H \bullet 12.1A}{2.1} = 14.4\mu s$$

Taking the 96% duty cycle into account:

ΔT = 14.4µs/0.96 = 15µs

In 15µs the output voltage drops to:

$$dV = \left[1/C_o \bullet \int_0^{15\mu s}\left(12.4 - 0.3A - \frac{dI}{dt}t\right)dt\right] + (12.4A - 0.3A) \bullet ESR$$

dI/dt = (V_{IN}–V_{OUT})/L = (5–2.9)/2.5µH = 0.84A/µs

Plugging in the numbers to equation (4) yields:

dV = 146.7mV

The output drop caused by the output capacitor discharging is less than voltage drop due to ESR and ESL of the output capacitor.

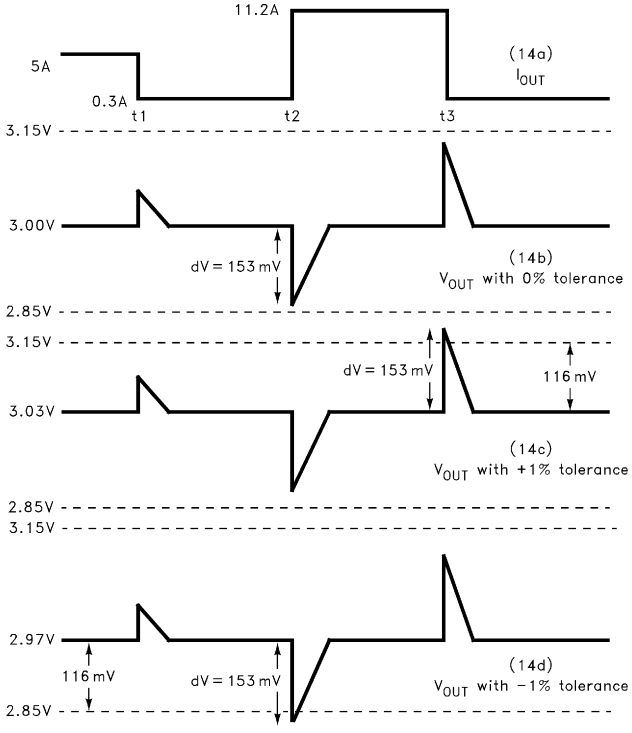


FIGURE 14. OUTPUT VOLTAGE VARIATION WITH TRADITIONAL CONTROL SCHEME

The total ΔV_{OUT} transient allowed by the Intel spec is ±5%. If we subtract 1% for the tolerance of the EL7560 reference we end up with only 4% of the 2.9V which is 116mV which is less than the 153mV that we calculated. However, the unique loop compensation of the EL7560 degrades the load regulation by ±2% so that at maximum load the output voltage is 2% lower than nominal and at minimum load the output voltage is 2% higher than nominal. The result is 58mV of additional output voltage head room to move around during load transient.

The timing diagrams in Figure 14 show how the output voltage changes in a converter with the traditional control scheme. The converter output current, waveform 14a, is changed from the nominal level (5A) to the minimum (0.3A) then to the maximum (12.4A) then back to 0.3A again.

Figure 14b depicts the output voltage response for a control IC with infinite open loop gain and the error amplifier reference voltage is exactly at 3.00V. The infinite open loop gain gives us the perfect load regulation, i.e., the output voltage always settles to 3.00V under all conditions. dV = 153mV is a result of ESR and ESL of the output capacitor. Equation (4) is the equation and derivation.

Figure (14c) and (14d) show output transient effects with ±1% tolerance on the error amplifier, 153mV of voltage change at the output gets out of the ±5% output voltage limit called out in the Intel P6 DC-DC converter design specification.

The EL7560 utilizes a unique error amplifier compensation technique to control the load regulation. The Intel spec allows a 4% total output change with loading. The load regulation is set such that at minimum output load (0.3A) the output voltage is 2% higher than nominal (5A) and at maximum load (12.4A) the output voltage is 2% lower. The result is an additional 2% (60 mV) of head room for transient load response. Figure 15 shows the transient response waveforms.

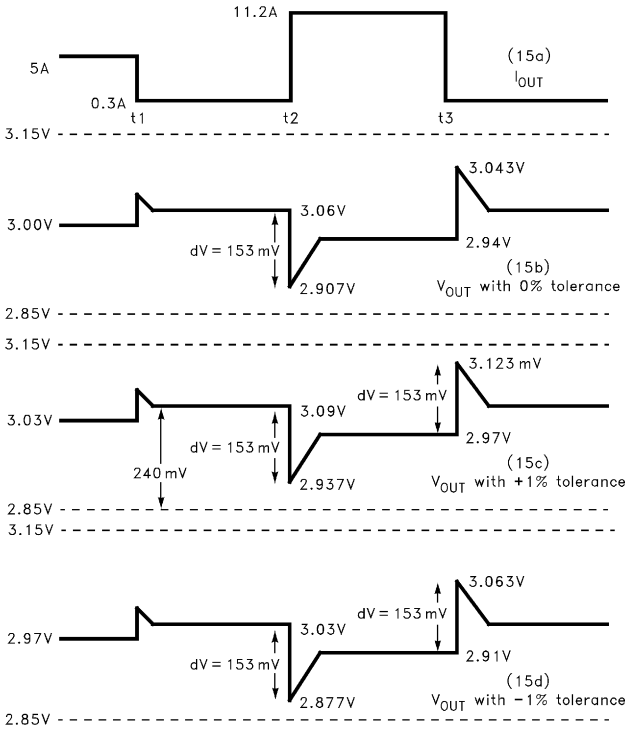


FIGURE 15. EL7560 TRANSIENT OUTPUT VOLTAGE RESPONSE

In summary, if the load regulation is properly controlled, i.e., at minimum load the output voltage is 2% (60mV) higher than nominal load (5A) and at maximum load the output voltage is 2% (60mV) lower than nominal load, we can fit the output transient response curves within Intel's ±5% window under any conditions.

Input Filter/Input Current Transient Analysis

A 1µH inductor in series with the input capacitor is required to meet the Intel “Load Transient Effects” specification which states that, “During this step response (the output load is switching from 0.3A to 12.4A) the input current di/dt shall not exceed 0.1A/µs.” The input filter inductor is absolutely necessary in the standard buck topology. The simulation results of input transient current during output load changes are shown in Figure 16. As the input inductance increases, the slope of the input transient current decreases.

In the Elantec module reference design, a custom inductor is used. The core of the inductor is Micrometals T30-26 and the wire gauge is AWG#20 with 7 turns. The inductance value is 1.6µH. For users who want to use an off the shelf inductor we suggest the Pulse engineering PE53188. Its inductance spec is 2.2µH at 6.4A.

Figure 16 shows the simulated input current response for various combinations of the input inductor and capacitor. The simulation result shows that a 1.5µH inductor and a 2mF capacitor combination suffice to meet the Intel input transient specification.

Over-Voltage Protection

The over-voltage condition is defined by Intel as the situation when the output voltage goes 10% higher than the programmed level. Upon detection of an over-voltage fault, the internal high side FET is turned off. A clamping diode D4 from the LX pin back to the input is recommended to keep the LX pin a diode voltage drop above the input. The switcher recovers automatically when the over-voltage fault is removed.

Over-Current Protection

The EL7560 has a built-in over-current protection feature. When an over-current fault occurs, the high side FET automatically turns off. The switcher recovers automatically when the over-current fault is removed.

Efficiency Calculations

Most of the power dissipated in the EL7560 is due to the “on” resistance of the power FETs. Each power FET exhibits a typical 30mΩ “on” resistance; therefore, the power loss is $P = I^2R = 12.4 \cdot 12.4 \cdot 0.030 = 4.61W$ (at rated maximum load).

Efficiency curves of the typical VRM demo module is depicted in Figure 17. The curves show low efficiency at both ends of the output loading. At the low output current end, switching losses of the switcher is high relative to the output power. At the high output current end, the on-resistance of the power MOSFET dominates.

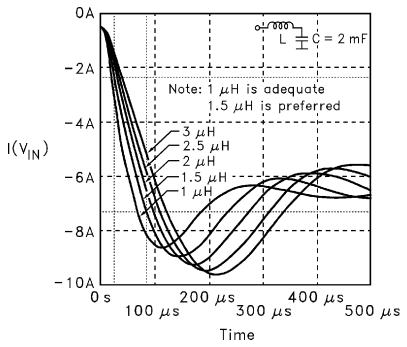


FIGURE 16. INPUT FILTER TRANSIENT RESPONSE

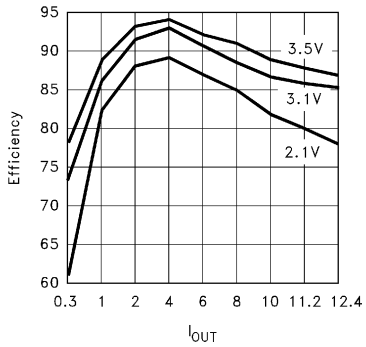


FIGURE 17. VRM EFFICIENCY

Heat Sinking Requirements

For reliability reasons, the Intel spec requires that the junction temperature of the EL7560 be kept below 115°C with the ambient temperature at 50°C and 100 LFM air flow. The minimum θ_{JA} required is:

θ_{JA} = (115–50)/4.61W = 14.1°C/W

The θ_{JA} for the 28-pin PSOP2 without a heat sink is 52°C/W, and the θ_{JC} is 5°C/W. The θ_{JC} of the device combined with the thermal resistance of the heat sink must be less than 17°C/W. Thermal analysis has been done with Wakefield 8052–60 mounted on top of the package with Ablebond 84–1 LMIT epoxy adhesive which has 0.2°C/W thermal resistance. With a board size of 1.5 x 3 and an air flow of 100LFM, measurements made by Elantec yield a θ_{JX} is 12.9°C/W.

Board Layout Considerations

Grounding Issues

Figure 18 is the simplified circuit of the power system.

When the high side FET is turned on, Figure 19 shows current flow directly from the AC/DC power supply and the input capacitor through the high side FETs to the load. The ground return current splits into two directions: 1) from the load directly to the AC/DC power supply 2) from the load into the DC-DC module and to the ground of the input capacitor.

When the low side FET is turned on, most of the output load current flows through the low side FET. Current from the AC/DC power supply continues to flow into the input capacitor, whose magnitude (around 8A at maximum output load) is the same as the ground return current from the load. The 12.4A of output current is a combination of current from the input capacitor and the ground input of the DC-DC module.

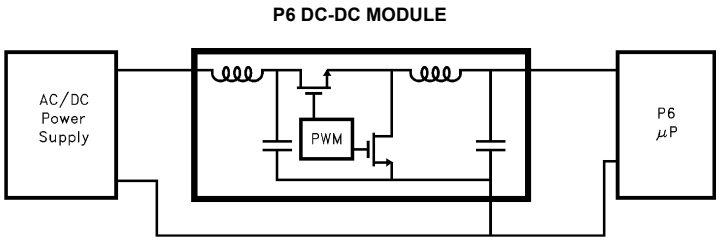


FIGURE 18. A SIMPLIFIED POWER SYSTEM BLOCK DIAGRAM

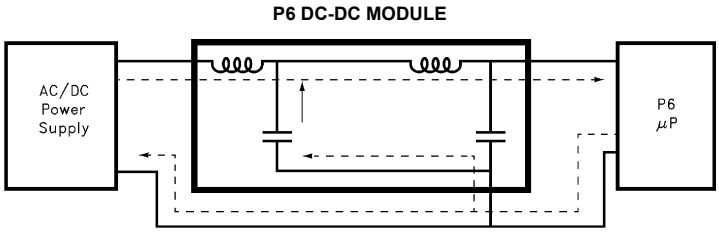


FIGURE 19. CURRENT FLOW PATH WHEN HIGH SIDE SWITCH IS ON

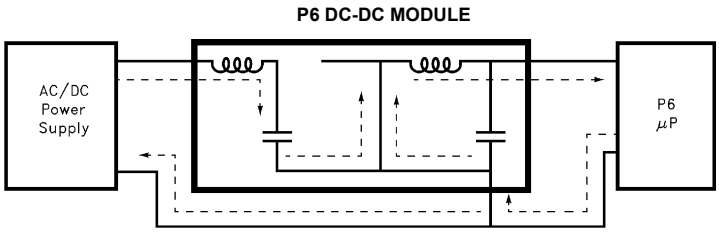


FIGURE 20. CURRENT FLOW PATH WHEN LOW SIDE SWITCH IS ON

Figure 21 summarizes the magnitudes and directions of currents at various nodes in the DC to DC converter under the maximum output loading condition. The DC-DC module input and output current, and AC/DC power supply ground return current, and load return current are constant under steady state conditions.

The current path in the above figures show that the power ground pin, V_{SSP}, V_{IN}, and LX pins, which are switching at 500kHz, are thus extremely noisy. They should be isolated from the logic control and reference of the PWM controller. The ground pin of the output capacitor, C10, is the quietest point in the converter. We recommended splitting the signal ground and power ground at the ground pin of the output capacitor.

The V_{SS} pin and ground connection for C4, C7 and C8 should all be connected to the signal ground.

A 12.4A DC-DC converter reference layout is included in the appendices section of this application note. Proper grounding and layout techniques discussed above are demonstrated in this design.

Charge Pump Design

The EL7560 has an internal voltage doubler and a bootstrap charge pump to generate the high voltage required to switch on the internal high side N-channel FETs. C5, the 1µF capacitor from pin 1 to 2, is the voltage doubler pump capacitor. It charges C11 through D2. A ceramic capacitor is adequate for C5. D1 and C6 are the bootstrap diode and capacitor. When the low side FET is turned on, capacitor C6 is charged to 10V, when the high side FET switch on the V_{HI} pin is bootstrapped to 15V. Capacitor C11 holds the voltage doubler output voltage and the 100Ω resistor R1 limits the current into the low side FET drivers inside the chip. A 1N914 type diode suffices for both D1 and D2. The most critical specification for selecting this diode is its reverse breakdown voltage which should be greater than 15V. In addition, a low forward voltage drop is desired to generate a higher voltage level for the high side drive. If a 12V supply is available, then the charge pump diode and voltage doubler capacitor can be eliminated. Figure 22 shows the circuit implementation.

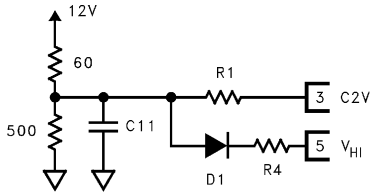


FIGURE 22.

Remote Sense

Although it is not specified in Intel P6 DC-DC converter design guide, remote sensing is often desired in many applications. In the case of a 200MHz P6 microprocessor, the supply current can reach over 12.4A. A 10mΩ of trace resistance results in a 124mV of voltage drop from the converter output to the microprocessor supply pin. A simple method of implementing remote sensing is depicted in Figure 23.

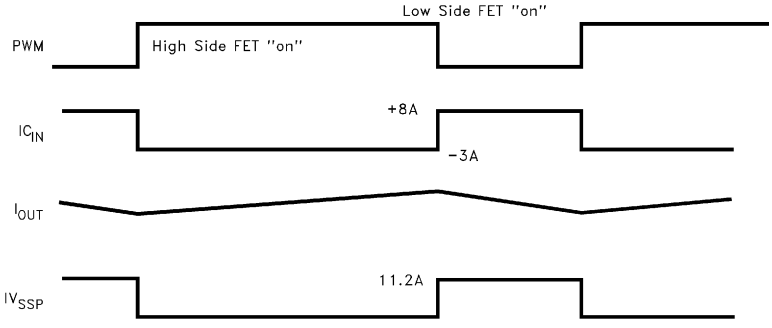


FIGURE 21.

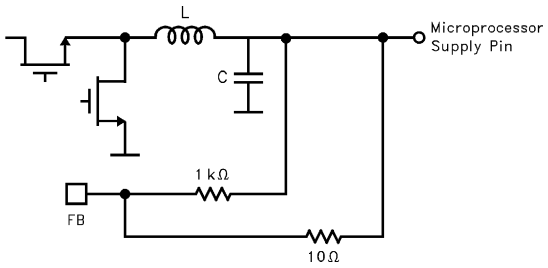


FIGURE 23.

The 1kΩ resistor is connected directly to the converter output and the 10Ω remote sense resistor should be tied directly to the load or the microprocessor supply input pin.

Bill of Materials

DESCRIPTION	QTY
C10, United Chemi-Con, LXF16VB681M10X20LL, 80µF	6 pcs
C9, United Chemi-Con, LXF16VB681M10X20LL, 680µF	3 pcs
L1, Pulse Engineering, Inductor, PE-53681, 2.5µH	1 pc
C4, C6, Chip Capacitors, 0.1µF	2 pcs
C7, Chip Capacitors, 400pF	1 pc
C8, Chip Capacitors, 200pF	1 pc
C5, C11, Chip Capacitors, 1µF	2 pcs
D1, D2 SMT Diode, 1N914	2 pcs
L2, Inductor, 1.5µH, Micrometals T30–26, 7T AWG#20	1 pc
R1, 100Ω	1 pc
R2, 10kΩ	1 pc
R3, 1K	1 pc
R4, 30Ω	1 pc
AS1004, 1.235V Reference Diode	1 pc
Heat Sink—Wakefield Engineering, 8052-60	1 pc

Appendices

Package outline

Core and Inductor Manufacturers

Magnetic Cores
Micrometals
1190 N. Hawk Circle
Anaheim, CA 92807
Phone 800-365-5977

Inductors
Pulse Engineering
P.O. Box 12235
San Diego, CA 92112
Phone 619-672-8100

Inductors
Pan Technology Ltd.
Unit 11, 6/F Proficient Industrial Center (Block A)
6 Wang Kwun Road
Kowloon Bay, Hong Kong
Phone 852-2758-5759
Fax 852-2758-5761

Capacitor Manufacturers

Aluminum Electrolytic Capacitors
United Chemi-Con
9801 West Higgins Road
Rosemont, IL 60018
Phone 708-696-2000

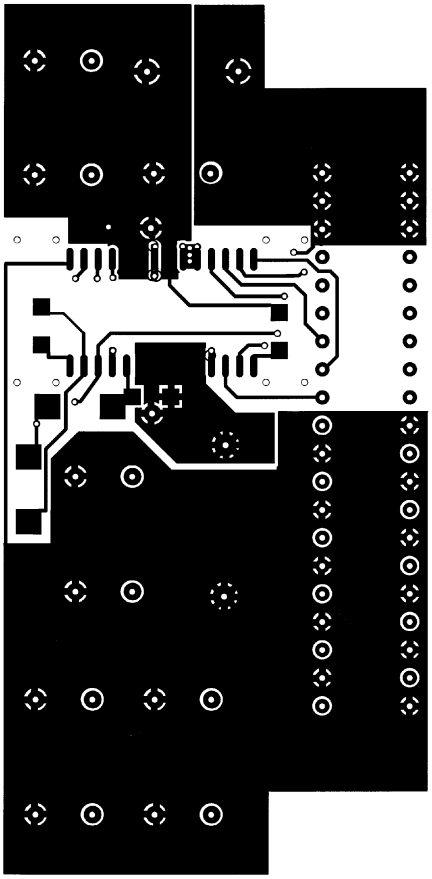
Solid Tantalum Chip Capacitors/OS-Con
Solid Aluminum Capacitors
Sprague
678 Main Street
Sanford, ME 04073
Phone 2070324-7223

Heat Sink Manufacturers

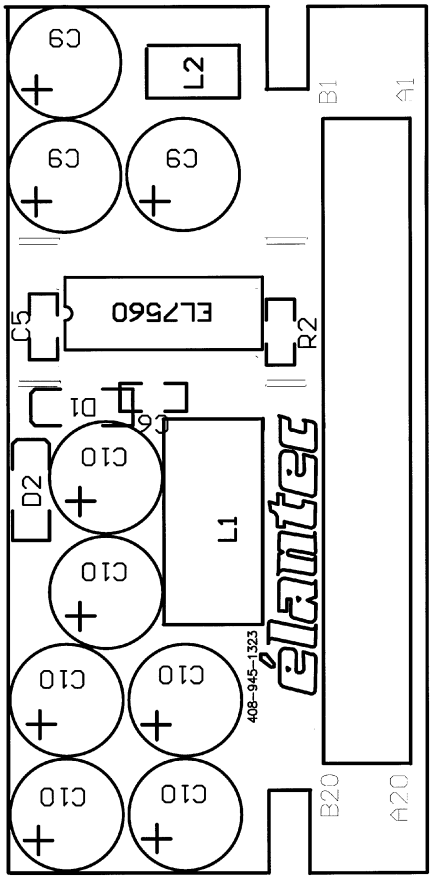
Heat Sink and Mounting Clip
Pan Technology Ltd.
Unit 11, 6/F Proficient Industrial Center (Block A)
6 Wang Kwun Road
Kowloon Bay, Hong Kong
Phone 852-2758-5759
Fax 852-2758-5761

Heat Sink
Wakefield Engineering

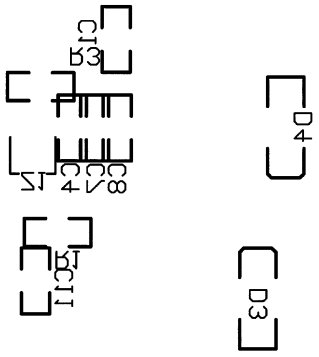
TOP LAYER



TOP LAYER SILKSCREEN



BOTTOM LAYER SILKSCREEN



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