

Principles and Applications of the ICL7660 CMOS Voltage Converter

Introduction

This application note describes a device originally designed to solve the specific problem of needing a negative supply when only a positive supply is available. This is very common, and occurs, for example, in systems using dynamic RAMs where the three-supply devices require a low current body bias supply of around -5V. Negative supply voltage is also desired in systems with a lot of digital logic (at +5V) but containing a small analog section using A/O converters, such as the ICL7107 or ICL7109 and/or op amps and comparators, operating on ground referenced signals. In all these cases, the current requirement and regulation are not very demanding, but nevertheless, generating such a -5V supply is usually expensive and inefficient. Typically, a large number of discrete and integrated-circuit components are needed to convert the common +5V line into a negative one, or to add an extra output to the main supply, the backplane wiring, etc.

This problem is solved by the ICL7660, a monolithic CMOS power supply circuit offering unique performance advantages over previously available devices. With the addition of only two noncritical capacitors (for charge pump and storage), it performs the complete supply voltage conversion from positive to negative for any input voltage between +1.5V and +10V, and provides the complementary output voltage of -1.5V to -10V. (An additional diode is needed for voltages above 6.5V.) The device operates by charging a pump capacitor to the input supply voltage and then applying the capacitor across the output supply, transferring the necessary charge to an open-circuit storage capacitor.

The ICL7660 delivers an open-circuit output equal to the negative of the input voltage to within 0.1%. Capable of producing 20mA, the device has a power-conversion efficiency of about 98% for load currents of 2mA to 5mA. The use of two or more ICL7660s extends the device's capability, as will be shown later.

Principles of Operation

Since the ICL7660 multiplies either positive or negative voltages by a factor of two, it can be considered a simple voltage doubler. This basic voltage doubling operation is shown in Figure 1, where S₁ and S₃ are the switches used to charge C₁, and S₂ and S₄ transfer the charge to C₂. It differs from most voltage doublers in that the usual blocking diodes are replaced by on-chip active MOS transistor switches.

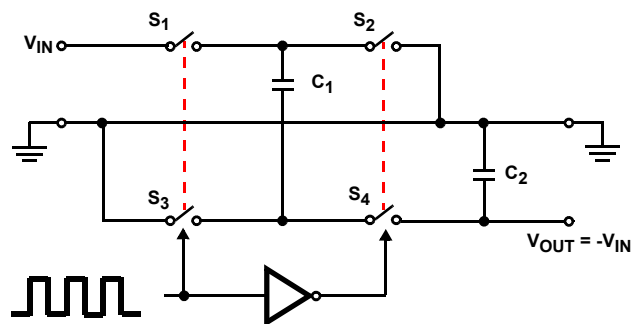


FIGURE 1. IDEALIZED VOLTAGE DOUBLER

For a negligible load, clearly the voltage inversion will be nearly perfect, with only a tiny charge being lost to stray capacitance. With a significant load, the behavior is more complex.

The amount of charge transferred from C₁ to C₂ depends upon the amount lost from C₂ to the load, and this charge must be made up by C₁ from the basic power supply. The switches themselves also have series resistance, leading to further theoretical complications, but the net result is a typical overall output impedance of around 55Ω (100Ω Max), provided that the capacitors are sufficiently large. For the natural oscillation frequency of the built-in oscillator (approximately 10kHz) values of 10μF are adequate.

The complete implementation of this function is achieved on a single CMOS chip, as shown in Figure 2.

The ICL7660 contains all the necessary conversion functions on-chip, except for the external pump and output reservoir capacitors and is made with a low-threshold CMOS technology using p- and N-Channel transistors that turn on at 0.6V. The low power dissipation, simplicity, and small chip size of CMOS make it a near-ideal technology for this application.

The ICL7660 contains an RC oscillator, a series voltage regulator, a voltage-level translator, and a logic network (Figure 2). The logic network senses the voltage on the sources and drains of the two output N-Channel transistors Q3 and Q4 and ensures that their substrates are always correctly biased.

Power Efficiency

In the case where a capacitor is charged and discharged between two voltages, V₁ and V₂, the energy lost is defined by

$$E = \frac{C(V_1^2 - V_2^2)}{2}$$

where C is value of the capacitor in farads and E is the lost energy. If $V_1 = V_2$ is very small compared with V_1 , the percentage energy loss is also small, given as:

$$\frac{100(V_1^2 - V_2^2)}{2(V_1^2)}$$

At the limit, when $V_2 = V_1$, no energy is lost. If the values of C_1 and C_2 in Figure 1 are made very large and their impedances at the switching frequency are very low compared with the load resistance, energy-conversion efficiencies approaching 100%

can be obtained. Energy is lost only by a change of voltage during the transfer of charge into and out of a capacitor.

Detailed Description

Oscillator - Divider - Regulator

The ICL7660S oscillator (Figure 3) drives a conventional divide-by-2 counter whose principal function is to supply a 50% duty cycle output (at half the input frequency) to the voltage-level translator circuit. The conventional static counter requires a two-phase clock, and supplies an output signal and its complement.

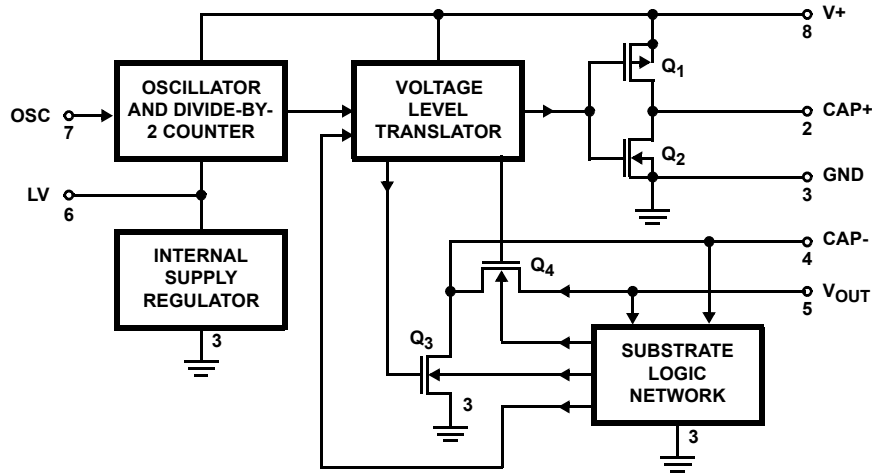


FIGURE 2. FUNCTIONAL DIAGRAM OF COMPLETE CHIP

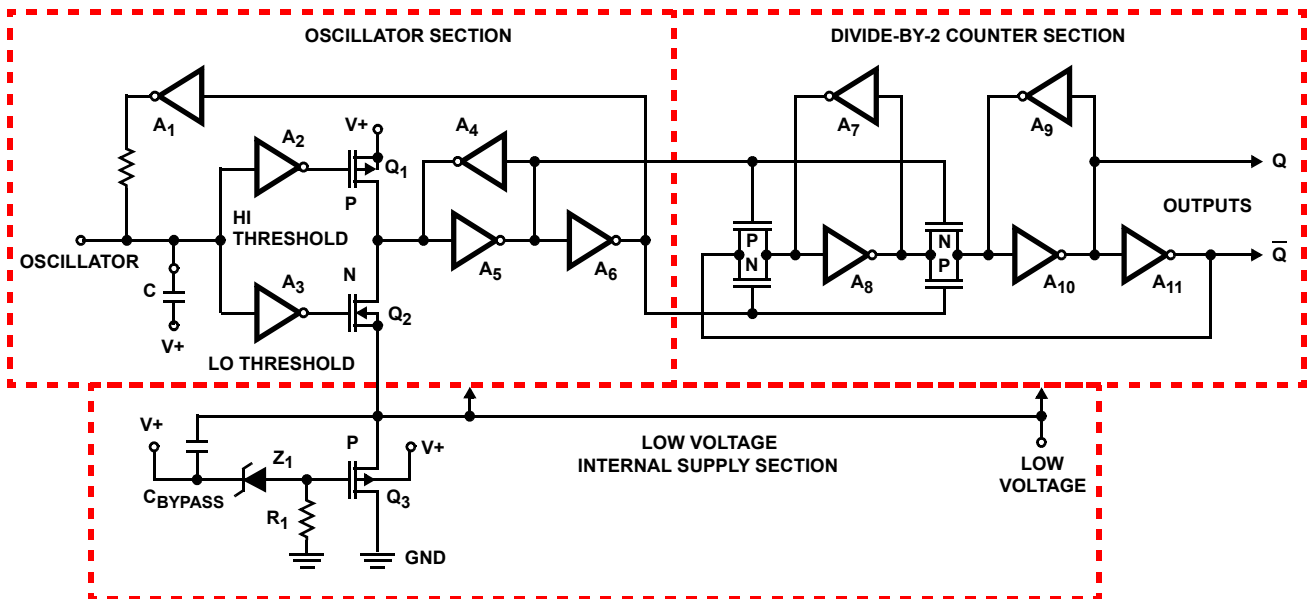


FIGURE 3. THE ICL7660S OSCILLATOR, DIVIDER AND INTERNAL REGULATOR

When the output of inverter A1 is switched high, capacitor C charges positively until inverter A2 (which has a high input-voltage trip point) switches its output low, to turn on transistor Q₁. Q₁ in turn forces the ratioed-inverter latch A4 - A5 to switch its output low. C then discharges negatively until inverter A3 (which has a low input-voltage trip point) switches its output high, turning on transistor Q₂. The output of Q₂ resets A₄ - A₅ and restarts the cycle.

Since the oscillator has a high input impedance of about 1MΩ, it may be driven from an external source such as a TTL gate or equivalent, or its frequency may be lowered by the addition of an external capacitor. At room temperature with a +5V supply and no external capacitor, the oscillator frequency will be 10kHz. The internal capacitance is about 10pF.

A series voltage regulator consisting of zener reference diode Z₁, resistor R₁, and source-follower P-Channel transistor Q₃ provides a partially regulated supply for all the low voltage circuitry on the chip. The regulator can supply up to -5V (with respect to the positive power supply) for input supply voltages

of about 6V and higher. Because of the modest size of Q₃, the voltage regulator not only reduces power consumption at high supply voltages, but also limits the maximum current taken by the oscillator and the divide-by-2 counter.

The LV terminal can be used to short out the on-chip series regulator for better operation at low supply voltages. With the Low-Voltage terminal connected to ground, operation with an input supply voltage as low as 1V is possible. At higher voltages, however, it is mandatory that this terminal be open, in order to allow the internal voltage regulator to stop device latchup and avoid internal damage.

The Level-Translator and Output Switches

The level translators (Figure 4) provide switching signals to the gates of the four output transistors, Q₁ through Q₄, with amplitudes equal to the sum of the output and supply voltages. They also ensure that a break-before-make sequence takes place as switching alternates between charge and pump configurations.

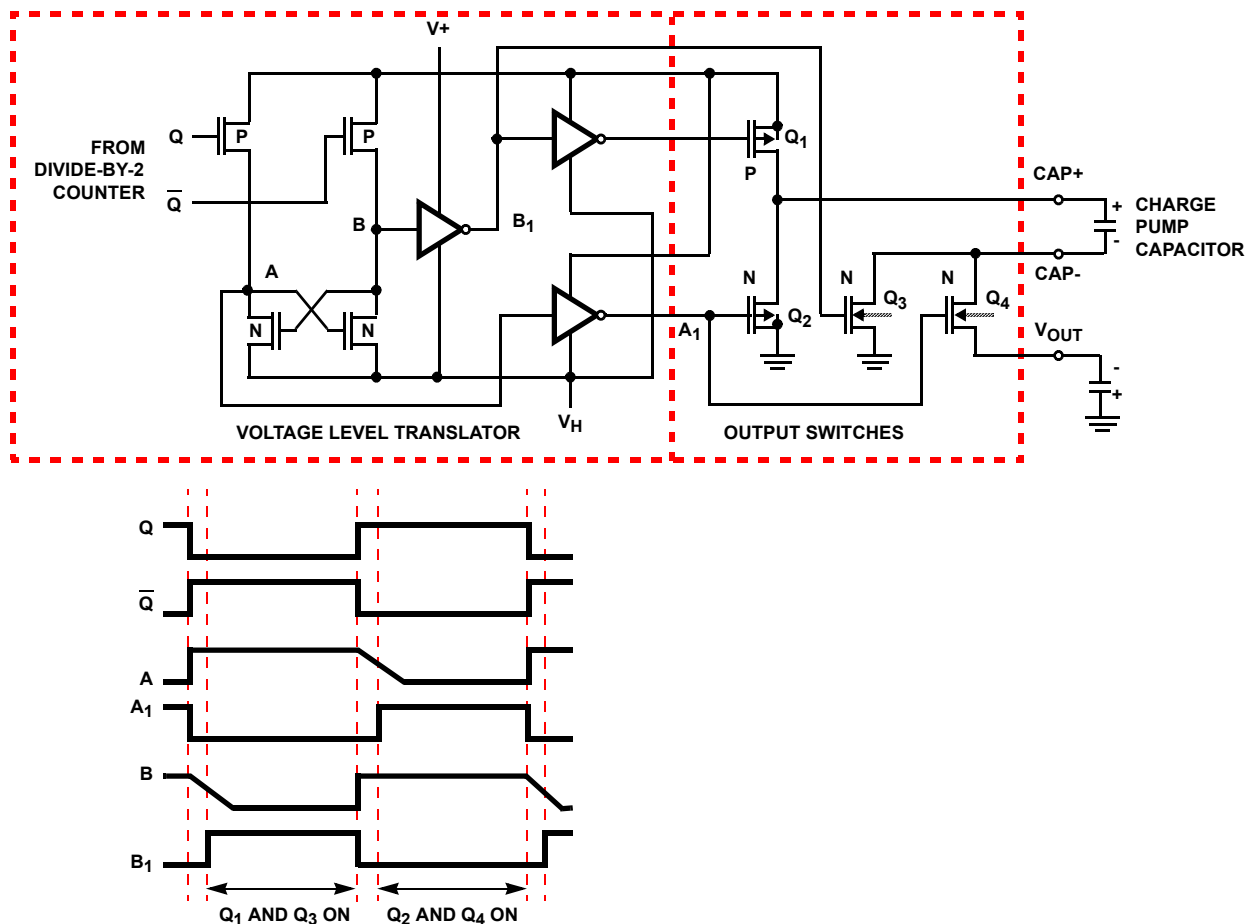


FIGURE 4. THE ICL7660S OUTPUT SWITCHES AND VOLTAGE LEVEL TRANSLATOR CIRCUIT

The Substrate Logic Network

The substrate logic network (Figure 5) is the most critical part of the converter chip. Its two main functions are to make sure that the substrates of Q_2 and Q_4 (Figure 4) are never forward-biased with respect to their sources and drains, and to establish the most negative voltage of any part of the circuit in either the charge or the pump cycles. This internal negative supply, V_{-} , is used to power the level translators. It drives the gate of either Q_3 or Q_4 to a voltage similar to that of the sources to ensure transistor turn off.

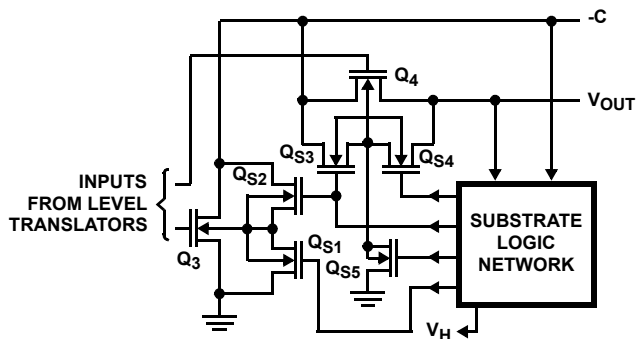


FIGURE 5. THE SUBSTRATE LOGIC NETWORK

Transistors Q_3 and Q_4 require special drive considerations, since the sources and drains are inverted on each device during pump and charge phases. Consider Q_3 's operation, for example. During the charge phase, the most positive source/drain terminal is connected to the external charge-pump capacitor. This terminal is then, by definition, the drain, whereas the source which is more negative is connected to ground. To minimize Q_3 's resistance, it is also desirable to connect its substrate to ground and not to the output voltage or to V_H , since reverse-biasing the substrate of an MOS transistor with respect to its source increases its threshold voltage, and therefore the ON resistance.

During the pumping phase, the external capacitor's negative terminal is shifted negatively by a voltage approximately equal to the supply voltage. In this case, the most negative source/drain terminal is connected to the negative side of the external capacitor (and thus becomes the source of Q_3), and its drain is connected to ground.

Similar source-drain reversals occur for Q_4 except that here conditions are different for output short-circuit operation than during normal operation. Sensing circuitry monitors the voltages on the external capacitors negative side and V_{OUT} , and compares them with ground. The substrate of Q_4 is then connected to the most negative of them. Figure 5 shows the substrate steering transistors for Q_3 and Q_4 . The steering transistors (Q_{S1-5} are relatively small N-Channel devices, and share Q_3 and Q_4 's substrates).

SCR Latch Up

A CMOS device is inherently a four-layer, or silicon-controlled-rectifier (SCR), structure. This structure can be turned on

through the forward biasing of the inherent pn junctions, and unless external current-limiting circuitry is used, latchup and resultant failure can occur.

The N-Channel transistor source acts as the cathode of the SCR, and the p+ source of the P-Channel transistor acts as the anode. Either N- or P-Channel drains can act as the SCR gate. With about 2V or more across the anode and cathode, the SCR can have either a low-impedance (ON) or high impedance (OFF) state. For the ON state to occur, three things must happen: the product of the transistors' current gains, or betas, must be at least unity, a current greater than the holding current must be present, and a trigger pulse must be applied to either gate of the SCR. Trigger signals may be caused by static discharge on the gates or by connecting either gate to the power supplies before connecting Power-supply lines to other terminals of the SCR. Even extremely high rates of voltage change across any two or more SCR pn junctions can produce latchup.

Triggering a CMOS SCR causes it to present an extremely low impedance (1Ω to 100Ω) across the power supply. Unless the power supply is current-limited, the device latches up and is often destroyed, usually by the vaporization of one of the bonding wires.

Although ICL7660 output-section switching transients are mainly capacitive, they inject currents into the substrate. At high input supply voltages, these transients can forward-bias junctions associated with the p- well or the Q_4 substrate. This in turn may trigger the inherent SCR in Q_4 and the adjacent on-chip circuitry. The result is to rapidly discharge the reservoir capacitor.

After the reservoir capacitor is almost totally discharged and the current in the SCR has fallen below the holding value, the device again operates correctly, until the output voltage (reservoir capacitance voltage) reaches the same critical value, and the latchup phenomenon starts again. Since this effect occurs only during the start of the charge cycle, and not during the pump cycle, isolating the reservoir capacitor with an external diode at the V_{OUT} terminal prevents capacitor discharge. This is recommended when using the device at higher voltage and temperatures. Otherwise the substrate logic network prevents SCR triggering, which is therefore not a problem for most operating conditions.

Basic Application

The applications of the ICL7660 are remarkably varied, especially considering the rather narrow nature of the basic device function.

The basic circuit is shown in Figure 6, and the output characteristics for 5V inversion in Figure 7. For light loads, the output voltage follows the input very precisely, while for heavier loads, the output can be viewed as having perfect inversion, plus an output resistance of about 55Ω .

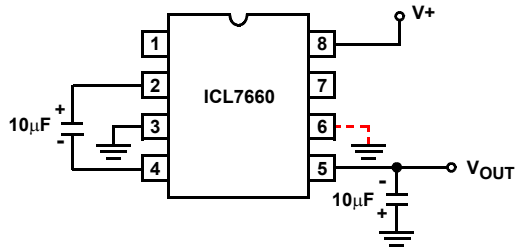


FIGURE 6. SIMPLE NEGATIVE CONVERTER

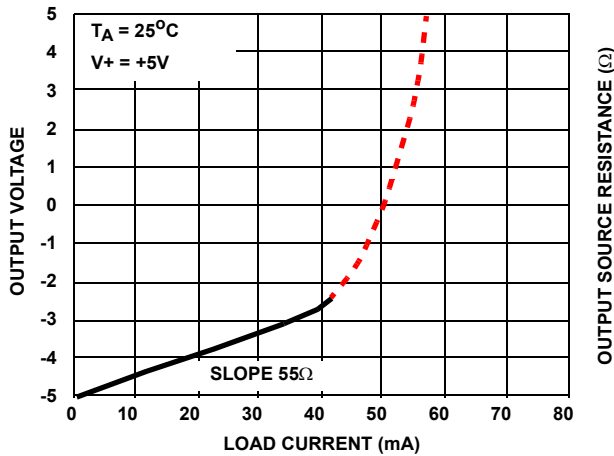


FIGURE 7. OUTPUT CHARACTERISTICS

Thus at 18mA load, the output voltage drops about 1V below the input. Beyond around 40mA, the voltage drop becomes very nonlinear, and the circuit self-limits, thereby protecting itself against excessive power dissipation. The output ripple is dependant primarily upon the output capacitor, since this must hold up the load during half the cycle time (or one oscillator period). In the steady-state case, this ripple is made up during the other half cycle time, and enough pump capacitance should be used to ensure that this is done monotonically. The recommended values ensure this for the internal oscillator frequency.

For operation at low voltages, the output impedance begins to rise rather rapidly, as a result of reduced turn-on voltage on the MOSFET switches (Figure 8). This effect can be reduced by bypassing the internal regulator, tying LV to Ground, as shown in Figure 9. This must not be done, however, if the incoming supply an exceed 8V under any circumstances, as the Internal logic oscillator and divider stages will be damaged. Note also the use of a series diode (Dx) at higher voltage and temperature, to protect the device against SCR action.

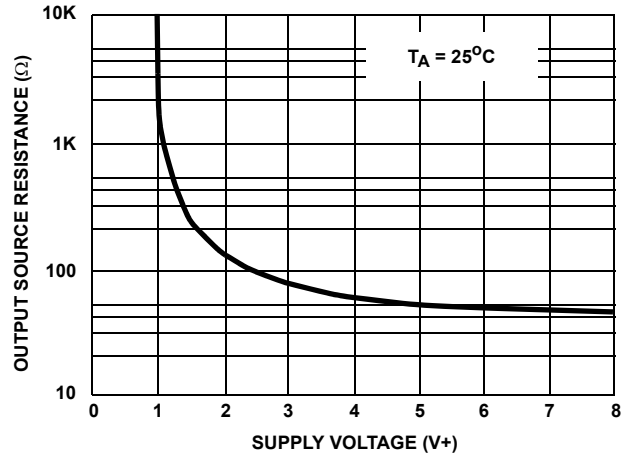


FIGURE 8. OUTPUT RESISTANCE

Figure 9 also shows an external oscillator capacitor. This can be used to reduce the oscillator frequency, giving a slight improvement in efficiency; see Figure 10.

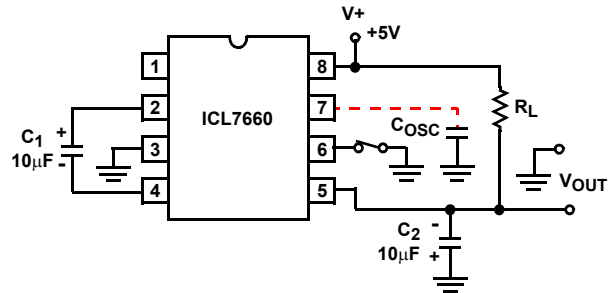


FIGURE 9. VARIATIONS OF BASIC CIRCUIT

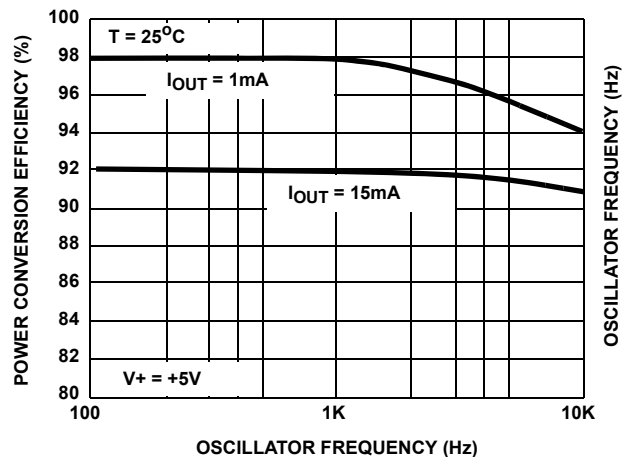


FIGURE 10. EFFICIENCY CHANGE WITH OSCILLATOR FREQUENCY

The dependence of the frequency on this external capacitance is shown in Figure 11. This can also be done to move the frequency away from a band of undue sensitivity to EMI in a system. However the output ripple will be increased, and the output impedance also unless the pump and storage capacitors are correspondingly increased.

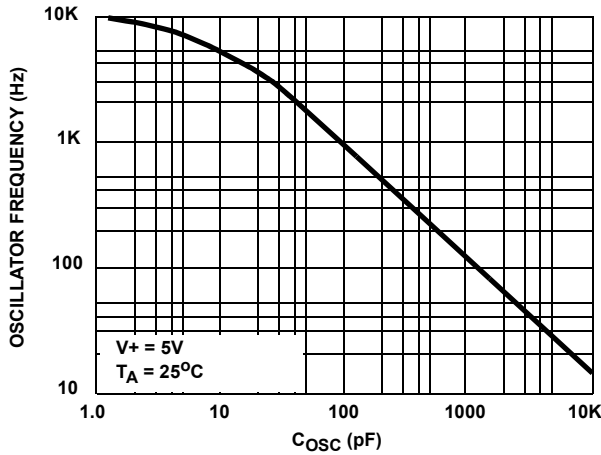


FIGURE 11. FREQUENCY VARIATION WITH OSCILLATOR CAPACITANCE

Synchronization to an external clock can be readily achieved, as shown in Figure 12. A TTL device can be used with the addition of a pull-up resistor ($10k\Omega$ to $V+$ is suitable), as can any input swinging rail-to-rail on the positive supply. The series resistor prevents problems with overdrive on the internal logic. Output transitions occur on the positive edge of the external input.

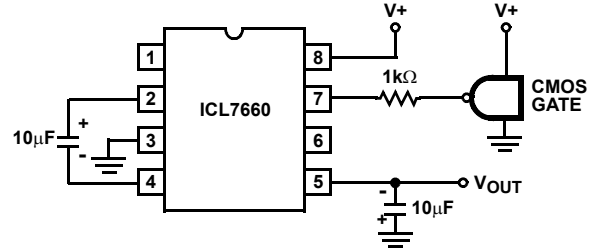


FIGURE 12. EXTERNAL CLOCKING

Wider (Parallel Connections)

For applications where the voltage drop due to load current is excessive, several ICL7660s can be paralleled. Normally this cannot be done efficiently with power supply circuits, since each one has a different idea of where the "ideal" output voltage would be and they usually end up fighting each other. However, here they see equal input voltages, and the virtually perfect inversion assures that each one does have the same idea of where the output should be so load sharing is assured. Each device must have a separate pump capacitor, since the oscillators cannot be synchronized except with an external drive, and even then the -2 will be in a random condition. The connections are shown in Figure 13. Naturally the output capacitor is common to each device. Running independently, the ripple content will include components at the difference frequency as well as the individual pumping frequencies. If this is undesirable, a single exclusive NOR gate can be used to put two ICL7660s into antiphase by comparing the outputs on pin 2, and clocking one to maintain near synchronization with the basic oscillator of the other, as shown in Figure 14.

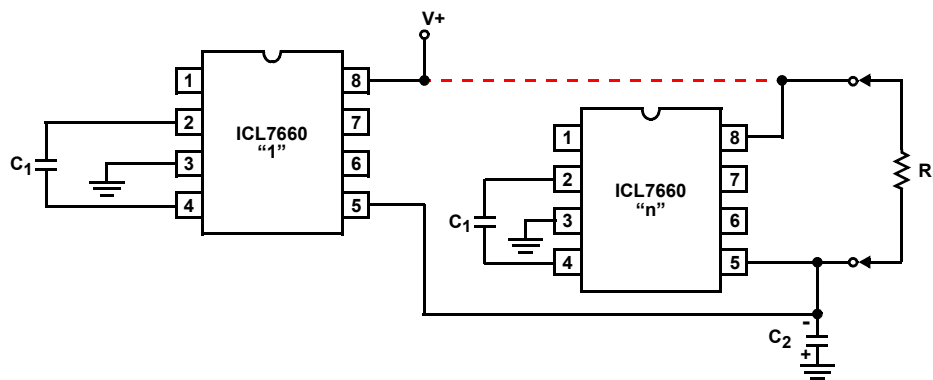


FIGURE 13. PARALLELING DEVICES

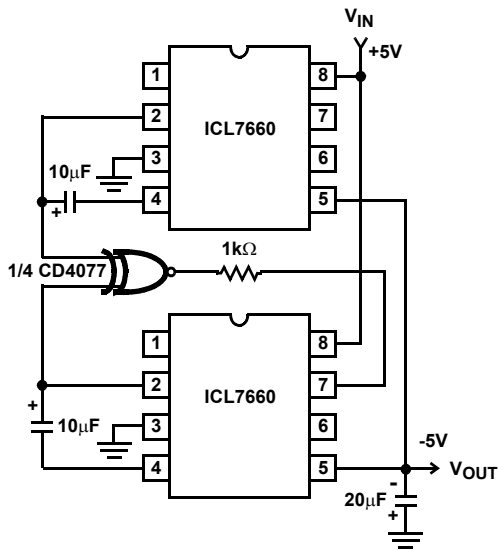


FIGURE 14. SYNCHRONIZING TWO ICL7660S

The concept can be extended to drive four devices in four separate phases, using a single extra logic-gate package, as shown in Figure 15. The duty cycle of the oscillator is reasonably close to 50%, so driving two pairs, each in the configuration of Figure 14, from opposite phases of the oscillator gives four separately-timed pumps per cycle. This circuit will give about 75mA output before the voltage drops by 1V, or an output impedance of under 14Ω. The four phase operation minimizes the ripple, while ensuring very even load sharing. For even more parallel synchronous device, a Johnson counter using Q and Q outputs should be considered.

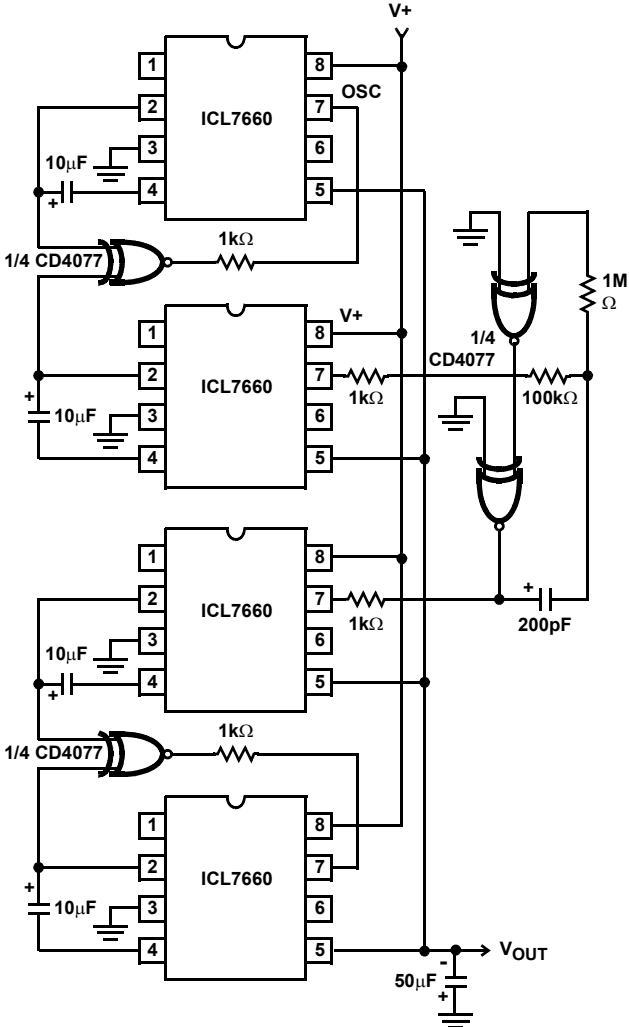


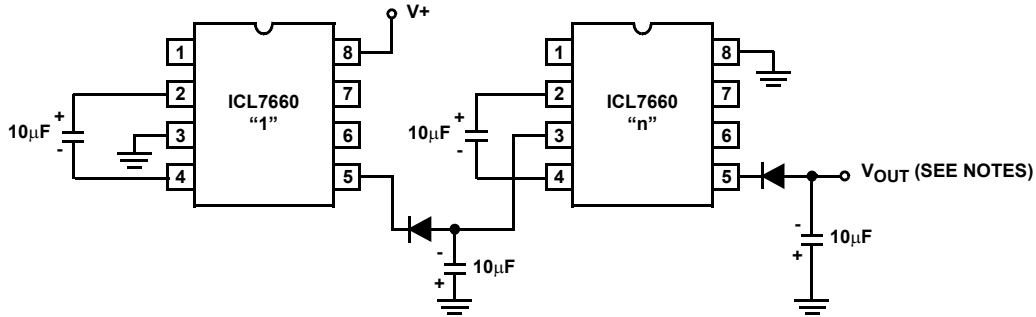
FIGURE 15. SYNCHRONIZING A QUAD

Deeper (Series Connection)

It is also possible to connect ICL7660s in series, cascading them to generate higher negative voltages. The basic connections are shown in Figure 16.

This technique can be extended to several multiplication levels. However, the basic limitations of this technique must be recognized. In line with the Laws of Thermodynamics, the input current required for each stage is twice the load current on that stage, plus the quiescent current required to operate that stage.

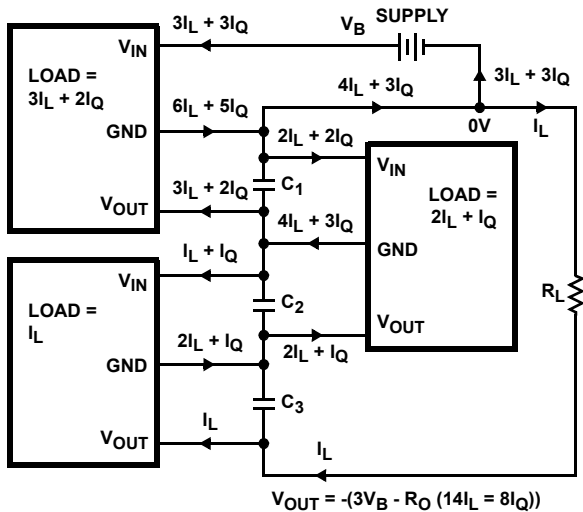
Thus the load current is rapidly multiplied down the chain, as shown in Figure 17. Note also that the quiescent current increases the load current on each stage, though not as fast as the ultimate load itself.



NOTES:

1. $V_{OUT} = -n+$ for $1.5V \leq V+ \leq 6.5V$
2. $V_{OUT} = -n (V+ - V_{FOX})$ for $6.5V \leq V+ \leq 10.0V$.

FIGURE 16. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE



$V_{C1} = V_B - R_O (3I_L = 2I_Q)$
 $V_{C2} = V_B - R_O (5I_L = 3I_Q)$
 $V_{C3} = V_B - R_O (6I_L = 3I_Q)$

FIGURE 17. CURRENT FLOW FOR CASCADED DEVICES

Furthermore, the loss in voltage in early stages due to series resistance is multiplied through all subsequent stages. Thus the effective output impedance mounts rapidly with the number of stages. (See Table 1.) This effect can be reduced by paralleling devices in the lowest stages (see above.) If the weighting corresponds to the square of the position, the effective resistance to load current goes up only linearly with the number of stages, but the cost quickly becomes prohibitive. Nevertheless, for light loads and moderate multiplication, useful performance can be achieved.

TABLE 1.

# STAGES	RESISTANCE	MULTIPLIERS
n	$R_O(L)$	$R_O(Q)$
1	1	0
2	5	2
3	14	8
4	30	20
5	55	40

A variation of this circuit, another form of series circuit, is shown in Figure 18. This circuit can be used effectively to generate -15V from +5V in light load applications using only two devices. The output impedance corresponds roughly to $n = 2$ in Table 1, much better than if the previous circuit were used with $n = 3$. In general, geometric increases, as in Figure 18, are better until the voltage limit is reached, at which time arithmetic cascading as in Figure 16 must be utilized.

Upside Down (Positive Multiplication)

The ICL7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 19. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of $V+ - V_F$ (where $V+$ is the supply voltage and V_F is the forward voltage drop of diode D_1) On the transfer cycle, the voltage on C_1 plus the supply voltage ($V+$) is applied through diode D_2 to capacitor C_2 . The voltage thus created on C_2 becomes $(2V+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2 .

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V+ = 5V$ and an output current of 10mA it will be approximately 60Ω.

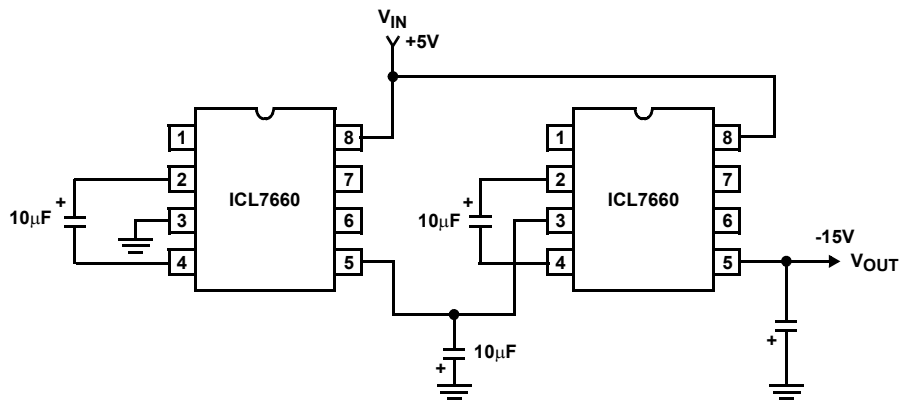


FIGURE 18. GETTING -15V FROM +5V

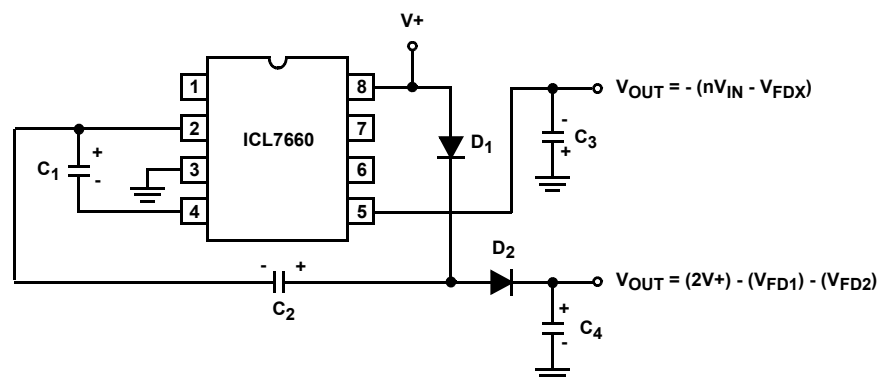


FIGURE 19. COMBINED NEGATIVE CONVERTER AND POSITIVE MULTIPLIER

Divide and Conquer

The ICL7660 can be used to split a supply in half, as shown in Figure 20.

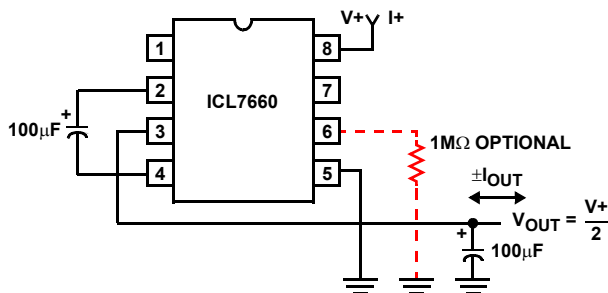


FIGURE 20. EFFICIENT SUPPLY SPLITTING

Here the “basic” output connection and the “basic” negative supply input are exchanged and the output voltage thus becomes the midpoint. Start-up can be a problem, and although careful capacitance and load balancing may frequently be adequate, a simple resistor to LV will always work. The circuit is useful for series-fed line systems, where a heavy local load at low voltage can be converted to a lighter current, at high voltage. Other useful applications are in driving low voltage (e.g., +7.5V) circuits from $\pm 15V$ supplies, or low

voltage logic from 9V or 12V batteries. The output impedance is extremely low; all parts of the circuit cooperate in sharing the current, and so act in parallel.

For other division ratios, the series configurations of Figure 16 can be driven backwards, to generate V_{IN}/n , or even $m/n(V_{IN})$, for small values of m and n . Again, care must be taken to ensure start up for each device.

One interesting combination of several preceding circuits is shown in Figure 21, where a +15V supply is converted, via +7.5V and -7.5V, to -1.5V using three ICL7660s. The output impedance of this circuit is about 250 Ω .

For cases where the output impedance of an ICL7660 circuit is too high, obviously some form of output regulation can be used. However in most cases adequate regulation can be achieved at high efficiency by pre-regulating the input. A suitable circuit is shown in Figure 22, using the ICL7611 low power CMOS op amp. Because of the large source-current capability of this op amp, even on its lowest bias current setting, very efficient operation is possible. An ICL8069 bandgap device is used as the reference generator for the regulator. The output impedance can be reduced to 4 Ω , while maintaining a current capability of well over 10mA. In designing circuits of this type, it is important to remember that there is a switching delay averaging one oscillator cycle between the

output of the op amp and the actual output voltage. This can have substantial repercussions on the transient response if the time-constants in the circuit are not adequate. If multiple voltage converters are used, synchronization schemes such as those of Figures 14 and 15 are probably advisable.

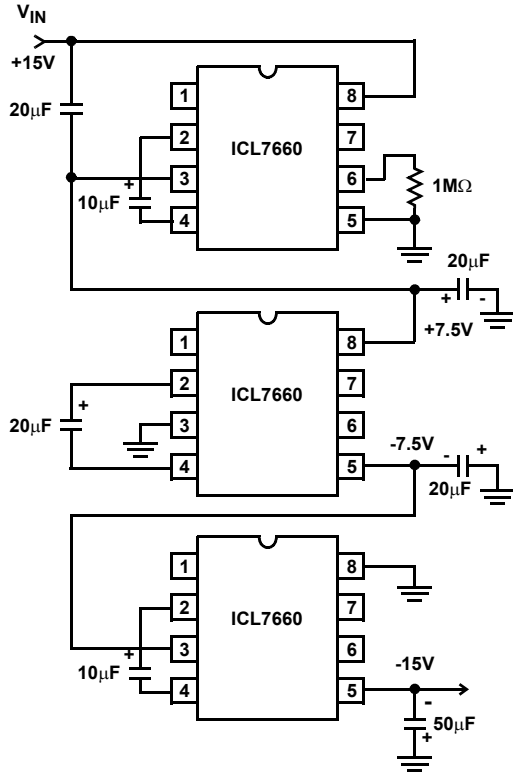


FIGURE 21. +15V TO -15V IN THREE EASY STAGES

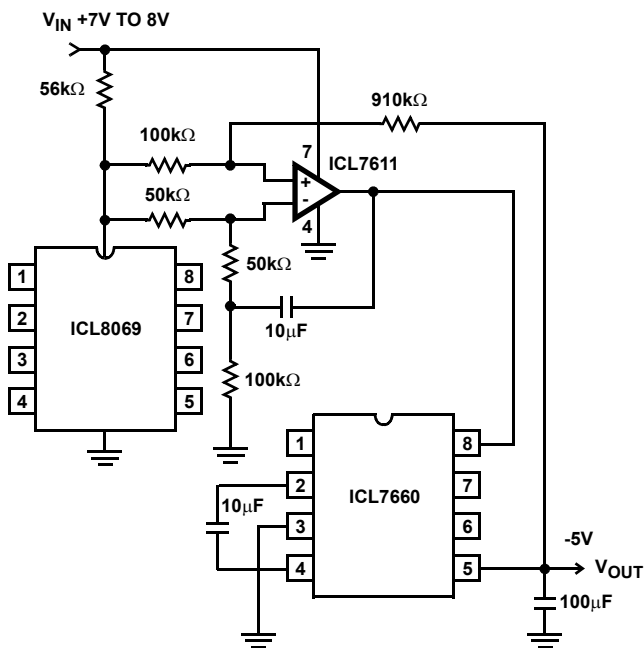


FIGURE 22. REGULATED OUTPUT INVERTER

Messing About

The applications shown so far have corresponded to the use of the ICL7660 as a sort of equivalent of single turns on a power transformer, with paralleled turns to get more current, series turns for more voltage, etc. However, there are some other possibilities. By looking again at the block diagram (Figure 2), it is evident that the device could be used as a 50% duty cycle high power clock driver, using either the internal oscillator or an external signal, as in Figure 23. An antiphase clock can also be derived from the circuit, as shown, but the pull-up on this output, being an N-Channel switch only, does not have as good a voltage swing. It is adequate for TIC level operation, but for CMOS clocking may require an external pull-up resistor or transistor.

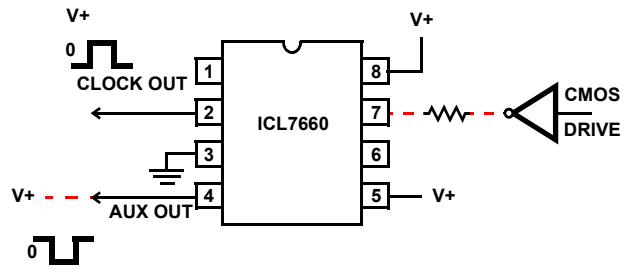


FIGURE 23. HIGH POWER CLOCK DRIVE

Another interesting class of applications comes from the capability to synchronously detect the output of an AC driven transducer, as shown in Figure 24. (This could be viewed as a signal transformer application.) Although the circuit shown utilizes a linear transformer type of transducer, any similar device may be used. The output voltage, which is correctly phased and of either polarity, may be fed into an A/D converter for display or microprocessor interface as desired.

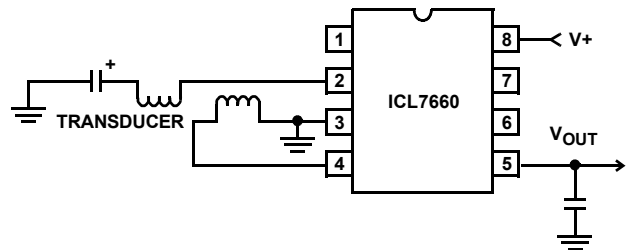


FIGURE 24. TRANSDUCER DRIVER AND DETECTOR

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