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April 1st, 2010
Renesas Electronics Corporation

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Introduction
The software FADD adds single-precision floating-point numbers placed in general-purpose registers and places the result of addition in general-purpose registers.

Target Device
H8/38024

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1. Arguments

<table>
<thead>
<tr>
<th>Description</th>
<th>Memory area</th>
<th>Data length (bytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>Augend</td>
<td>R0, R1</td>
</tr>
<tr>
<td></td>
<td>Addend</td>
<td>R2, R3</td>
</tr>
<tr>
<td>Output</td>
<td>Result of addition</td>
<td>R0, R1</td>
</tr>
</tbody>
</table>

2. Changes to Internal Registers and Flags

<table>
<thead>
<tr>
<th>R0</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
<th>R5</th>
<th>R6</th>
<th>R7</th>
</tr>
</thead>
<tbody>
<tr>
<td>○</td>
<td>○</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>—</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I</th>
<th>U</th>
<th>H</th>
<th>U</th>
<th>N</th>
<th>Z</th>
<th>V</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>×</td>
<td>—</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
</tbody>
</table>

Legend
—: No change
×: Undefined
○: Result

3. Specifications

<table>
<thead>
<tr>
<th>Program memory (bytes)</th>
<th>280</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data memory (bytes)</td>
<td>0</td>
</tr>
<tr>
<td>Stack (bytes)</td>
<td>0</td>
</tr>
<tr>
<td>Clock cycle count</td>
<td>268</td>
</tr>
<tr>
<td>Reentrant</td>
<td>Possible</td>
</tr>
<tr>
<td>Relocation</td>
<td>Possible</td>
</tr>
<tr>
<td>Interrupt</td>
<td>Possible</td>
</tr>
<tr>
<td></td>
<td>Possible</td>
</tr>
</tbody>
</table>
4. **Notes**

The clock cycle count (268) in the specifications is for the example shown in figure 1. For the format of floating-point numbers, see "About Single-precision floating-point Numbers <Reference>.”

5. **Description**

5.1 **Details of functions**

1. The following arguments are used with the software FADD:
   a. Input arguments:
      - R0: Sets the upper 2 bytes of a single-precision floating-point as augend.
      - R1: Sets the lower 2 bytes of a single-precision floating-point as augend.
      - R2: Sets the upper 2 bytes of a single-precision floating-point as addend.
      - R3: Sets the lower 2 bytes of a single-precision floating-point as addend.

   b. Output arguments:
      - R0: The upper 2 bytes of a single-precision floating-point are placed here as the result of addition.
      - R1: The lower 2 bytes of a single-precision floating-point are placed here as the result of addition.

2. The following figure illustrates the execution of the software FADD. When the input arguments are set as shown in (1), the result of addition is placed in R0 and R1 as shown in (2).

![Figure 1 Example of Software FADD Execution](image-url)
5.2 Notes on usage

1. The maximum and minimum values that can be handled by the software FADD are as follows:
   - Positive maximum: H'7F800000
   - Positive minimum: H'00000001
   - Negative maximum: H'80000001
   - Negative minimum: H'FF800000

2. All positive single-precision floating-point numbers H'7F800001 to H'7FFFFFFF are treated as a maximum value (H'7F800000). All negative single-precision floating-point numbers H'FF800000 to H'FFFFFFFF are treated as a minimum value (H'FF800000).

3. As a maximum value is treated as infinity (∞), the result of ∞ + 100 or ∞ - 100 becomes infinite. (See table 1.)

Table 1 Examples of Operation with Maximum Values Used as Arguments

<table>
<thead>
<tr>
<th>Augend</th>
<th>Addend</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>H'7F800000 to H'7FFFFFFF</td>
<td>*********</td>
<td>H'7F800000</td>
</tr>
<tr>
<td>Not H'7F800000 to H'FFFFFFFF</td>
<td>H'7F800000 to H'7FFFFFFF</td>
<td>H'7F800000</td>
</tr>
<tr>
<td>H'FF800000 to H'FFFFFFFF</td>
<td>*********</td>
<td>H'FF800000</td>
</tr>
<tr>
<td>Not H'7F800000 to H'7FFFFFFF</td>
<td>H'FF800000 to H'FFFFFFFF</td>
<td>H'FF800000</td>
</tr>
</tbody>
</table>

Note: * represents a hexadecimal number.

4. H'80000000 is treated as H'00000000 (zero).

5. After execution of the software FADD, the augend and addend data will be lost. When the input arguments are still needed after software FADD execution, save them in memory.

5.3 Description of data memory

The software FADD uses no data memory.
5.4 Example of usage

Set an augend and an addend in the general-purpose registers and call the software FADD as a subroutine.

| WORK1 | . RES. W 2 | Reserve a data memory area in which the user program places an augend. |
| WORK2 | . RES. W 2 | an addend. |
| WORK3 | . RES. W 2 | the result of addition. |

MOV. W @WORK1, R0  
MOV. W @WORK1+2, R1  
MOV. W @WORK2, R2  
MOV. W @WORK2+2, R3  

Place the augend set by the user program in R0 and R1.

Place the addend set by the user program in R2 and R3.

JSR @FADD  

Call the software FADD as a subroutine.

MOV. W R0, @WORK3  
MOV. W R1 @WORK3+2  

Save the result of addition set in the output argument in R0 and R1.

5.5 Operation

Addition of single-precision floating-point numbers is done in the following steps:

1. The software checks whether the augend and addend are +∞ or -∞.
   a. When the exponent of the augend is H'FF, either of the following values is output depending on the state of the sign bit:

<table>
<thead>
<tr>
<th>Sign bit</th>
<th>Output value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (positive)</td>
<td>H'7F800000 (+∞)</td>
</tr>
<tr>
<td>1 (negative)</td>
<td>H'FF800000 (−∞)</td>
</tr>
</tbody>
</table>

   b. The table above also applies when the augend is neither +∞ nor -∞ and the exponent of the addend is H'FF.

2. The software checks whether the augend and addend are "0".
   a. If either the augend or addend is "0", the other number is output (if both are "0", "H'00000000" is output).

3. The software attempts to match the exponent of the augend with that of the addend.
   a. The smaller number of the exponent is incremented and, at the same time, the mantissa (including the implicit MSB) is shifted digit by digit to right until the exponent of the augend matches that of the addend. (In the case of the denormalized format, 1 is added to the exponent and the MSB of the mantissa is taken as implicitly being zero.

4. The mantissas are added.
5. The result of addition is corrected to produce a number in the floating-point data format.

(Example)

Augend = 1.2088876915 \times 2^{114}
\quad (H'789ABCDE)
\quad Sign bit = 0, exponent = H'F1, mantissa = H'1ABCDE
\quad (implicit MSB is not included)

Addend = 1.21282410622 \times 2^{-117}
\quad (H'7A1B3DD2)
\quad Sign bit = 0, exponent = H'F4, mantissa = H'1B3DD2
\quad (implicit MSB is not included)

\[ 1111 \ 0001 \ 1 . 00 \ 1010 \ 1011 \ 1100 \ 1101 \ 1110 \]
\[ H'789ABCDE \]
\[ 1111 \ 0100 \ 1 . 0011 \ 0101 \ 0111 \ 1101 \ 1101 \ 0010 \]
\[ H'7A1B3DD2 \]
\[ \rightarrow \text{Matches exponent parts (3 is added to the augend)} \]
\[ \rightarrow \text{Shift the mantissa of the augend 3 bits to right} \]

Augend 1111 0100 0 . 0011 0101 0111 1101 1101
\[ \times \]
Addend 1111 0100 1 . 0111 0011 0011 1101 1101 0010
\[ \rightarrow \text{The exponent part remains unchanged.} \]
\[ \rightarrow \text{Only the mantissa part undergoes addition.} \]

Result of addition = 1.36393511295 \times 2^{-117}
\quad (H'7A2E956D)
\quad Sign bit = 0, exponent part = H'F4, mantissa part = H'2E956D
\quad (excluding the implicit MSB)
6. Flowchart

```
FADD

#H'00 → R6L
#H'7F80 → R5

Bit 7 of R0H → Bit 0 of R6L

0 → Bit 7 of R0H

Bit 7 of R2H → Bit 1 of R6L

0 → Bit 7 of R2H

R0 ≥ R5

Yes

R2 < R5

Yes

Shift R6L 1 bit to right

No

No

C = 0

Yes

#H'7F80 → R0

#H'0000 → R1

RTS

No

#H'FF80 → R0

#H'0000 → R1

RTS

----- Clear R6L to 0. Place #H'7F80 in R5.

----- Place the sign bit of the augend in bit 0 of R6L.

----- Clear the sign bit of the augend.

----- Place the sign bit of the addend in bit 1 of R6L.

----- Clear the sign bit of the addend.

----- Branch when the exponent part of the augend is "H'FF".

----- Branch when the exponent part of the augend is not "H'FF".

----- Shift the sign bit of the addend to bit 0 of R6L.

----- Place "H'7F800000" as output when the sign bit is "0" (positive), or "H'FF800000" as output when the sign bit is "1" (negative).
```
Addition of Single-Precision Floating-Point Numbers (FADD)

Place "1" in bit 7 of R6L when the augend is "0".

Place "1" in bit 6 of R6L when the addend is "0".

Place "1" in bit 6 of R6L when the addend is "0".

Place the augend or addend as an output value in R0 and R1.
Addition of Single-Precision Floating-Point Numbers (FADD)

- Place the exponent part of the augend in R0H.
- Places the exponent part of the addend.
- Clear bit 7 of R0L.
- Place "1" in bit 7 of R0L when the augend is represented in normalized format (R0H ≠ 0), and add #1 to R0H when the augend is represented in denormalized format (R0H = 0).
- Clear bit 7 of R2L.
- Place "1" in bit 7 of R2L when the addend is represented in normalized format (R2H ≠ 0), and adds #1 to R2H when the addend is represented in denormalized format (R2H = 0).
Addition of Single-Precision Floating-Point Numbers (FADD)

Place the exponent (R0H) of the augend in R5H and the exponent (R2H) of the addend in R5L.

Compare R5H with R5L: branch to (4) when R5H = R5L or to (5) when R5H < R5L.

Find the difference (R5H) when R5H > R5L.

Clear the addend to 0 and branch to (4) when R5H > #D’24.

Shift the mantissa of the addend to right as many times as R5H (the difference between exponents).
Addition of Single-Precision Floating-Point Numbers (FADD)

---

5

LBL14

\[ R5L \rightarrow R5H \rightarrow R5L \]

---

\[ R5L < \#D'24 \]

Yes

---

\[ R2H \rightarrow R0H \]

---

\[ \#H'0000 \rightarrow R1 \]

\[ R1L \rightarrow R0L \]

---

Yes

---

\[ \text{Shift R0L 1 bit to right} \]

\[ \text{Rotate R1H and R1L 1 bit to right} \]

---

\[ R5L - \#1 \rightarrow R5L \]

---

\[ \text{Check the sign bits and branch when they have opposite signs.} \]

---

8

LBL17

\[ C = 1 \]

Yes

---

No

---

4

LBL16

\[ \text{Shift the mantissa of the augend to right as many as R5L} \]

\[ \text{(the difference between exponents).} \]

---

\[ \text{Transfer R2H to R0H.} \]

---

7

No

---

\[ \text{Transfer R2H to R0H, clear the mantissa of the augend, and branch when R5L > \#D'24.} \]

---

\[ \text{Check the sign bits and branch when they have opposite signs.} \]
Addition of Single-Precision Floating-Point Numbers (FADD)

7

R1 + R3 \rightarrow R1
R0L + R2L + C \rightarrow R0L

------ Add the mantissas.

9

R0H + #1 \rightarrow R0H

------ Rotate the mantissa 1 bit to right and add #1 to the exponent when a carry occurs.

10

Branch to (10) when R0H \neq \#H'FF or to (11) when R0H = \#H'FF.

11

R0H = \#H'FF

------ No

C = 0

Yes

Yes

No

No

Yes

Yes

LBL23

LBL19

LBL1
R1 - R3 → R1
R0L - R2L - C → R0L

Subtract the mantissa.

Yes

R0L ≠ 0

No

#H'00 → R0H

Yes

Place H'00 in R0H to end when the result of subtraction is "0".

No

LBL18

C = 0

Yes

Reverse the signed bits and take two's complement of mantissa when a borrow occurs.

No

Bit 0 of R6L

LBL19

R0L → R0L
R1H → R1H
R1L → R1L

LBL17

R1L + #1 → R1L
R1H + #H'00 + C → R1L
R0L + #H'00 + C → R0L

RTS

R0L → R0L
R1H → R1H
R1L → R1L
Shift R1L 1 bit to left
Rotate R1H and R0L 1 bit to left

R0H - #1 → R0H

R0H = 0

C = 0

C → Bit 7 of R0L

Bit 0 of R6L → C
C → Bit 7 of R0H

RTS
7. Program List

*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 10:20:43

PROGRAM NAME =

;***********************************************************************
;*  00 - NAME  :FLOATING POINT ADDITION (FADD)
;***********************************************************************

;***********************************************************************
;*  ENTRY  :R0 (UPPER WORD OF SUMMAND)
;*   R1 (LOWER WORD OF SUMMAND)
;*   R2 (UPPER WORD OF ADDEND)
;*   R3 (LOWER WORD OF ADDEND)
;***********************************************************************

;***********************************************************************
;*  RETURNS  :R0 (UPPER WORD OF RESULT)
;*   R1 (LOWER WORD OF RESULT)
;***********************************************************************

;***********************************************************************

17 FADD_cod C 0000
18 .SECTION FADD_code,CODE,ALIGN=2
19 .EXPORT FADD

20 FADD_cod C 00000000 FADD .EQU $ ;Entry point
21 FADD_cod C 0000 FE00 MOV.B #H'00,R6L ;Clear R6L
22 FADD_cod C 0002 79057F80 MOV.W #H'7F80,R5 ;Set "H'7F80"

23 FADD_cod C 0006 7770 BLD #7,R0H
24 FADD_cod C 0008 670E BST #0,R6L ;Set sign bit to bit 0 of R6L
25 FADD_cod C 000A 7272 BCLR #7,R0H ;Bit clear bit 7 of R0H
26 FADD_cod C 0012 1D05 CMP.W R0,R5
27 FADD_cod C 0014 4306 BLS LBL1 ;Branch if "exponent of summand"="H'FF"
28 FADD_cod C 0016 1D25 CMP.W R2,R5
29 FADD_cod C 0018 421A BHI LBL4 ;Branch if not "exponent of summand"="H'FF"
30 FADD_cod C 0020 7272 BCLR #7,R2H ;Bit clear bit 7 of R2H
31 FADD_cod C 0022 110E SHLR R6L 1 bit right
32 FADD_cod C 0024 450A BCS LBL3 ;Branch if sign bit=1
33 FADD_cod C 0026 79007F80 MOV.W #H'7F80,R0 ;Set plus maximum number
34 FADD_cod C 0028 79010000 MOV.W #H'0000,R1
35 FADD_cod C 0030 5470 RTS
36 FADD_cod C 0032 5470 RTS

;
Addition of Single-Precision Floating-Point Numbers (FADD)

49 FADD_cod C 0034  LBL4
50 FADD_cod C 0034  0D11  MOV.W  R1,R1  ;
51 FADD_cod C 0036  4608  BNE  LBL5  ;Branch if Z=0
52 FADD_cod C 0038  0D00  MOV.W  R0,R0
53 FADD_cod C 003A  4604  BNE  LBL5  ;Branch if Z=0
54 FADD_cod C 003C  707E  BSET  #7,R6L  ;Bit set bit 7 of R6L
55 FADD_cod C 003E  720E  BCLR  #0,R6L  ;Bit clear bit 0 of R6L
56 FADD_cod C 0040  LBL5
57 FADD_cod C 0040  0D33  MOV.W  R3,R3
58 FADD_cod C 0042  4608  BNE  LBL6  ;Branch if Z=0
59 FADD_cod C 0044  0D22  MOV.W  R2,R2
60 FADD_cod C 0046  4604  BNE  LBL6  ;Branch if Z=0
61 FADD_cod C 0048  706E  BSET  #6,R6L  ;Bit set bit 6 of R6L
62 FADD_cod C 004A  721E  BCLR  #1,R6L  ;Bit clear bit 1 of R6L
63 FADD_cod C 004C  LBL6
64 FADD_cod C 004C  777E  BLD  #7,R6L
65 FADD_cod C 004E  746E  BOR  #6,R6L
66 FADD_cod C 0050  440C  BCC  LBL8  ;Branch if not summand+addend=0
67 FADD_cod C 0052  0931  ADD.W  R3,R1  ;Set summand and addend to result
68 FADD_cod C 0054  0920  ADD.W  R2,R0
69 FADD_cod C 0056  770E  BLD  #0,R6L
70 FADD_cod C 0058  741E  BOR  #1,R6L
71 FADD_cod C 005A  6770  BST  #7,R0H  ;Set sign bit
72 FADD_cod C 005C  5470  RTS
73
74 FADD_cod C 005E  LBL8
75 FADD_cod C 005E  7778  BLD  #7,R0L
76 FADD_cod C 0060  1200  ROTXL  R0H  ;Set exponent of summand to R0H
77
78 FADD_cod C 0062  777A  BLD  #7,R2L
79 FADD_cod C 0064  1202  ROTXL  R2H  ;Set exponent of addend to R0L
80
81 FADD_cod C 0066  7278  BCLR  #7,R0L
82 FADD_cod C 0068  0C00  MOV.B  R0H,R0H
83 FADD_cod C 006A  4704  BEQ  LBL9  ;Branch if summand is normalized
84 FADD_cod C 006C  7078  BSET  #7,R0L  ;Set implicit MSB to summand
85 FADD_cod C 006E  4002  BRA  LBL10  ;Branch always
86 FADD_cod C 0070  LBL9
87 FADD_cod C 0070  8001  ADD.B  #H'01,R0H
88 FADD_cod C 0072  LBL10
89 FADD_cod C 0072  727A  BCLR  #7,R2L
90 FADD_cod C 0074  0C22  MOV.B  R2H,R2H
91 FADD_cod C 0076  4704  BEQ  LBL11  ;Branch if addend is normalized
92 FADD_cod C 0078  707A  BSET  #7,R2L  ;Set implicit MSB to addend
93 FADD_cod C 007A  4002  BRA  LBL12  ;Branch always
94 FADD_cod C 007C  LBL11
95 FADD_cod C 007C  8201  ADD.B  #H'01,R2H
96
97 FADD_cod C 007E  LBL12
98 FADD_cod C 007E  0C05  MOV.B  R0H,R5H
99 FADD_cod C 0080  0C2D  MOV.B  R2H,R5L
100 FADD_cod C 0082  1CD5  CMP.B  R5L,R5H
101 FADD_cod C 0084  4738  BEQ  LBL16  ;Branch if R5H=R5L
102 FADD_cod C 0086  451A  BCS  LBL14  ;Branch if R5H<R5L
H8/300L Series
Addition of Single-Precision Floating-Point Numbers (FADD)

103
104 FADD_cod C 0088 18D5 SUB.B R5L,R5H
105 FADD_cod C 008A A518 CMP.B #D'24,R5H ;Set bit counter
106 FADD_cod C 008C 4508 BCS LBL13 ;Branch if R5H<D'24
107 FADD_cod C 008E 79020000 MOV.W #H'0000,R2 ;Clear addend
108 FADD_cod C 0092 0D23 MOV.W R2,R3
109 FADD_cod C 0094 4028 BRA LBL16 ;Branch always
110 FADD_cod C 0096 LBL13
111 FADD_cod C 0096 110A SHLR R2L ;Shift mantissa of addend 1 bit left
112 FADD_cod C 0098 1303 ROTXR R3H
113 FADD_cod C 009A 1305 ROTXR R3L
114 FADD_cod C 009C 1A05 DEC.B R5H ;Decrement bit counter
115 FADD_cod C 009E 46F6 BNE LBL15 ;Branch Z=0
116 FADD_cod C 00A0 401C BRA LBL16 ;Branch always
117
118 FADD_cod C 00A2 LBL14
119 FADD_cod C 00A2 185D SUB.B R5H,R5L
120 FADD_cod C 00A4 AD18 CMP.B #D'24,R5L ;Branch if R5L<D'24
121 FADD_cod C 00A6 4508 BCS LBL15 ;Branch if R5L<D'24
122 FADD_cod C 00A8 0C20 MOV.B R2H,R0H
123 FADD_cod C 00AA 79010000 MOV.W #H'0000,R1 ;Clear summand
124 FADD_cod C 00AE 0C98 MOV.B R1L,R0L
125 FADD_cod C 00B0 400C BRA LBL16 ;Branch always
126 FADD_cod C 00B2 LBL15
127 FADD_cod C 00B2 1108 SHLR R0L ;Shift mantissa of summand 1 bit right
128 FADD_cod C 00B4 1301 ROTXR R1H
129 FADD_cod C 00B6 1309 ROTXR R1L
130 FADD_cod C 00B8 1A05 DEC.B R5L ;Decrement bit counter
131 FADD_cod C 00BA 46F6 BNE LBL15 ;Branch if Z=0
132 FADD_cod C 00BC 0C20 MOV.B R2H,R0H
133
134 FADD_cod C 00BE LBL16
135 FADD_cod C 00BE 770E BLD #0,R6L
136 FADD_cod C 00C0 751E BXOR #1,R6L
137 FADD_cod C 00C2 4516 BCS LBL17 ;Branch if different sign bit
138
139 FADD_cod C 00C4 0931 ADD.W R3,R1 ;Addition mantissa
140 FADD_cod C 00C6 0EA8 ADDX.B R2L,R0L
141 FADD_cod C 00C8 442A BCC LBL19 ;Branch if C = 0
142 FADD_cod C 00CA 1308 ROTXR R0L ;Rotate mantissa 1 bit right
143 FADD_cod C 00CC 1301 ROTXR R1H
144 FADD_cod C 00CE 1309 ROTXR R1L
145 FADD_cod C 00D0 8001 ADD.B #H'01,R0H ;Increment exponent
146 FADD_cod C 00D2 A0FF CMP.B #H'FF,R0H
147 FADD_cod C 00D4 4638 BNE LBL23 ;Branch if not exponent=H'FF
148 FADD_cod C 00D6 5A000000 JMP @LBL1 ;Jump
149
150 FADD_cod C 00DA LBL17
151 FADD_cod C 00DA 1931 SUB.W R3,R1 ;Substruct mantissa
152 FADD_cod C 00DC 1A08 SUBX.B R2L,R0L
153 FADD_cod C 00DE 4604 BNE LBL18 ;Branch if Z=0
154 FADD_cod C 00E0 F000 MOV.B #H'00,R0H ;Clear R0H
155 FADD_cod C 00E2 5470 RTS
156  FADD_cod  C  00E4   LBL18
157  FADD_cod  C  00E4  440E   BCC  LBL19  ;Branch if C = 0
158  FADD_cod  C  00E6  710E   BNOT  #0,R6L  ;Bit not sign bit
159  FADD_cod  C  00E8  1708   NOT  R0L  ;2's complement mantissa
160  FADD_cod  C  00EA  1701   NOT  R1H
161  FADD_cod  C  00EC  1709   NOT  R1L
162  FADD_cod  C  00EE  8901   ADD.B  #H'01,R1L
163  FADD_cod  C  00F0  9100   ADDX.B  #H'00,R1H
164  FADD_cod  C  00F2  9800   ADDX.B  #H'00,R0L
165  ;
166  FADD_cod  C  00F4   LBL19
167  FADD_cod  C  00F4  1009   SHLL  R1L  ;Shift mantissa 1 bit left
168  FADD_cod  C  00F6  1201   ROTXL  R1H
169  FADD_cod  C  00F8  1208   ROTXL  R0L
170  FADD_cod  C  00FA  1A00   DEC.B  R0H  ;Decrement exponent
171  FADD_cod  C  00FC  470C   BEQ  LBL22  ;Branch if exponent=0
172  FADD_cod  C  00FE  44F4   BCC  LBL19  ;Branch if exponent>0
173  FADD_cod  C  0100   LBL20
174  FADD_cod  C  0100  0A00   INC.B  R0H  ;Increment exponent
175  FADD_cod  C  0102   LBL21
176  FADD_cod  C  0102  1308   ROTXR  R0L  ;Rotate mantissa 1 bit right
177  FADD_cod  C  0104  1301   ROTXR  R1H
178  FADD_cod  C  0106  1309   ROTXR  R1L
179  FADD_cod  C  0108  4004   BRA  LBL23  ;Branch always
180  FADD_cod  C  010A   LBL22
181  FADD_cod  C  010A  45F4   BCS  LBL20  ;Branch if C = 1
182  FADD_cod  C  010C  40F4   BRA  LBL21  ;Branch always
183  ;
184  FADD_cod  C  010E   LBL23  ;Change floating point format
185  FADD_cod  C  010E  1100   SHLR  R0H
186  FADD_cod  C  0110  6778   BST  #7,R0L
187  FADD_cod  C  0112  770E   BLD  #0,R6L
188  FADD_cod  C  0114  6770   BST  #7,R0H
189  FADD_cod  C  0116  5470   RTS
190  ;
191  .END

*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
About Single-Precision Floating-Point Numbers <Reference>

Single-Precision Floating-Point Formats:

1. Internal representation of single-precision floating-point numbers

In this Application Note, the following formats are applied to single-precision floating-point numbers depending on their values \( R = \text{real number} \):

A. Internal representation for \( R = 0 \)

\[
\begin{array}{cccccccccccccccccccccccc}
31 & 30 & 29 & \cdots & \cdots & 2 & 1 & 0 \\
0 & 0 & 0 & \cdots & \cdots & 0 & 0 & 0 \\
\end{array}
\]

All of the 32 bits are 0's.

B. Normalized format

\[
\begin{array}{cccccccccccccccccccccccc}
31 & 30 & \alpha & 23 & 22 & 0 \\
S & \alpha & \beta & \cdots & \cdots & 0 \\
\end{array}
\]

\( \alpha \) is an exponent whose field is 8 bits long, \( \beta \) is a mantissa whose field is 23 bits long. The value of \( R \) can be represented by the following equation (on conditions that \( 1 \leq \alpha \leq 254 \)):

\[
R = 2^S \times 2^{\alpha-127} \times (1 + 2^{-1} \times \beta_{22} + 2^{-2} \times \beta_{21} + \ldots \ldots + 2^{-23} \times \beta_0)
\]

where \( \beta_i \) is the value of the i-th bit \( (0 \leq i \leq 22) \) and \( S \) is the sign bit.

C. Denormalized format

\[
\begin{array}{cccccccccccccccccccccccc}
31 & 30 & 23 & 22 & 0 \\
S & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \beta \\
\end{array}
\]

where \( \beta \) is a mantissa whose field is 23 bits long. This format is used to represent a real number too small to be represented in the normal format. In this format, \( R \) can be represented by the following equation:

\[
R = 2^S \times 2^{-126} \times (2^{-1} \times \beta_{22} + 2^{-2} \times \beta_{21} + \ldots \ldots + 2^{-23} \times \beta_0)
\]

D. Infinity

\[
\begin{array}{cccccccccccccccccccccccc}
31 & 30 & 23 & 22 & 0 \\
S & 1 & 1 & 1 & 1 & 1 & 1 & 1 & \beta \\
\end{array}
\]

where \( \beta \) is a mantissa whose field is 23 bits long. In this Application Note, however, the following rules apply if all exponents are 1's;

Positive infinity when \( S = 0 \)

\( R = +\infty \)

Negative infinity when \( S = 1 \)

\( R = -\infty \)
2. Example of internal representation

If \( S = \text{B'}0 \) (binary)
\[ \alpha = \text{B'}10000011 \] (binary)
\[ \beta = \text{B'}1011100……0 \] (binary)

Then the corresponding real number is as follows:
\[ R = 2^0 \times 2^{131-127} \times (1 + 2^{-1} + 2^{-3} + 2^{-4} + 2^{-5}) \]
\[ = 16 + 8 + 2 + 1 + 0.5 = 27.5 \]

A. Maximum and minimum values

The maximum value (\( R_{\text{MAX}} \)) and minimum value (\( R_{\text{MIN}} \)), in terms of the absolute value, are as follows:
\[ R_{\text{MAX}} = 2^{254-127} \times (1 + 2^{-1} + 2^{-2} + 2^{-3} \ldots + 2^{-23}) \]
\[ = 3.37 \times 10^{38} \]
\[ R_{\text{MIN}} = 2^{-126} \times 2^{-23} = 2^{-149} = 1.40 \times 10^{-45} \]

The absolute values within the above range can be represented.
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