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# H8/300L Super Low Power Series

## Addition of Multiple-Precision Binary Numbers (ADD2)

### Introduction

The software ADD2 adds a multiple-precision binary number to another multiple-precision binary number and places the result in the data memory where the augend was placed.

### Target Device

H8/38024

### Contents

## 1. Arguments

| Description | | Memory area | Data length (bytes) |
|---|---|---|---|
| Input | Augend and addend byte length | R0L | 1 |
| | Start address of augend | R3 | 2 |
| | Start address of addend | R4 | 2 |
| Output | Start address of the result of addition | R3 | 2 |
| | Error | Z flag (CCR) | — |
| | Carry | C flag (CCR) | — |

## 2. Changes to Internal Registers and Flags

| R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 |
|---|---|---|---|---|---|---|---|
| × | × | × | ○ | × | × | — | — |

| I | U | H | U | N | Z | V | C |
|---|---|---|---|---|---|---|---|
| — | — | × | — | × | ○ | × | ○ |

Legend
—: No change
×: Undefined
○: Result

## 3. Specifications

| |
|---|
| Program memory (bytes) |
| 42 |
| Data memory (bytes) |
| 0 |
| Stack (bytes) |
| 0 |
| Clock cycle count |
| 7170 |
| Reentrant |
| Possible |
| Relocation |
| Possible |
| Interrupt |
| Possible |

## 4. Notes

The clock cycle count (7170) in the specifications is for addition of 255 bytes to 255 bytes.

## 5. Description

### 5.1 Details of functions

1. The following arguments are used with the software ADD2:
   - R0L: Sets, as an input argument, the byte count of an augend and an addend in 2-digit hexadecimals.
   - R3: Contains the start address of the augend in the data memory area. The start address of the result of addition is placed in this register after execution of the software ADD2.
   - R4: Sets, as an input argument, the start address of the addend in the data memory area.
   - Z flag (CCR): Indicates an error in data length as an output argument.
     - Z flag = 0: The data byte count (R0L) was not 0.
     - Z flag = 1: The data byte count (R0L) was 0 (indicating an error).
   - C flag (CCR): Indicates the presence or absence of a carry, as an output argument, after execution of the software ADD2.
     - C flag = 0: No carry occurred in the result of addition.
     - C flag = 1: A carry occurred in the result of addition (see figure 2).

2. The following figure illustrates the execution of the software ADD2. When the input arguments are set as shown in (1), the result of addition is placed in the data memory area as shown in (2).

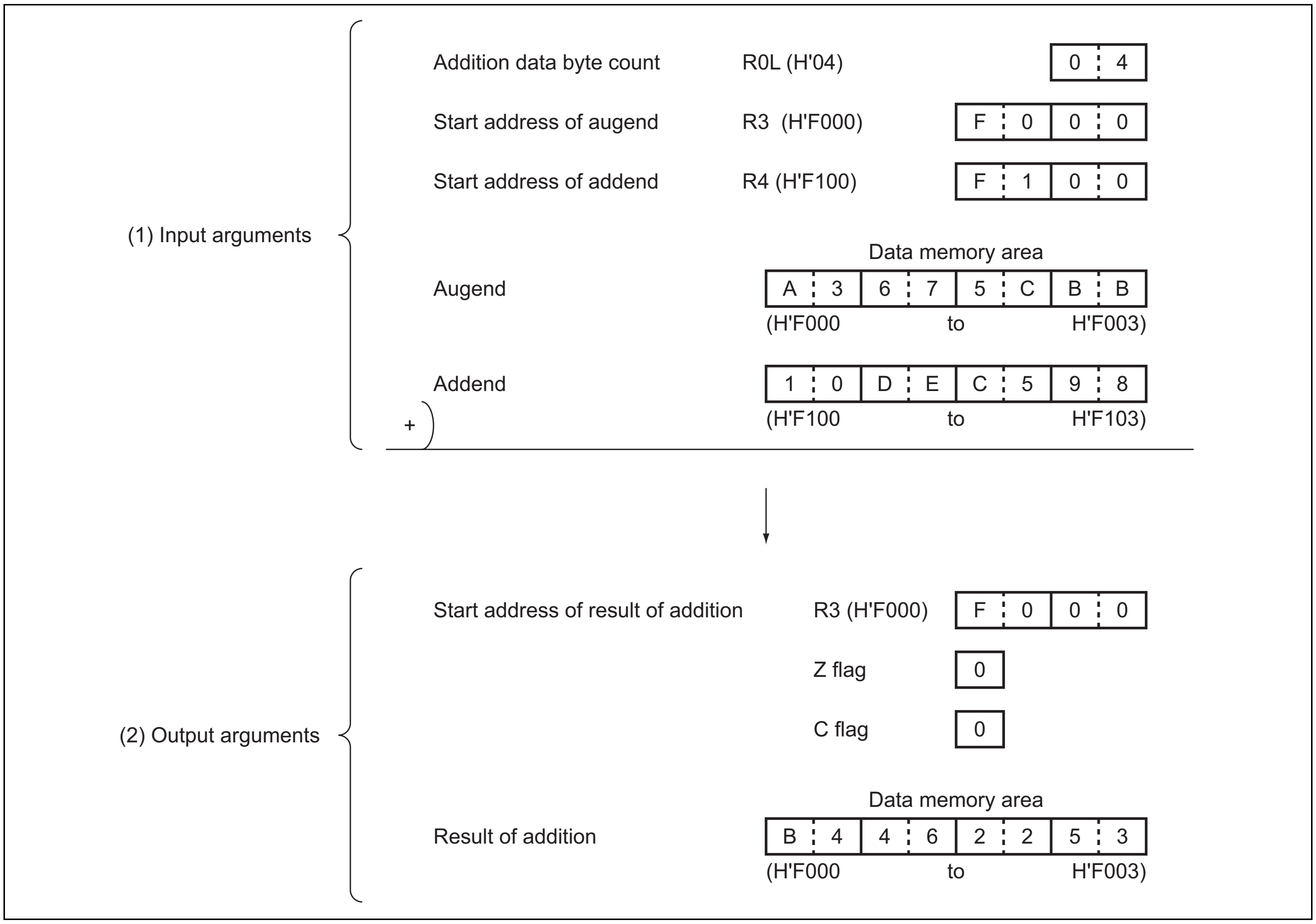



**Figure 1 Example of Software ADD2 Execution**

Figure 2 shows an example of addition with a carry that occurred in the result.

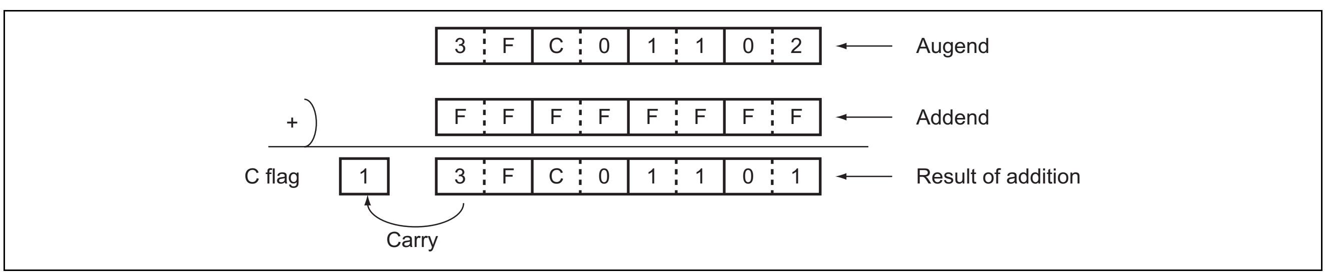



**Figure 2 Example of Addition with a Carry**

## 5.2 Notes on usage

1. When the upper bits are not used (see figure 3), set them to 0. The software ADD2 performs byte-based addition; when 0 are not set in the unused upper bits, a correct result cannot be obtained because the addition is done on the numbers including indeterminate data.

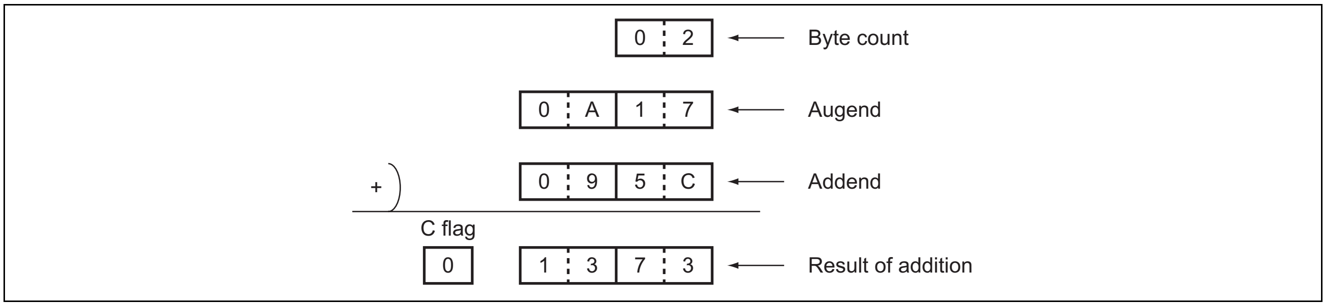



**Figure 3 Example of Addition with Upper Bits Unused**

2. After execution of the software ADD2, the augend will be lost because the result is placed in the data memory area where the augend was set. When the augend is still needed after software ADD2 execution, save it in memory.

## 5.3 Data memory

The software ADD2 uses no data memory.

## 5.4 Example of usage

This is an example of adding 8 bytes of data. Set the start addresses of a byte count, an augend and an addend in the registers and call the software ADD2 as a subroutine.

```
WORK1     . RES. W     2          --------- Reserve a data memory area in which the user program places
                                            a 32-bit binary dividend.

WORK2     . RES. W     2          --------- Reserve a data memory area in which the user program places
                                            a 16-bit binary divisor.

WORK3     . RES. W     2          --------- Reserve a data memory area in which the user program places
                                            a 32-bit binary quotient.

WORK4     . RES. W     2          --------- Reserve a data memory area in which the user program places
                .                           a 32-bit binary remainder.
                .
                .
          MOV. W       @WORK1, R0    }------ Contain the 32-bit binary dividend set by
          MOV. W       @WORK1+2, R1  }       the user program.

          MOV. W       @WORK2, R2    }------ Contain the 32-bit binary divisor set by
          MOV. W       @WORK2+2, R3  }       the user program.

        | JSR          @DIV        |  ------- Call the software DIV as a subroutine.

          BEQ          ERROR          ------- Branch to the error processing routine
                                              when an error has occurred as the result of division.
          MOV. W R0,   @WORK3        }
          MOV. W R1,   @WORK3+2      }------ Place the result of division set in the output
          MOV. W R4,   @WORK4        }       arguments in the data memory of the user program.
          MOV. W R5,   @WORK4+2      }
                .
                .
                .
ERROR     | Error processing routine |
```

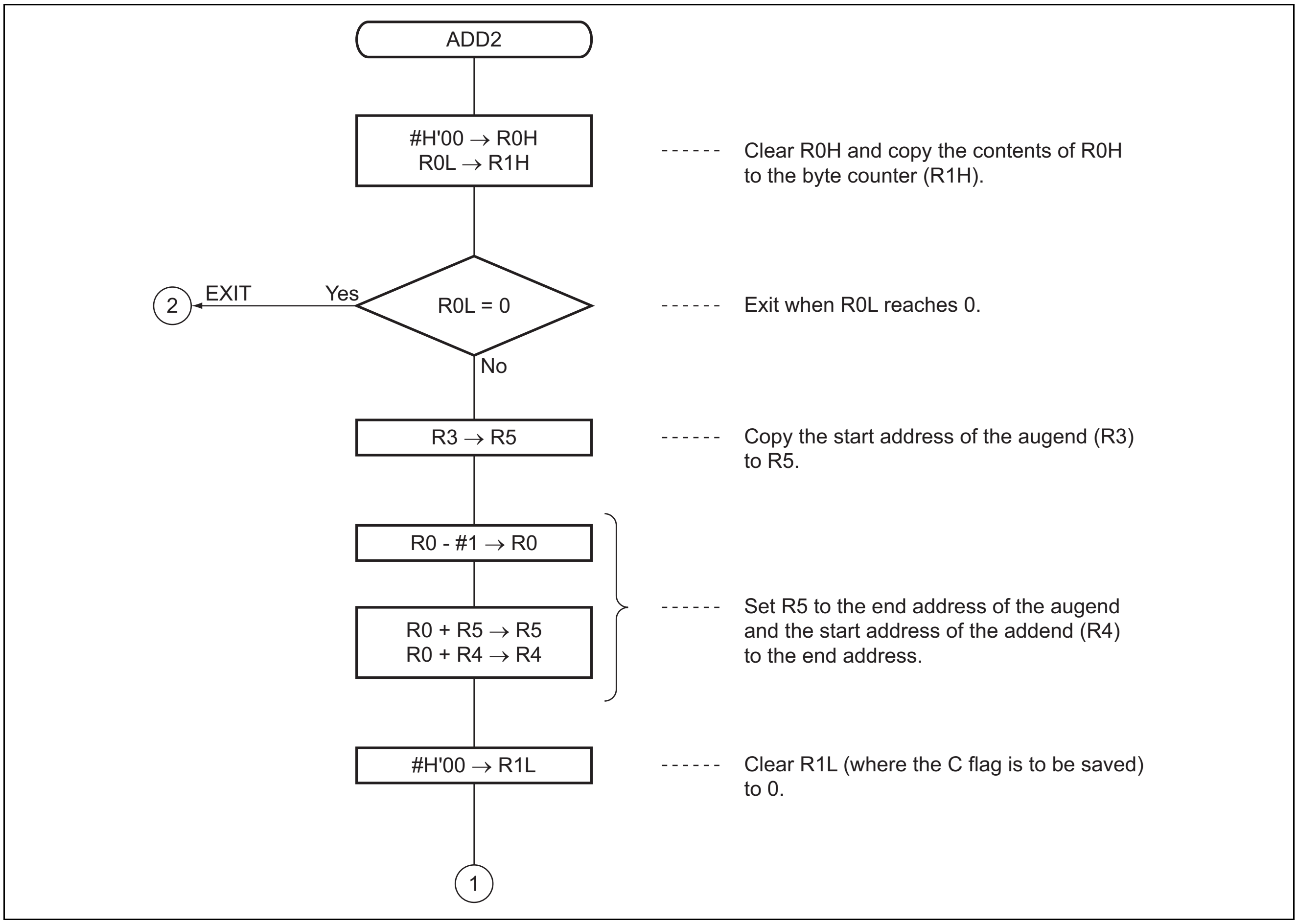
## 5.5 Operation

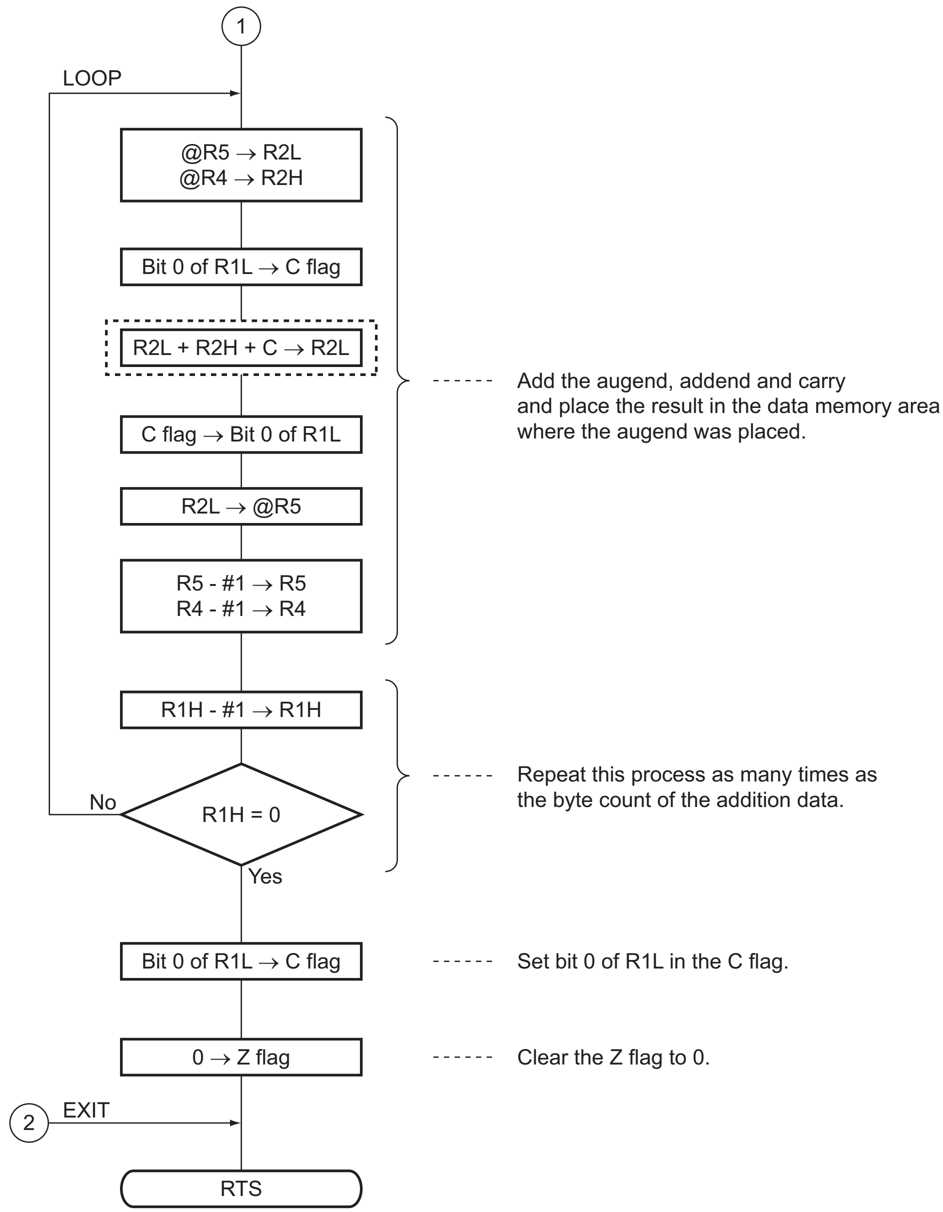
1. Addition of multiple-precision binary numbers can be done by performing a series of addb instructions with a carry flag (ADDX.B) as the augend and addend data are placed in registers on a byte basis.
2. The end address of the data memory area containing the augend is placed in R3, and the end address of the data memory area containing the addend is placed in R4.
3. R1L is cleared for saving the C flag.
4. The augend and addend are loaded in R2L and R2H respectively, byte by byte, starting at their end address and equation 1 is executed:

$$\left.\begin{array}{r}\text{Augend} + \text{addend} + \text{C} \rightarrow \text{R2L} \\ \text{R2L} \rightarrow \text{@R3}\end{array}\right\} \text{ ------- equation 1}$$

   where the C flag indicates a carry that may occur in the result of addition of the lower bytes.
5. The result of step 4 is placed in the data memory area for the augend.
6. R3, R4, and R0L are decremented each time the operation of steps 4 and 5 has finished. This processing is repeated until R0L reaches 0.

## 6. Flowchart


ADD2
#H'00 → R0H
R0L → R1H
Clear R0H and copy the contents of R0H to the byte counter (R1H).
R0L = 0
Yes
EXIT
2
No
Exit when R0L reaches 0.
R3 → R5
Copy the start address of the augend (R3) to R5.
R0 - #1 → R0
R0 + R5 → R5
R0 + R4 → R4
Set R5 to the end address of the augend and the start address of the addend (R4) to the end address.
#H'00 → R1L
Clear R1L (where the C flag is to be saved) to 0.
1




Note: ADD2 is the same as SUB2, ADDD2 and SUBD2 except for the stop surrounded by dotted lines.

## 7. Program List

```
*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 09:59:33
PROGRAM NAME =
                                  ;****************************************************************
                                  ;*
                                  ;*      00 - NAME    :MULTIPLE PRECISION BINARY ADDITION
                                  ;*                    (ADD2)
                                  ;*
                                  ;****************************************************************
                                  ;*
                                  ;*      ENTRY        :R0L (BYTE LENGTH OF ADDTION DATA)
                                  ;*                    R3 (START ADDRESS OF SUMMAND)
                                  ;*                    R4 (START ADDRESS OF ADDEND)
                                  ;*
                                  ;*      RETURNS      :R3 (START ADDRESS OF RESULT)
                                  ;*                    Z flag OF CCR (Z=0;TRUE , Z=1;FALSE)
                                  ;*                    C flag OF CCR (C = 0;TRUE , C = 1;OVER FLOW)
                                  ;*
                                  ;****************************************************************
                                  ;
ADD2_cod C    0000                        .SECTION            ADD2_code,CODE,ALIGN=2
                                          .EXPORT  ADD2
                                  ;
ADD2_cod C          00000000      ADD2    .EQU $              ;Entry point
ADD2_cod C    0000  F000                  MOV.B    #H'00,R0H  ;Clear R0H
ADD2_cod C    0002  0C81                  MOV.B    R0L,R1H    ;Set byte counter(R1H)
ADD2_cod C    0004  4722                  BEQ      EXIT       ;Branch if R0L=0
ADD2_cod C    0006  0D35                  MOV.W    R3,R5      ;R3 -> R5
ADD2_cod C    0008                MAIN
ADD2_cod C    0008  1B00                  SUBS.W   #1,R0      ;Decrement R0
ADD2_cod C    000A  0905                  ADD.W    R0,R5      ;Set start address of summand(R5)
ADD2_cod C    000C  0904                  ADD.W    R0,R4      ;Set start address of addend(R4)
ADD2_cod C    000E  F900                  MOV.B    #H'00,R1L  ;Clear R1L
ADD2_cod C    0010                LOOP
ADD2_cod C    0010  685A                  MOV.B    @R5,R2L    ;Load summand to R2L
ADD2_cod C    0012  6842                  MOV.B    @R4,R2H    ;Load addend to R2H
ADD2_cod C    0014  7709                  BLD      #0,R1L     ;Load bit 0 of R1L to C flag
ADD2_cod C    0016  0E2A                  ADDX.B   R2H,R2L    ;Addition
ADD2_cod C    0018  6709                  BST      #0,R1L     ;Store C flag to bit 0 of R1L
ADD2_cod C    001A  68DA                  MOV.B    R2L,@R5    ;Store result
ADD2_cod C    001C  1B05                  SUBS.W   #1,R5      ;Decrement summand address(R5)
ADD2_cod C    001E  1B04                  SUBS.W   #1,R4      ;Decrement addend address(R4)
ADD2_cod C    0020  1A01                  DEC.B    R1H        ;Decrement byte counter(R1H)
ADD2_cod C    0022  46EC                  BNE      LOOP       ;Branch if Z=0
                                  ;
ADD2_cod C    0024  7709                  BLD      #0,R1L     ;Load bit 0 of R1L to c flag
ADD2_cod C    0026  06FB                  ANDC.B   #H'FB,CCR  ;Clear Z flag
ADD2_cod C    0028                EXIT
ADD2_cod C    0028  5470                  RTS
                                  ;
                                          .END
*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
```

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