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Renesas Electronics Corporation

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M16C/64 Group

A/D Converter Operation (Single-Shot Mode, Extension Analog Input)

1. Abstract

In single-shot mode where extension analog inputs are used, any desired function can be selected from those listed in Table 1. In this application note, the operation of the function selected from the items in Table 1 (marked with a circle) is described.

Table 1. Contents of Settings

Set item	Content of setting		Set item	Content of setting	
Operating clock ϕAD	○	fAD divided by 12/ fAD divided by 6 /fAD divided by 4/ fAD divided by 3/ fAD divided by 2/ fAD	A/D conversion start condition	○	Software trigger
					$\overline{\text{ADTRG}}$ trigger
			Extension analog input pin	○	ANEX0 pin
					ANEX1 pin

2. Introduction

The application example presented in this document applies to the microcomputers listed below.

・Microcomputers: M16C/64 group

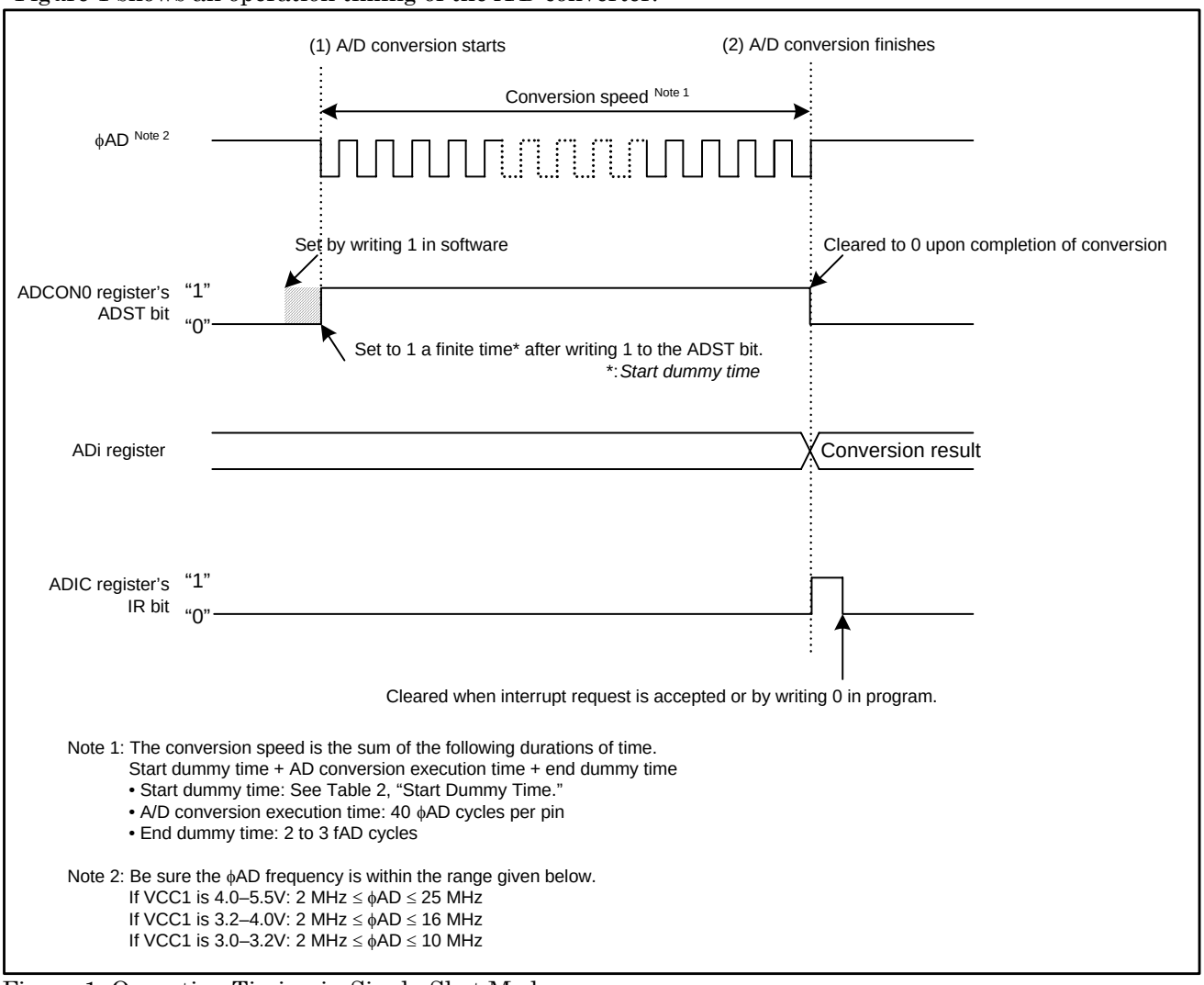
This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

Operation (1) When the ADCON0 register's ADST bit is set to 1 (A/D conversion start), the A/D converter converts the input voltage on ANEXi pin (i = 0, 1) from analog to digital quantities.

(2) After the A/D conversion is finished, the content of the successive approximation register (conversion result) is transferred to the ADi register. At the same time, the ADIC register's IR bit is set to 1 (interrupt requested). Also, the ADCON0 register's ADST bit is cleared to 0 (A/D conversion stopped), causing the A/D converter to stop operating.

Figure 1 shows an operation timing of the A/D converter.



Note 1: The conversion speed is the sum of the following durations of time.
Start dummy time + AD conversion execution time + end dummy time
- Start dummy time: See Table 2, "Start Dummy Time."
- A/D conversion execution time: 40 ϕAD cycles per pin
- End dummy time: 2 to 3 fAD cycles

Note 2: Be sure the ϕAD frequency is within the range given below.
If VCC1 is 4.0–5.5V: 2 MHz ≤ ϕAD ≤ 25 MHz
If VCC1 is 3.2–4.0V: 2 MHz ≤ ϕAD ≤ 16 MHz
If VCC1 is 3.0–3.2V: 2 MHz ≤ ϕAD ≤ 10 MHz

Figure 1. Operation Timing in Single-Shot Mode

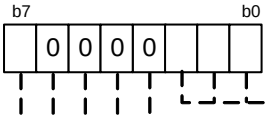
Table 2. Start Dummy Time

Selected ϕAD	Start dummy time
fAD	1 to 2 fAD cycles
fAD divided by 2	2 to 3 fAD cycles
fAD divided by 3	3 to 4 fAD cycles
fAD divided by 4	3 to 4 fAD cycles
fAD divided by 6	4 to 5 fAD cycles
fAD divided by 12	7 to 8 fAD cycles

4. How to Set Up

The following shows how to set up the registers to accomplish the operation described in Section 3, "Application Example." For details about each register, see the hardware manual of the M16C/64 group.

(1) Set up the A/D control register 0, A/D control register 1, and A/D control register 2.

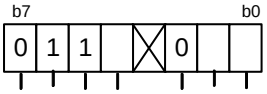


A/D control register 0 (ADCON0)

- CH2–CH0 Analog input pin select bits
  Have no effect when extension analog input pins are used.
- MD0–MD1 A/D operation mode select bits
  00: Single-shot mode
- TRG Trigger select bit
  0: Software trigger
- ADST A/D conversion start flag
  0: A/D conversion stopped
- CKS0 Clock frequency select bit Note 1

Note 1: Selection of the operating clock, ϕAD
The clock ϕAD is selected using the following register bits in combination.
- ADCON0 register's CKS0 bit
- ADCON1 register's CKS1 bit
- ADCON2 register's CKS2 bit

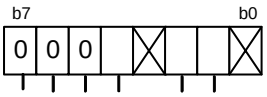
CKS2	CKS1	CKS0	ϕAD
0	0	0	fAD divided by 4
0	0	1	fAD divided by 2
0	1	0	fAD
0	1	1	
1	0	0	fAD divided by 12
1	0	1	fAD divided by 6
1	1	0	fAD divided by 3
1	1	1	



A/D control register 1 (ADCON1)

- SCAN0–SCAN1 A/D sweep pin select bits
  Have no effect in single-shot mode.
- MD2 A/D operation mode select bit 1
  0: Other than repeat sweep mode 1
- CKS1 Clock frequency select bit 1 Note 1
- ADSTBY A/D standby bit
  1: A/D operation ready
- ADEX1–ADEX0 Extension pin select bits
  01: A/D converts ANEX0 input

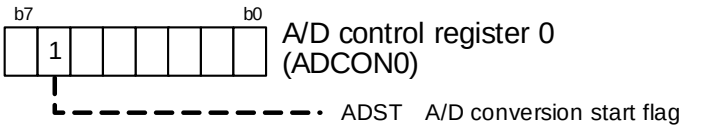
If the ADSTBY bit is changed from 0 (A/D operation stopped) to 1 (A/D operation ready), wait 1 ϕAD cycle or more before starting A/D conversion.



A/D control register 2 (ADCON2)

- ADGSEL1–ADGSEL0 A/D input group select bits
  00: Selects port P10 group
  01: Setting prohibited
  10: Selects port P0 group
  11: Selects port P2 group
- CKS2 Clock frequency select bit 2 Note 1
- Reserved bits
  Set these bits to 0.

(2) Start A/D conversion.

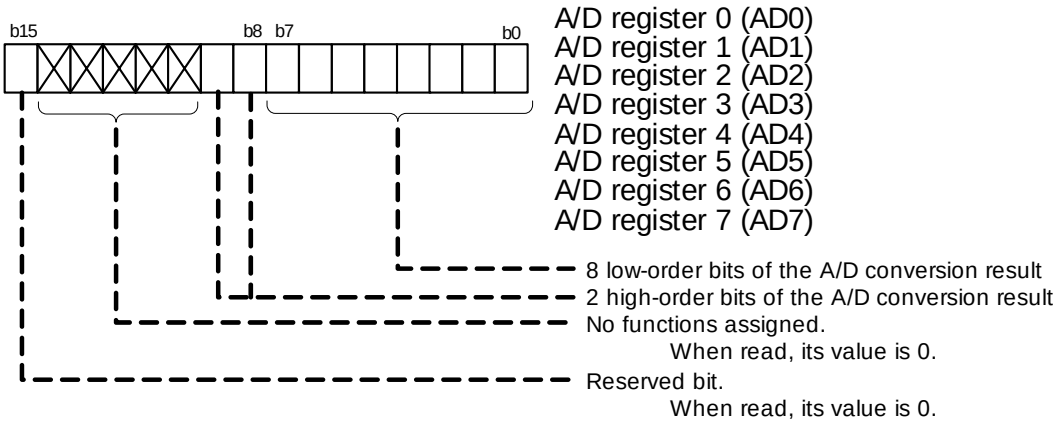


The ADST bit reads 0 when it is read before an A/D conversion starts after writing 1 to the ADST bit.

(3) Wait until the A/D conversion is finished.

When the A/D conversion on a specified extension analog input pin is finished, the ADIC register' s IR bit is set to 1 (interrupt requested). At the same time, the ADST bit it cleared to 0 (A/D conversion stopped).

(4) Read out the A/D conversion result.



5. Reference Sample Programs

Download reference sample programs from the Renesas Technology website.

Click the screen menu “Application Note” on the left side of the M16C family top page.

6. Reference Documents

Hardware manuals

M16C/64 Group Hardware Manual

(Obtain the latest edition from the Renesas Technology website.)

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