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April 1\textsuperscript{st}, 2010  
Renesas Electronics Corporation

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1. Abstract

In single-shot mode where extension analog inputs are used, any desired function can be selected from those listed in Table 1. In this application note, the operation of the function selected from the items in Table 1 (marked with a circle) is described.

Table 1. Contents of Settings

<table>
<thead>
<tr>
<th>Set item</th>
<th>Content of setting</th>
<th>Set item</th>
<th>Content of setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating clock</td>
<td>fAD divided by 12/ fAD divided by 6 /fAD divided by 4/ fAD divided by 3/ fAD divided by 2/ fAD</td>
<td>A/D conversion start condition</td>
<td>Software trigger</td>
</tr>
<tr>
<td>φAD</td>
<td></td>
<td></td>
<td>ADTRG trigger</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ANEX0 pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ANEX1 pin</td>
</tr>
<tr>
<td>Extension analog</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>input pin</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2. Introduction

The application example presented in this document applies to the microcomputers listed below.

• Microcomputers: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Application Example

Operation
(1) When the ADCON0 register’s ADST bit is set to 1 (A/D conversion start), the A/D converter converts the input voltage on ANEXi pin (i = 0, 1) from analog to digital quantities.
(2) After the A/D conversion is finished, the content of the successive approximation register (conversion result) is transferred to the ADi register. At the same time, the ADIC register’s IR bit is set to 1 (interrupt requested). Also, the ADCON0 register’s ADST bit is cleared to 0 (A/D conversion stopped), causing the A/D converter to stop operating.

Figure 1 shows an operation timing of the A/D converter.

Table 2. Start Dummy Time

<table>
<thead>
<tr>
<th>Selected φAD</th>
<th>Start dummy time</th>
</tr>
</thead>
<tbody>
<tr>
<td>φAD</td>
<td>1 to 2 φAD cycles</td>
</tr>
<tr>
<td>φAD divided by 2</td>
<td>2 to 3 φAD cycles</td>
</tr>
<tr>
<td>φAD divided by 3</td>
<td>3 to 4 φAD cycles</td>
</tr>
<tr>
<td>φAD divided by 4</td>
<td>3 to 4 φAD cycles</td>
</tr>
<tr>
<td>φAD divided by 6</td>
<td>4 to 5 φAD cycles</td>
</tr>
<tr>
<td>φAD divided by 12</td>
<td>7 to 8 φAD cycles</td>
</tr>
</tbody>
</table>
4. How to Set Up

The following shows how to set up the registers to accomplish the operation described in Section 3, “Application Example.” For details about each register, see the hardware manual of the M16C/64 group.

(1) Set up the A/D control register 0, A/D control register 1, and A/D control register 2.

A/D control register 0 (ADCON0)

- CH2–CH0  Analog input pin select bits
  Have no effect when extension analog input pins are used.
- MD0–MD1  A/D operation mode select bits
  00: Single-shot mode
- TRG  Trigger select bit
  0: Software trigger
- ADST  A/D conversion start flag
  0: A/D conversion stopped
- CKS0  Clock frequency select bit

Note 1: Selection of the operating clock, φAD
The clock φAD is selected using the following register bits in combination.
- ADCON0 register’s CKS0 bit
- ADCON1 register’s CKS1 bit
- ADCON2 register’s CKS2 bit

<table>
<thead>
<tr>
<th>CKS2</th>
<th>CKS1</th>
<th>CKS0</th>
<th>φAD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>fAD divided by 4</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>fAD divided by 2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>fAD</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>fAD divided by 12</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>fAD divided by 6</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>fAD divided by 3</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>fAD</td>
</tr>
</tbody>
</table>

If the ADSTBY bit is changed from 0 (A/D operation stopped) to 1 (A/D operation ready), wait 1 φAD cycle or more before starting A/D conversion.

A/D control register 1 (ADCON1)

- SCAN0–SCAN1  A/D sweep pin select bits
  Have no effect in single-shot mode.
- MD2  A/D operation mode select bit 1
  0: Other than repeat sweep mode 1
- CKS1  Clock frequency select bit 1
- ADSTBY  A/D standby bit
  1: A/D operation ready
- ADEX1–ADEX0  Extension pin select bits
  01: A/D converts ANEX0 input

A/D control register 2 (ADCON2)

- ADGSEL1–ADGSEL0  A/D input group select bits
  00: Selects port P10 group
  01: Setting prohibited
  10: Selects port P0 group
  11: Selects port P2 group
- CKS2  Clock frequency select bit 2
- Reserved bits
  Set these bits to 0.
(2) Start A/D conversion.

A/D control register 0 (ADCON0)

- ADST: A/D conversion start flag
  - 1: Starts A/D conversion

(3) Wait until the A/D conversion is finished.

When the A/D conversion on a specified extension analog input pin is finished, the ADIC register’s IR bit is set to 1 (interrupt requested). At the same time, the ADST bit is cleared to 0 (A/D conversion stopped).

(4) Read out the A/D conversion result.

A/D register 0 (AD0)
A/D register 1 (AD1)
A/D register 2 (AD2)
A/D register 3 (AD3)
A/D register 4 (AD4)
A/D register 5 (AD5)
A/D register 6 (AD6)
A/D register 7 (AD7)

- 8 low-order bits of the A/D conversion result
- 2 high-order bits of the A/D conversion result
- No functions assigned.
- When read, its value is 0.
- Reserved bit.
- When read, its value is 0.
5. Reference Sample Programs

Download reference sample programs from the Renesas Technology website.
Click the screen menu “Application Note” on the left side of the M16C family top page.

6. Reference Documents

Hardware manuals
M16C/64 Group Hardware Manual
(Obtain the latest edition from the Renesas Technology website.)

Technical updates and technical news
(Obtain the latest information from the Renesas Technology website.)
Renesas Website and Where to Contact for Support

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http://japan.renesas.com/m16c

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E-mail : csc@renesas.com

REVISION HISTORY

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<th>Rev.</th>
<th>Issue date</th>
<th>Content of revision</th>
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<tbody>
<tr>
<td>1.00</td>
<td>Mar 23, 2009</td>
<td>– First edition issued</td>
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