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M16C/64 Group

A/D Converter Operation (Repeated Sweep Mode 1)

1. Abstract

In repeated sweep mode 1, any desired function can be selected from the items listed in Table 1. This application note describes the operations performed when the contents marked with circles are selected out of the items shown in Table 1.

Table 1. Set Contents

Set item	Set content		Set item	Set content	
Operating clock ϕAD	○	fAD divided by 12 / fAD divided by 6 / fAD divided by 4 / fAD divided by 3 / fAD divided by 2 / fAD	Priority analog input pins to be A/D-converted	○	1 pin (AN0, AN1 / AN0_0, AN0_1 / AN2_0, AN2_1)
					2 pins (AN0–AN3 / AN0_0–AN0_3 / AN2_0–AN2_3)
A/D conversion start condition	○	Software trigger			3 pins (AN0–AN5 / AN0_0–AN0_5 / AN2_0–AN2_5)
		Triggered by $\overline{\text{ADTRG}}$			
A/D input group	○	Port P10 group (AN0–AN7)			4 pins (AN0–AN7 / AN0_0–AN0_7 / AN2_0–AN2_7)
		Port P0 group (AN0_0–AN0_7)			
		Port P2 group (AN2_0–AN2_7)			

2. Introduction

The application example described here applies for use with the microcomputers listed below.

・Microcomputers: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

Operation (1) When the ADST bit of the ADCON0 register is set to 1 (A/D conversion start), the A/D converter starts operating, converting the input voltage on AN0 pin from analog to digital quantities.

(2) When the A/D conversion for the AN0 pin is completed, the content of the successive approximation register (conversion result) is transferred to the AD0 register.

(3) If AN0 (1 pin) is made the priority pin, A/D conversion is performed repeatedly in order of AN0 → AN1 → AN0 → AN2 → …→ AN0 → AN7 → AN0 → AN1, and so on. Each time the /D conversion of one pin is finished, the conversion result is transferred to the ADi register (i = 0–7) corresponding to each pin. The IR bit of the ADIC register is not set to 1 (interrupt requested).

(4) The A/D converter does not stop until the ADST bit of the ADCON0 register is reset to 0 (A/D conversion stop) in a program.

Figure 1 shows the order in which the AN0–AN7 pins are scanned. Figure 2 shows the operation timing of A/D conversion.

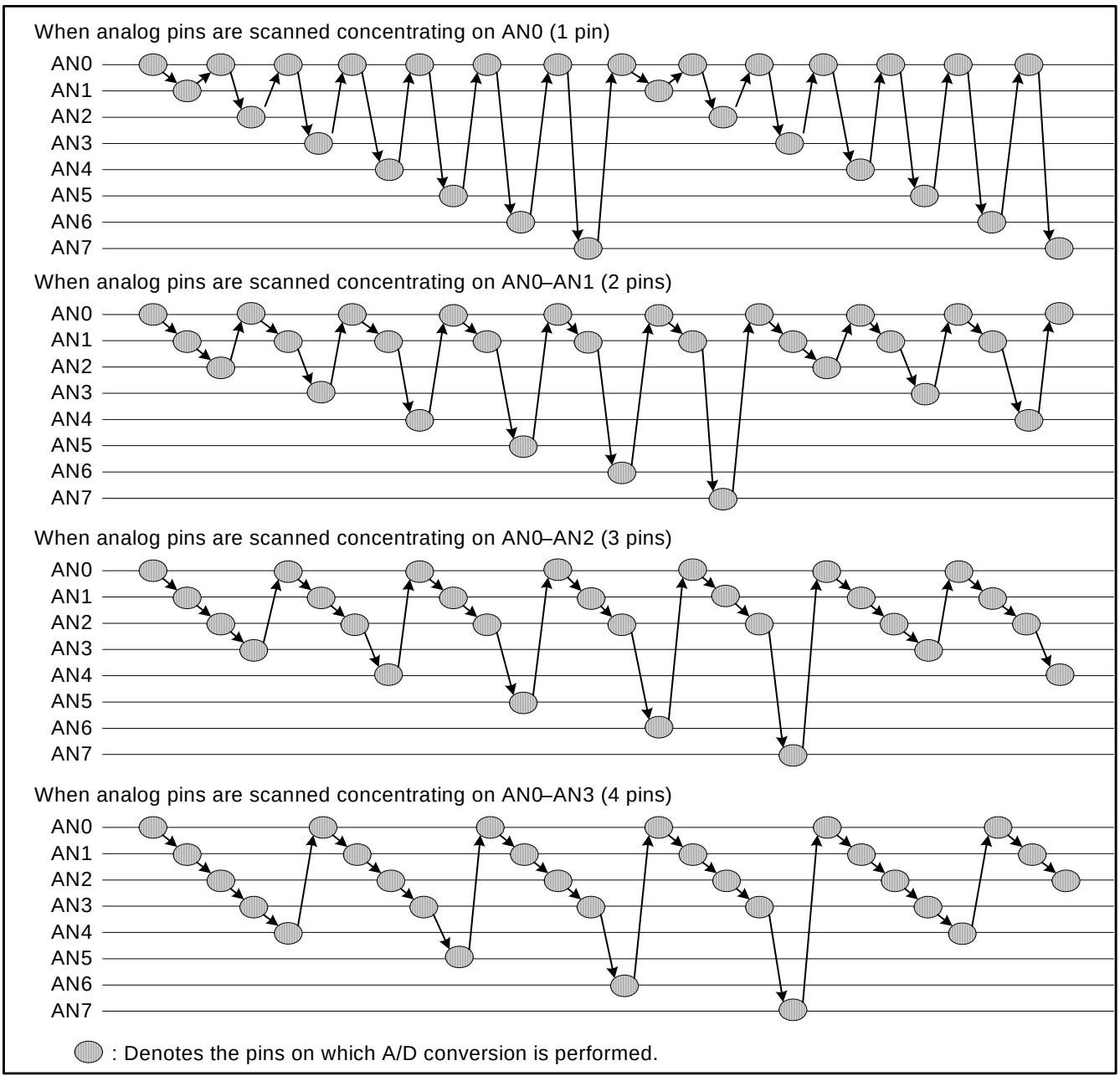
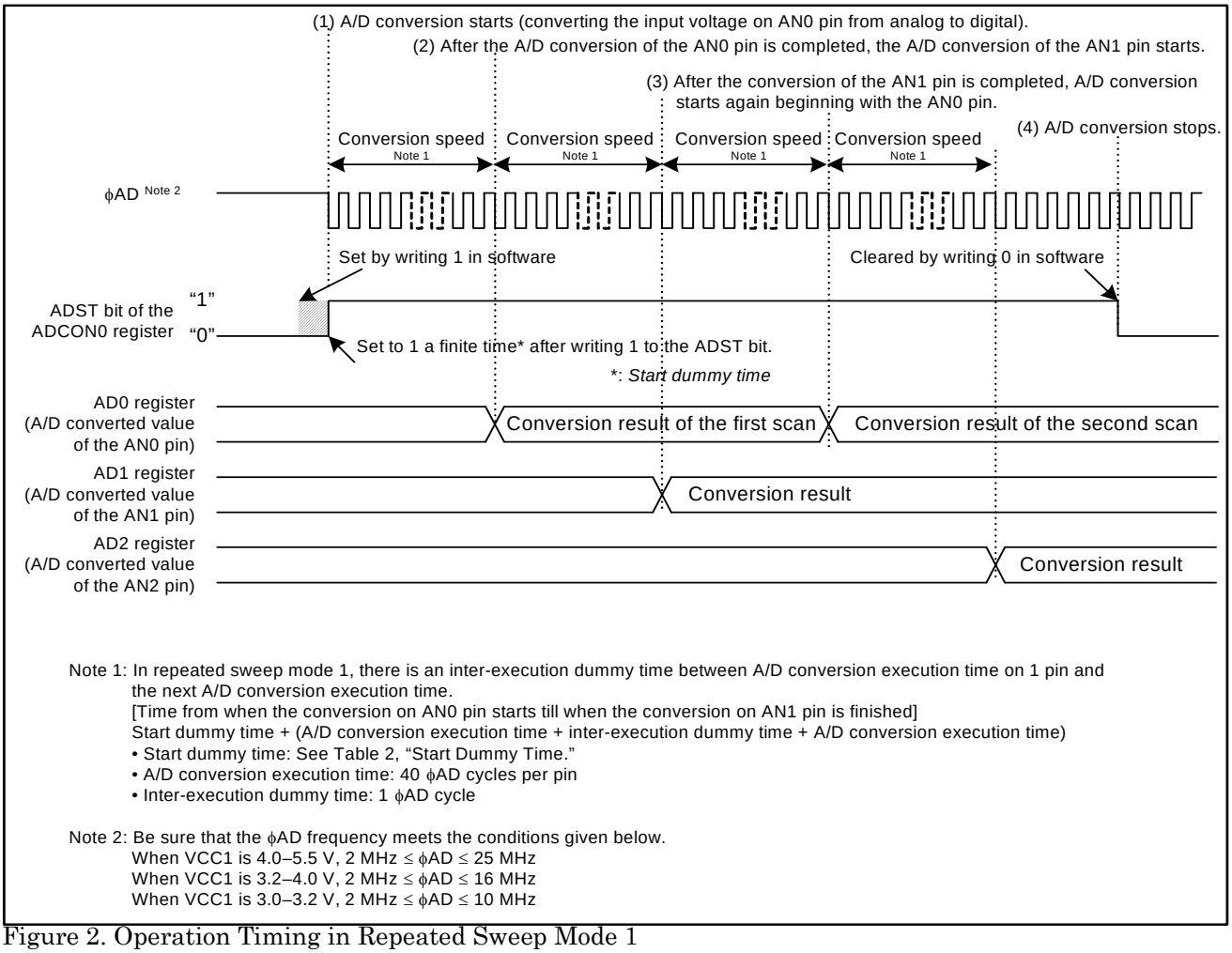


Figure 1. The Order in Which AN0–AN7 Pins are Scanned in Repeated Sweep Mode 1



Note 1: In repeated sweep mode 1, there is an inter-execution dummy time between A/D conversion execution time on 1 pin and the next A/D conversion execution time.
[Time from when the conversion on AN0 pin starts till when the conversion on AN1 pin is finished]
Start dummy time + (A/D conversion execution time + inter-execution dummy time + A/D conversion execution time)
• Start dummy time: See Table 2, "Start Dummy Time."
• A/D conversion execution time: 40 ϕAD cycles per pin
• Inter-execution dummy time: 1 ϕAD cycle

Note 2: Be sure that the ϕAD frequency meets the conditions given below.
When VCC1 is 4.0–5.5 V, 2 MHz ≤ ϕAD ≤ 25 MHz
When VCC1 is 3.2–4.0 V, 2 MHz ≤ ϕAD ≤ 16 MHz
When VCC1 is 3.0–3.2 V, 2 MHz ≤ ϕAD ≤ 10 MHz

Figure 2. Operation Timing in Repeated Sweep Mode 1

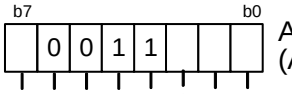
Table 2. Start Dummy Time

Selection of ϕAD	Start dummy time
fAD	1–2 fAD cycles
fAD divided by 2	2–3 fAD cycles
fAD divided by 3	3–4 fAD cycles
fAD divided by 4	3–4 fAD cycles
fAD divided by 6	4–5 fAD cycles
fAD divided by 12	7–8 fAD cycles

4. Setup Method

This section shows the setup procedure and set values necessary to realize the operation described in Section 3, "Application Example." See the M16C/64 group hardware manual for details about each register.

(1) Setting up the A/D control registers 0, 1 and 2

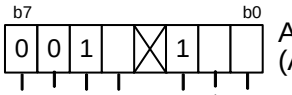


A/D control register 0 (ADCON0)

CH2–CH0 Analog input pin select bits
Have no effect in repeated sweep mode 1.
MD0–MD1 A/D operation mode select bits
11: Repeated sweep mode 0 or repeated sweep mode 1
TRG Trigger select bit
0: Trigger by software
ADST A/D conversion start flag
0: A/D conversion stops
CKS0 Clock frequency select bit Note 1

Note 1: Selection of the operating clock ϕAD
ϕAD can be selected in combination of the following.
• CKS0 bit of the ADCON0 register
• CKS1 bit of the ADCON1 register
• CKS2 bit of the ADCON2 register

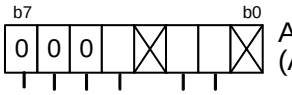
CKS2	CKS1	CKS0	ϕAD
0	0	0	fAD divided by 4
0	0	1	fAD divided by 2
0	1	0	fAD
0	1	1	
1	0	0	fAD divided by 12
1	0	1	fAD divided by 6
1	1	0	fAD divided by 3
1	1	1	



A/D control register 1 (ADCON1)

SCAN0–SCAN1 A/D sweep pin select bits
00: AN0 (1 pin)
01: AN0–AN1 (2 pins)
10: AN0–AN2 (3 pins)
11: AN0–AN3 (4 pins)
MD2 A/D operation mode select bit 1
0: Other than repeated sweep mode 1
CKS1 Clock frequency select bit 1 Note 1
ADSTBY A/D standby bit
1: A/D operation ready
ADEX1–ADEX0 Extended pin select bits
00: ANEX0, ANEX1 not used

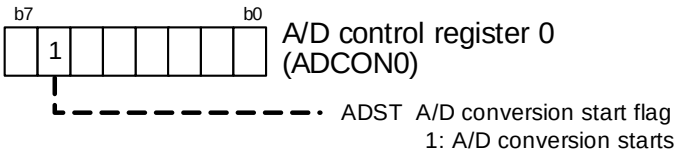
When the ADSTBY bit is changed from 0 (A/D operation idle) to 1 (A/D operation ready), be sure to wait 1 ϕAD cycle or more before starting A/D conversion.



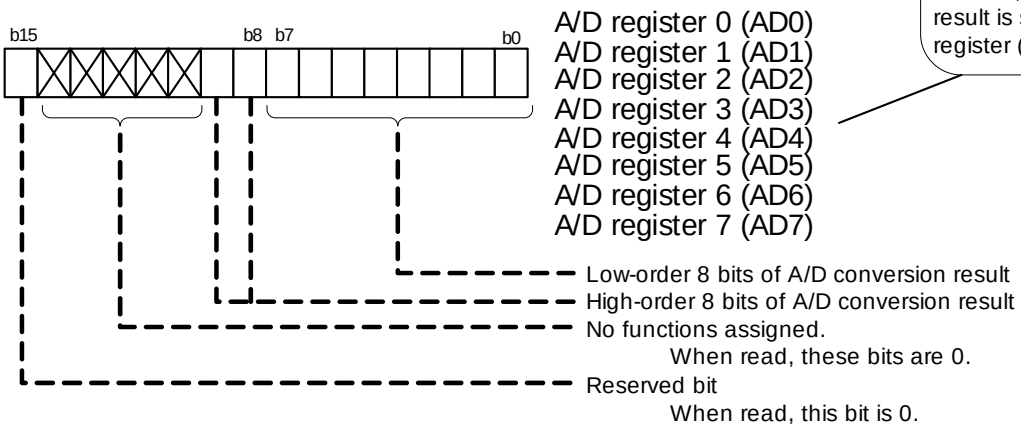
A/D control register 2 (ADCON2)

ADGSEL1–ADGSEL0 A/D input group select bits
00: Selects port P10 group
01: Settings prohibited
10: Selects port P0 group
11: Selects port P2 group
CKS2 Clock frequency select bit 2 Note 1
Reserved bits
Set these bits to 0.

(2) A/D conversion start



(3) A/D conversion result readout



5. Reference Sample Programs

Download reference sample programs from the Renesas Technology website.

Click the screen menu “Application Note” on the left side of the M16C family top page.

6. Reference Documents

Hardware manuals

M16C/64 Group Hardware Manual

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