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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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M16C/64 Group
A/D Converter Operation (Repeat Mode)

1. Abstract

In repeat mode, any desired function can be selected from those listed in Table 1. In this application note, the operation of the function selected from the items in Table 1 (marked with a circle) is described.

Table 1. Contents of Settings

<table>
<thead>
<tr>
<th>Set item</th>
<th>Content of setting</th>
<th>Set item</th>
<th>Content of setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating clock</td>
<td>fAD divided by 12/ fAD divided by 6/ fAD divided by 4/</td>
<td>Analog input pin</td>
<td>One from AN0–AN7</td>
</tr>
<tr>
<td>$AD</td>
<td>fAD divided by 3/ fAD divided by 2/ fAD</td>
<td></td>
<td>One from AN0_0–AN0_7</td>
</tr>
<tr>
<td></td>
<td>O</td>
<td></td>
<td>One from AN2_0–AN2_7</td>
</tr>
<tr>
<td>A/D conversion</td>
<td>Software trigger</td>
<td>Extension analog</td>
<td>Unused</td>
</tr>
<tr>
<td>start condition</td>
<td>ADTRG trigger</td>
<td>input pin</td>
<td></td>
</tr>
<tr>
<td></td>
<td>O</td>
<td></td>
<td>ANEX0 pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ANEX1 pin</td>
</tr>
</tbody>
</table>

2. Introduction

The application example presented in this document applies to the microcomputers listed below.

• Microcomputers: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Application Example

Operation  
1. When the ADCON0 register’s ADST bit is set to 1 (A/D conversion start), the A/D converter starts operating.
2. After the A/D conversion is finished, the content of the successive approximation register (conversion result) is transferred to the ADi register (i = 0–7). (The ADIC register’s IR bit is not set to 1 (interrupt requested).)
3. The A/D converter continues operating until the ADCON0 register’s ADST bit is cleared by writing 0 in a program. Each time an A/D conversion is finished, the conversion result is transferred to the ADi register.

Figure 1 shows an operation timing of the A/D converter.

![Figure 1. Operation Timing in Repeat Mode](image)

Note 1: In repeat mode, there is an interexecution dummy time inserted between an A/D conversion execution time on one pin and the next A/D conversion execution time. [Time from when conversion on ANi pin starts to when the second conversion finishes]
- Start dummy time + (A/D conversion execution time + interexecution dummy time + A/D conversion execution time)
  - Start dummy time: See Table 2, “Start Dummy Time.”
  - A/D conversion execution time: 40 $\phi_{AD}$ cycles per pin
  - Interexecution dummy time: 1 $\phi_{AD}$ cycle

Note 2: Be sure the $\phi_{AD}$ frequency is within the range given below.
If VCC1 is 4.0–5.5V: $2 \text{MHz} \leq \phi_{AD} \leq 25 \text{MHz}$
If VCC1 is 3.2–4.0V: $2 \text{MHz} \leq \phi_{AD} \leq 16 \text{MHz}$
If VCC1 is 3.0–3.2V: $2 \text{MHz} \leq \phi_{AD} \leq 10 \text{MHz}$

Table 2. Start Dummy Time

<table>
<thead>
<tr>
<th>Selected $\phi_{AD}$</th>
<th>Start dummy time</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\phi_{AD}$</td>
<td>1 to 2 $\phi_{AD}$ cycles</td>
</tr>
<tr>
<td>$\phi_{AD}$ divided by 2</td>
<td>2 to 3 $\phi_{AD}$ cycles</td>
</tr>
<tr>
<td>$\phi_{AD}$ divided by 3</td>
<td>3 to 4 $\phi_{AD}$ cycles</td>
</tr>
<tr>
<td>$\phi_{AD}$ divided by 4</td>
<td>3 to 4 $\phi_{AD}$ cycles</td>
</tr>
<tr>
<td>$\phi_{AD}$ divided by 6</td>
<td>4 to 5 $\phi_{AD}$ cycles</td>
</tr>
<tr>
<td>$\phi_{AD}$ divided by 12</td>
<td>7 to 8 $\phi_{AD}$ cycles</td>
</tr>
</tbody>
</table>
4. How to Set Up

The following shows how to set up the registers to accomplish the operation described in Section 3, “Application Example.” For details about each register, see the hardware manual of the M16C/64 group.

(1) Set up the A/D control register 0, A/D control register 1, and A/D control register 2.
(2) Start A/D conversion.

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A/D control register 0 (ADCON0)

ADST A/D conversion start flag
1: Starts A/D conversion

(3) Read out the A/D conversion result.

<table>
<thead>
<tr>
<th>b15</th>
<th>b14</th>
<th>b13</th>
<th>b12</th>
<th>b11</th>
<th>b10</th>
<th>b9</th>
<th>b8</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D register 0 (AD0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/D register 1 (AD1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/D register 2 (AD2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/D register 3 (AD3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/D register 4 (AD4)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/D register 5 (AD5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/D register 6 (AD6)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/D register 7 (AD7)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8 low-order bits of the A/D conversion result
2 high-order bits of the A/D conversion result
No functions assigned.
When read, its value is 0.

Reserved bit.
When read, its value is 0.

Each time an A/D conversion is finished, the A/D conversion result is stored in the ADi register (i = 0–7).
5. Reference Sample Programs

Download reference sample programs from the Renesas Technology website.
Click the screen menu “Application Note” on the left side of the M16C family top page.

6. Reference Documents

Hardware manuals
M16C/64 Group Hardware Manual
(Obtain the latest edition from the Renesas Technology website.)

Technical updates and technical news
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<table>
<thead>
<tr>
<th>Rev.</th>
<th>Issue date</th>
<th>Content of revision</th>
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<tbody>
<tr>
<td>1.00</td>
<td>Mar 23, 2009</td>
<td>First edition issued</td>
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