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April 1st, 2010
Renesas Electronics Corporation

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M16C/5LD and 56D Groups

A/D Conversion Using Timer B

1. Abstract

This document describes A/D conversion using timer B0, timer B1, and timer B2.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

- MCUs: M16C/5LD Group, M16C/56D Group

The sample program in this application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the hardware manual for any modifications to functions.

3. How to use A/D Trigger using Timer B

When bits HPTRG1 to HPTRG0 in registers ADTRGCON and ADITRGCON are 01b (timer B0 interrupt request), 10b (timer B1 interrupt request), or 11b (timer B2 interrupt request), an interrupt request for timer Bj can be used as the trigger to start A/D conversion ($j = 0$ to 2).

For the timer count source that generates the A/D trigger, select the f1 clock by setting the CKS3 bit in registers ADCON2 and AD1CON2, and set the count source periods to at least two times that of fAD. Use the f1 clock as the PLL clock or the main clock.

For ϕ AD, set the periods to not more than twice as long as that of the timer count source used in A/D trigger mode. Table 3.1 shows the Possible Combinations.

Table 3.1 Possible Combinations

fAD	ϕ AD	Clock Prior to Timer B Division	Timer B Count Source
f1	f1 divided by 4	f1	f2TIMAB
	f1 divided by 6		
	f1 divided by 12		

This section describes the different timer B and A/D converter combinations.

3.1 Periodic Sampling

This section describes the method for performing constant A/D conversion every cycle.

Select timer B_j as the timer mode and as the A/D_i conversion start trigger (j = 0 to 2; i = no value, 1).

A/D_i conversion starts every time timer B_j underflows.

Figure 3.1 shows Periodic Sampling.

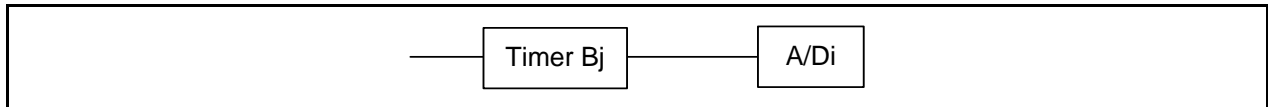


Figure 3.1 Periodic Sampling

3.2 Two-channel Simultaneous Sampling

When two channels are sampled simultaneously, select the same timer (timer B₀, B₁, or B₂) as the start trigger for A/D and A/D₁ conversion. A/D and A/D₁ start A/D conversion simultaneously when timer B_j underflows.

Figure 3.2 shows Two-channel Simultaneous Sampling.

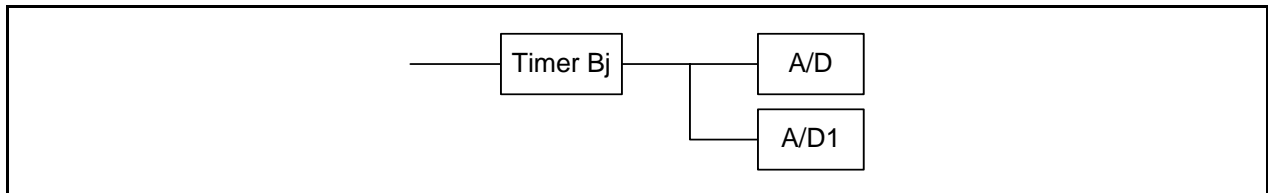


Figure 3.2 Two-channel Simultaneous Sampling

3.3 Delayed Sampling

Set both the TB₀EN bit and TB₁EN bit in the TB₂SC register to 1 (A/D trigger mode).

Timers B₀ and B₁ operate as one-shot timers. Timer B₂ underflow is the trigger to start A/D conversion for timers B₀ and B₁.

Set the sampling period in the TB₂ register.

Timers B₀ and B₁ start counting every time timer B₂ underflows.

When timer B₂ underflows, A/D conversion starts and timer B₀ stops counting.

When timer B₁ underflows, A/D₁ conversion starts and timer B₁ stops counting.

Figure 3.3 shows Delayed Sampling.

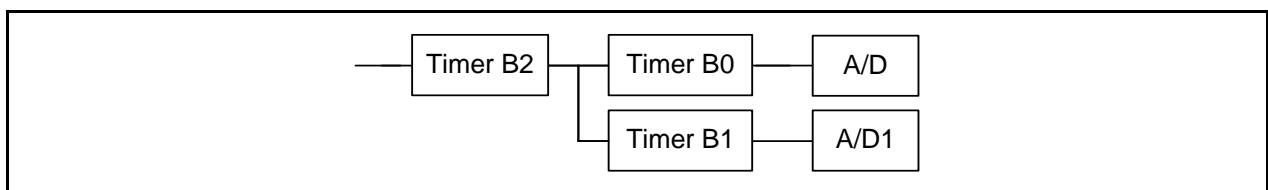


Figure 3.3 Delayed Sampling

4. Application Example

This section describes an application example to achieve the delayed sampling described in section 3.3.

- (1) Set timer B0 as the A/D start delay time, timer B1 as the A/D1 start delay time, and timer B2 as the sampling period. Start the counts for timers B0, B1, and B2.
- (2) Timers B0 and B1 start counting when timer B2 underflows.
- (3) A/D conversion starts when timer B0 underflows and timer B0 stops counting.
- (4) A/D1 conversion starts when timer B1 underflows and timer B1 stops counting.

Figure 4.1 shows the Connection Example.

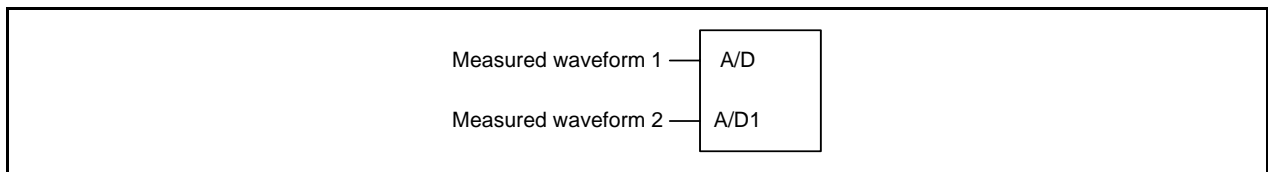


Figure 4.1 Connection Example

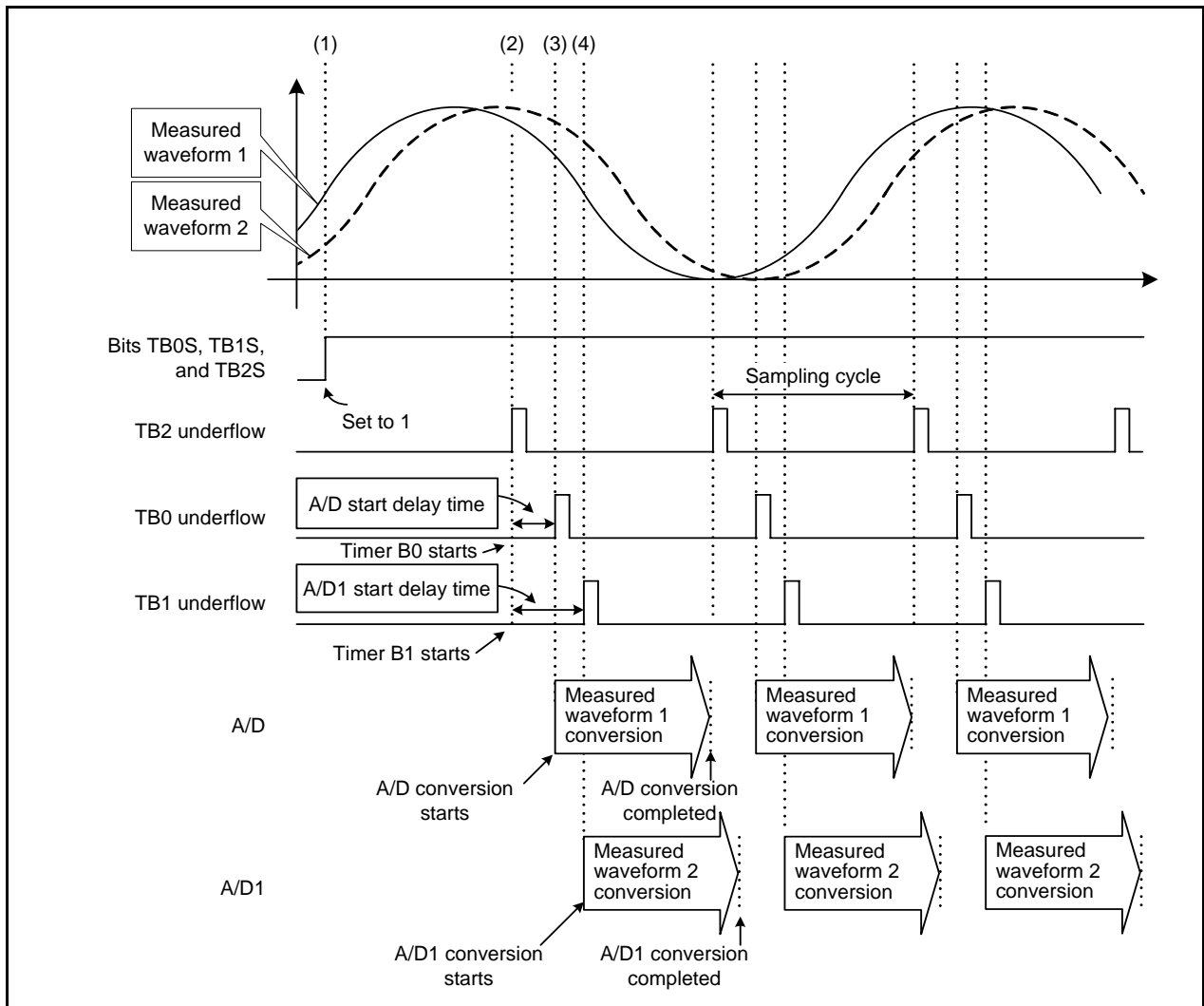


Figure 4.2 Operation Example

5. Setting Procedure

This section describes the procedure and values necessary for running the application example.

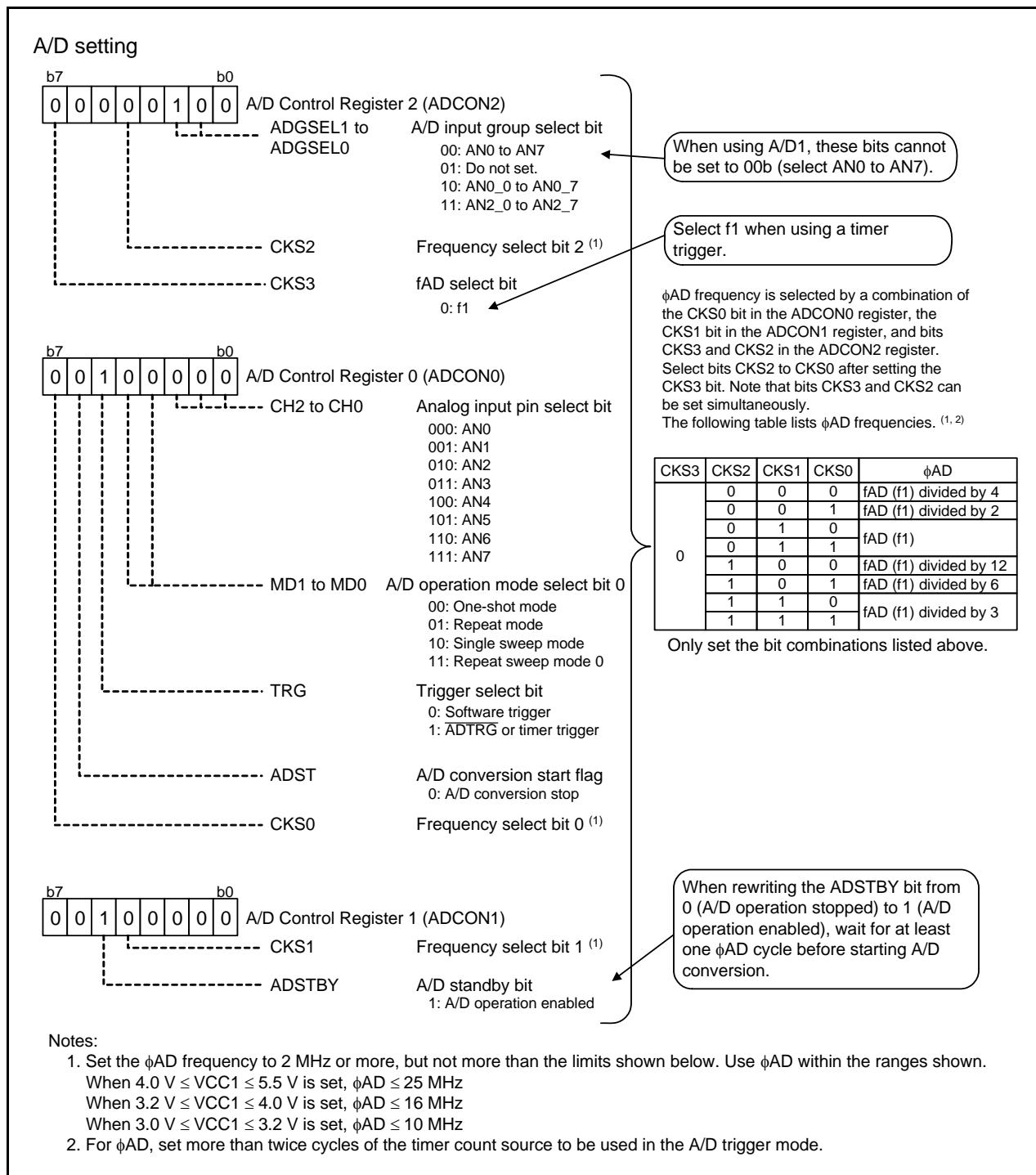


Figure 5.1 Setting Procedure (1/7)

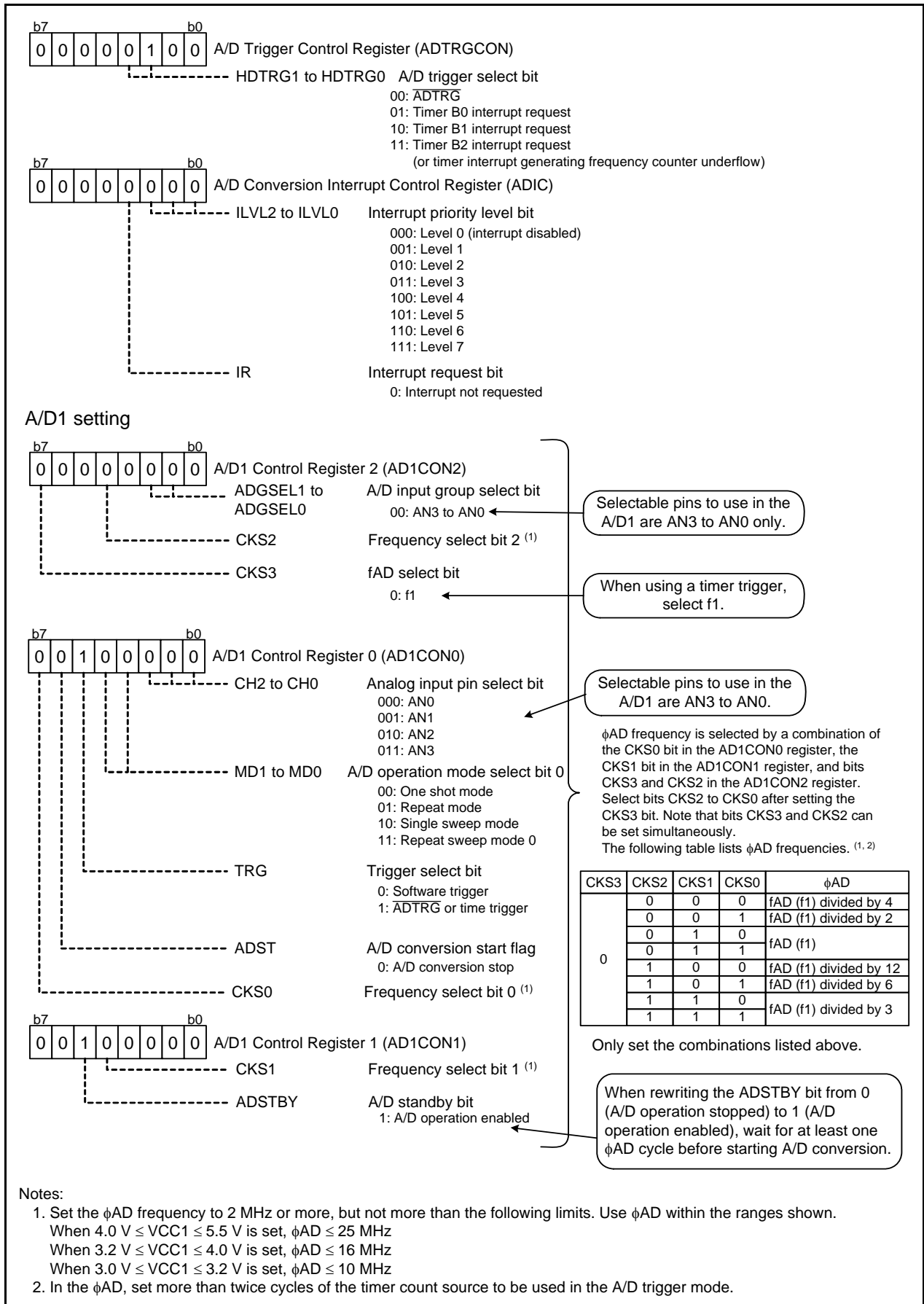


Figure 5.2 Setting Procedure (2/7)

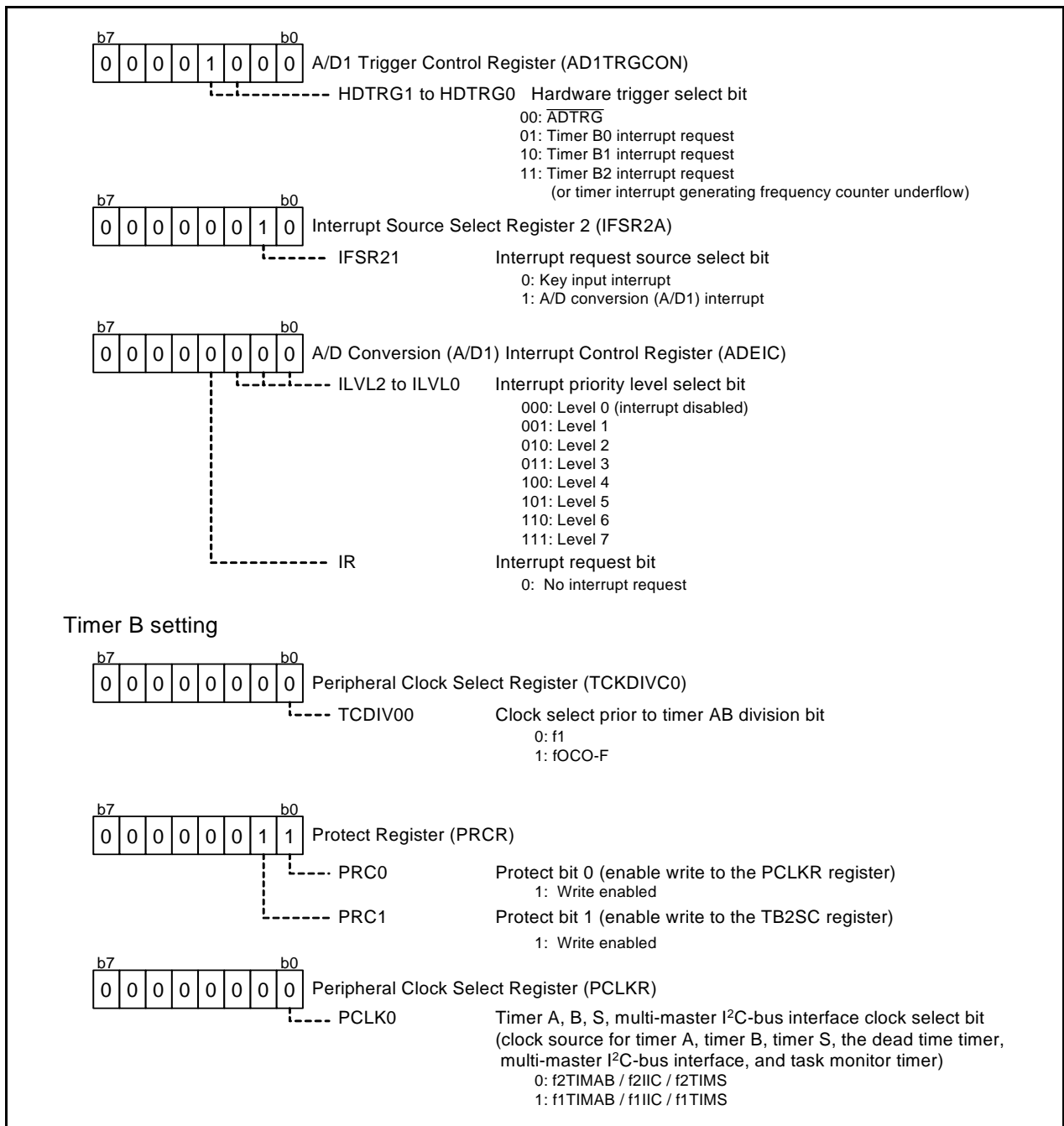


Figure 5.3 Setting Procedure (3/7)

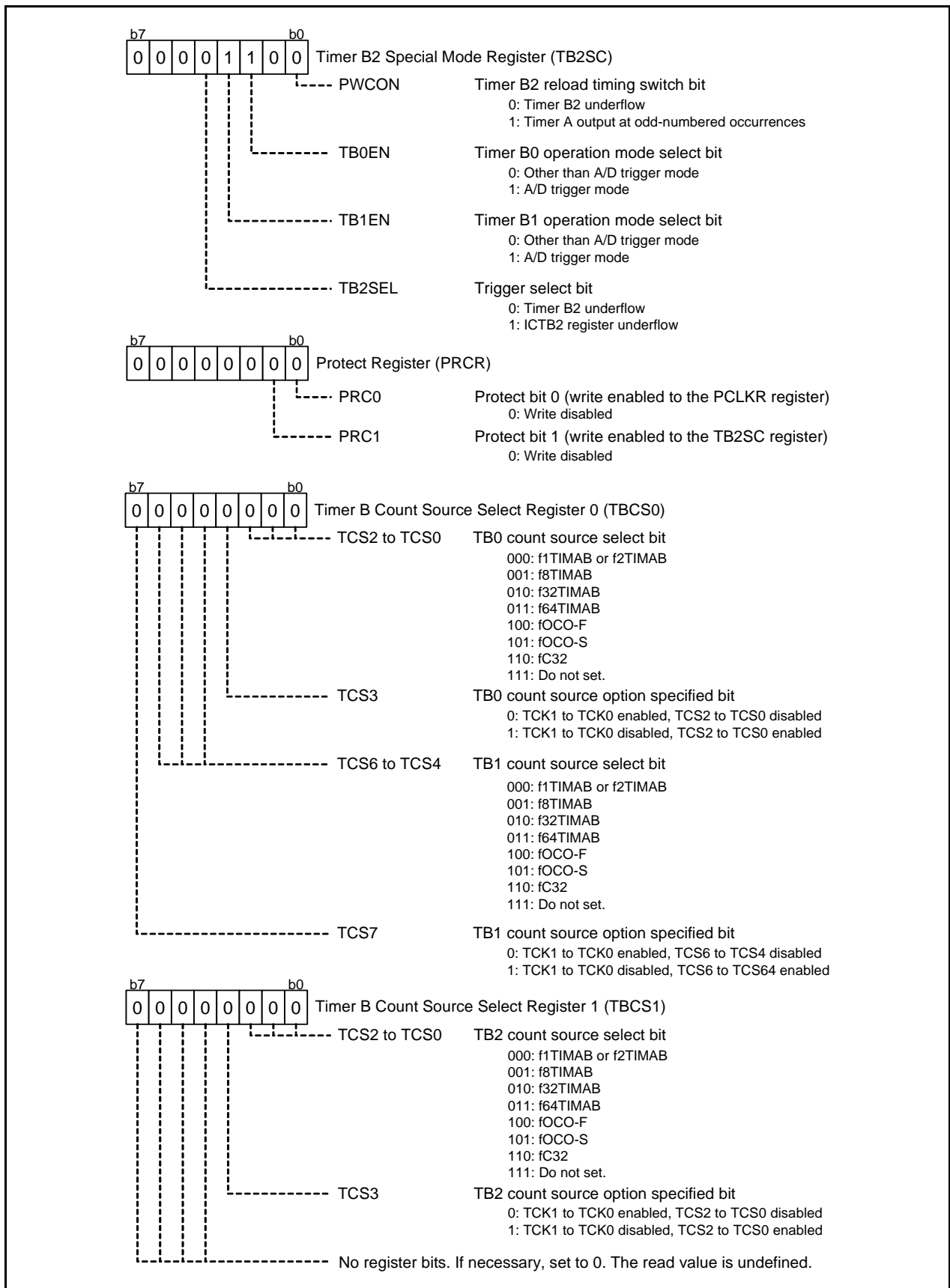


Figure 5.4 Setting Procedure (4/7)

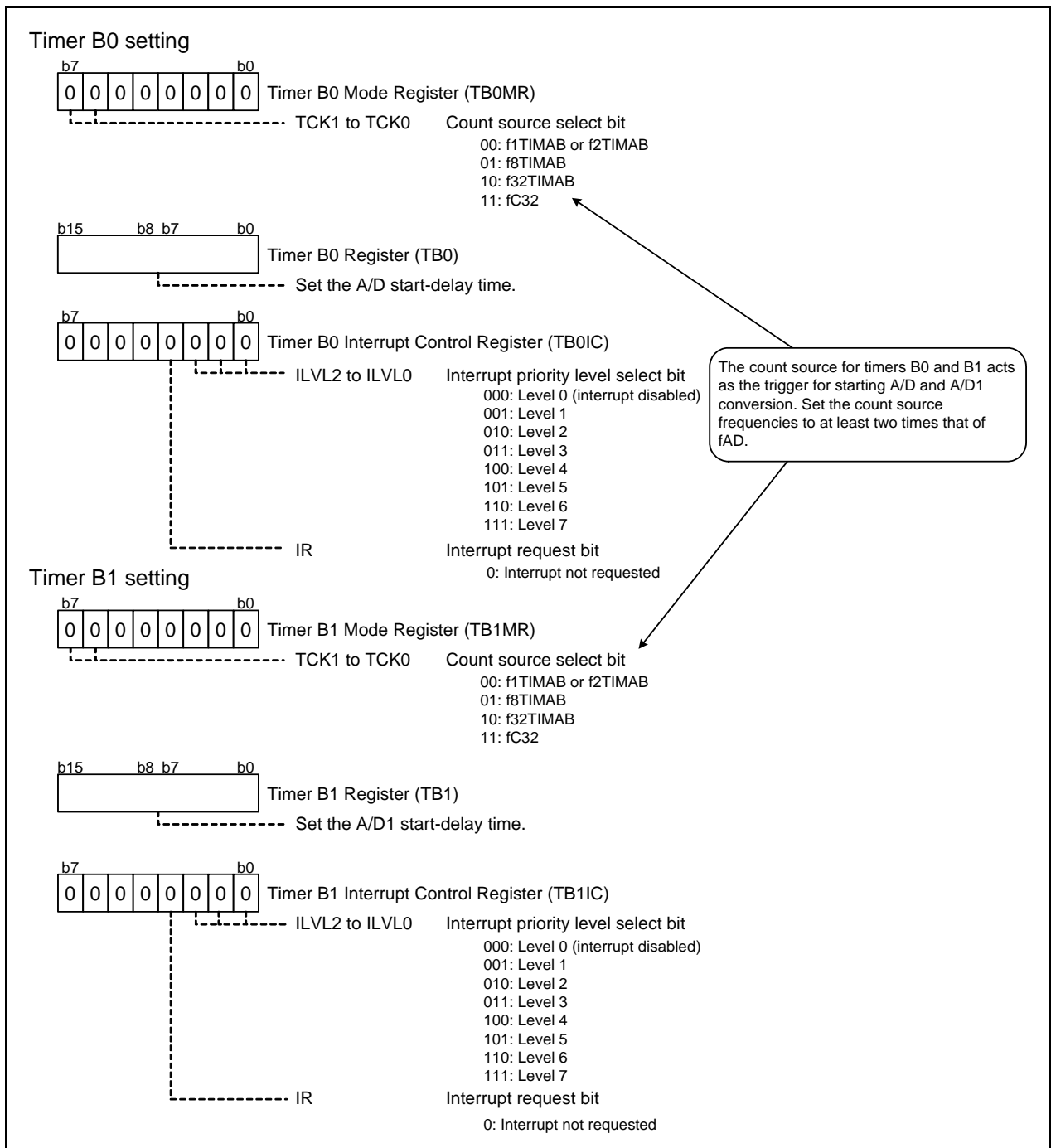


Figure 5.5 Setting Procedure (5/7)

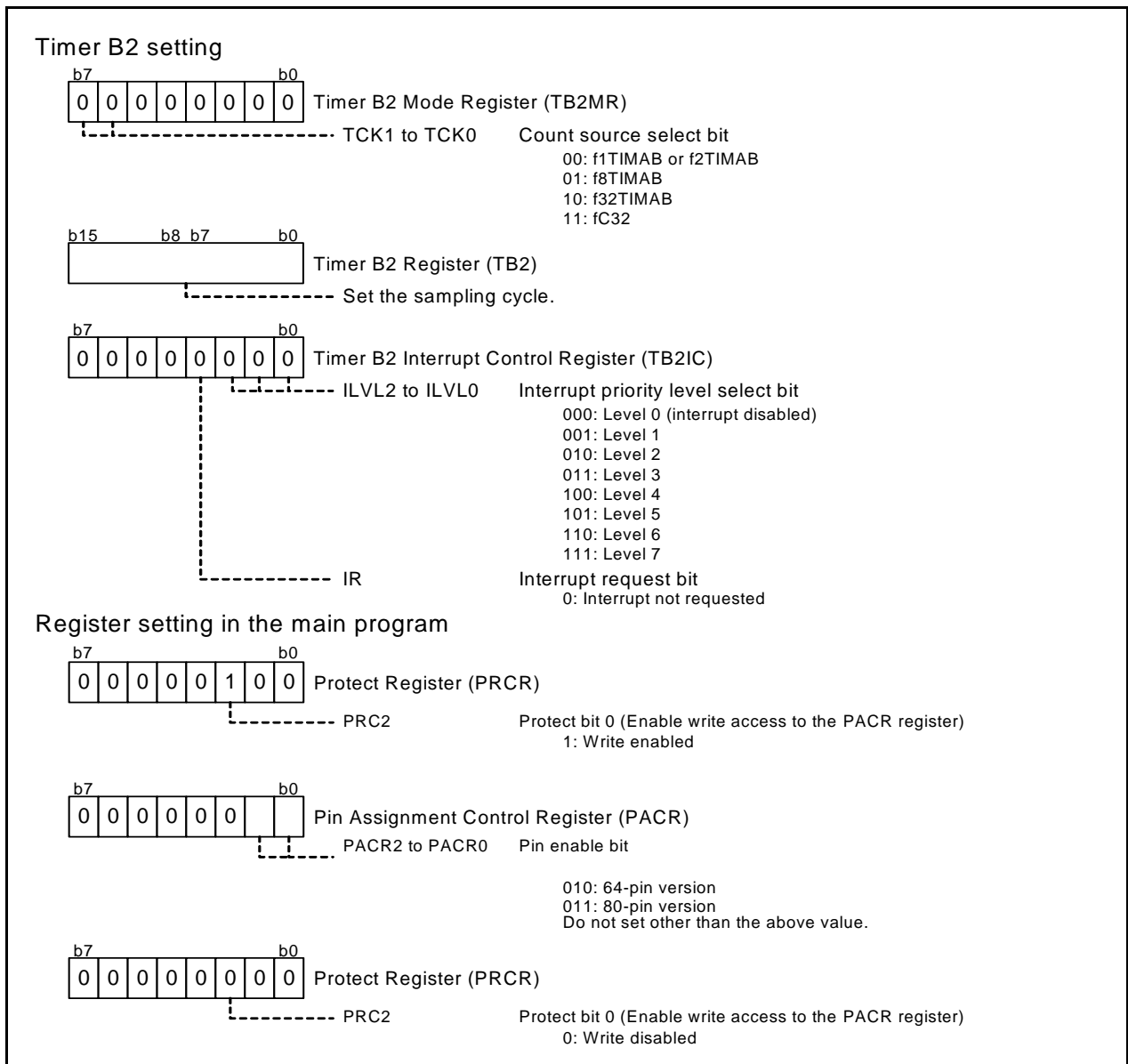


Figure 5.6 Setting Procedure (6/7)

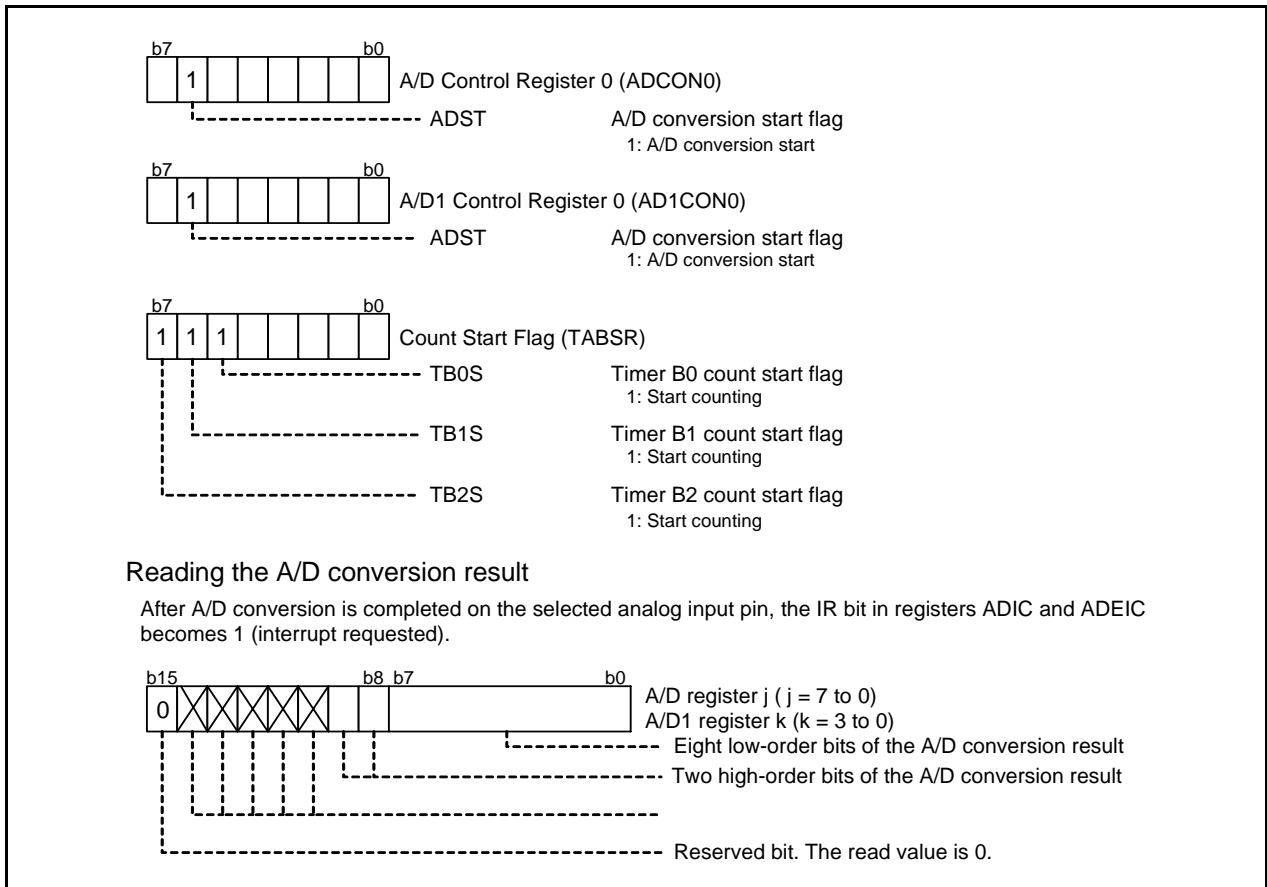


Figure 5.7 Setting Procedure (7/7)

6. Sample Program

A sample program can be downloaded from the Renesas Technology website.

To download, click “Application Notes” in the left-hand side menu of the M16C Family page.

7. Reference Documents

Hardware Manuals

M16C/5LD Group Hardware Manual

M16C/56D Group Hardware Manual

The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual

C compiler package V.5.45 for M16C Series and R8C Family.

C compiler user’s Manual Rev.1.00.

The latest information can be downloaded from the Renesas Technology website

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REVISION HISTORY	M16C/5LD and 56D Groups A/D Conversion Using Timer B
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Rev.	Date	Description	
		Page	Summary
1.00	Nov 30, 2009	-	First Edition issued

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