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Renesas Electronics Corporation

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H8SX Series

A/D Conversion Using Scan Mode

Introduction

As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

This H8SX series Application Note provides information you may be need during software and hardware design. This is a basic edition that provides operation examples that each use a single H8SX series on-chip peripheral function.

Although the operation of each program, circuit, and other aspects covered by this application note has been checked, make sure that you conduct your own operation checks before actually using the H8SX series.

Contents

1. Overview

Four-channel voltage data is input to the H8SX series as shown in Figure 1. The A/D conversion result is then stored into RAM. The A/D converter is started by an external trigger.

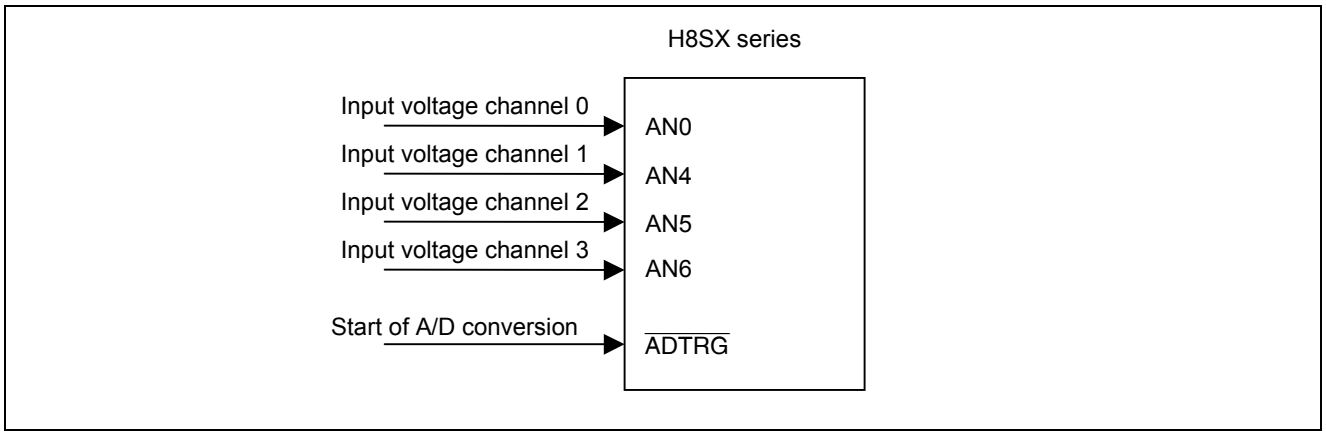


Figure 1 Block Diagram of Voltage Measurement Using the H8SX Series

2. Configuration

Figure 2 is a block diagram of four-channel A/D conversion.

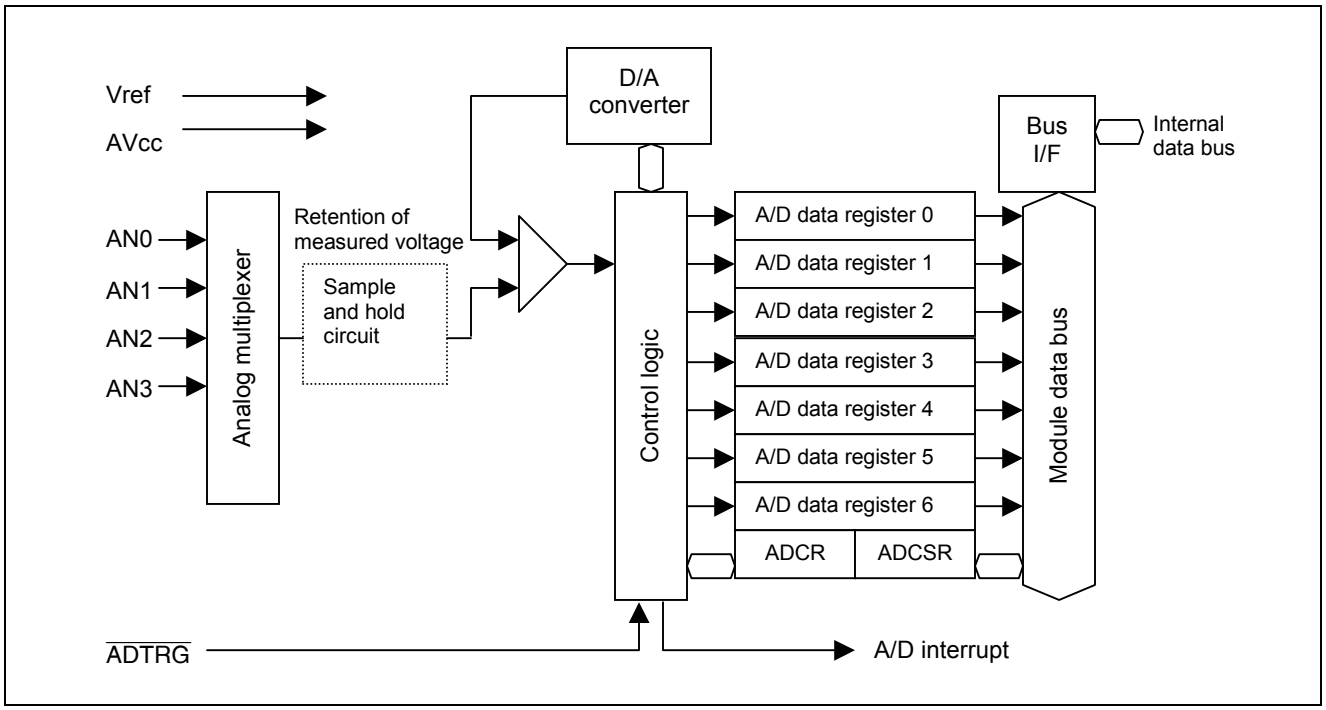


Figure 2 Block Diagram of A/D Converter

Table 1 lists the function allocations for this sample task. The H8SX series functions are allocated and A/D conversion is performed.

Table 1 Function Allocation for H8SX Series

H8SX series function	Function
ADCSR	Selects A/D conversion channels (group) and displays the status.
ADCR	Selects the start trigger signal and sets the operating mode (scan).
ADDRA to ADDRG	Stores the A/D conversion result.
ADTRG	A/D external trigger input pin

Figure 3 shows the description of operation. As shown in Figure 3, external trigger ADTRG starts the A/D converter which repeats A/D conversion for channels AN0 and AN4 to AN6 (four channels). The ADST bit is set to 1 until it is cleared to 0 by software. While this bit remains set to 1, A/D conversion of the selected input channels is repeated. In this task, buffer operation (consisting of four stages) is used. The A/D conversion result in ADDRA to ADDRG is stored in 140 bytes of RAM between SCN0 and SCN6.

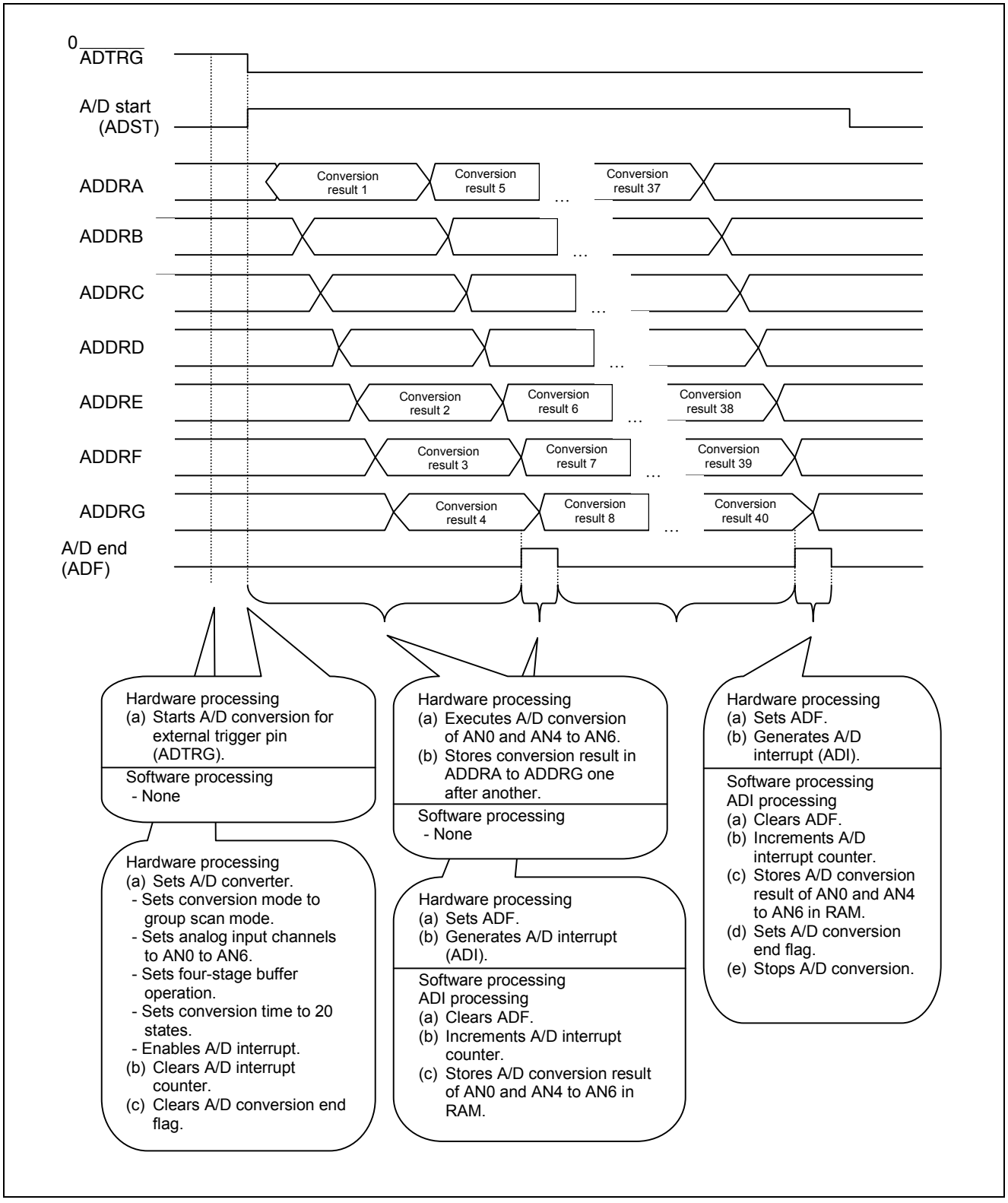


Figure 3 Description of A/D Conversion Using Scan Mode

3. Sample Program

3.1 Function

This program performs an A/D conversion of analog voltage captured in four-channel scan mode.

The program uses external trigger pin to turn A/D conversion on or off. It generates an interrupt at the end of A/D conversion and obtains the A/D-converted value. This sample program obtains each channel ten times.

3.2 Function Specifications

```
void ad_scan(void);
```

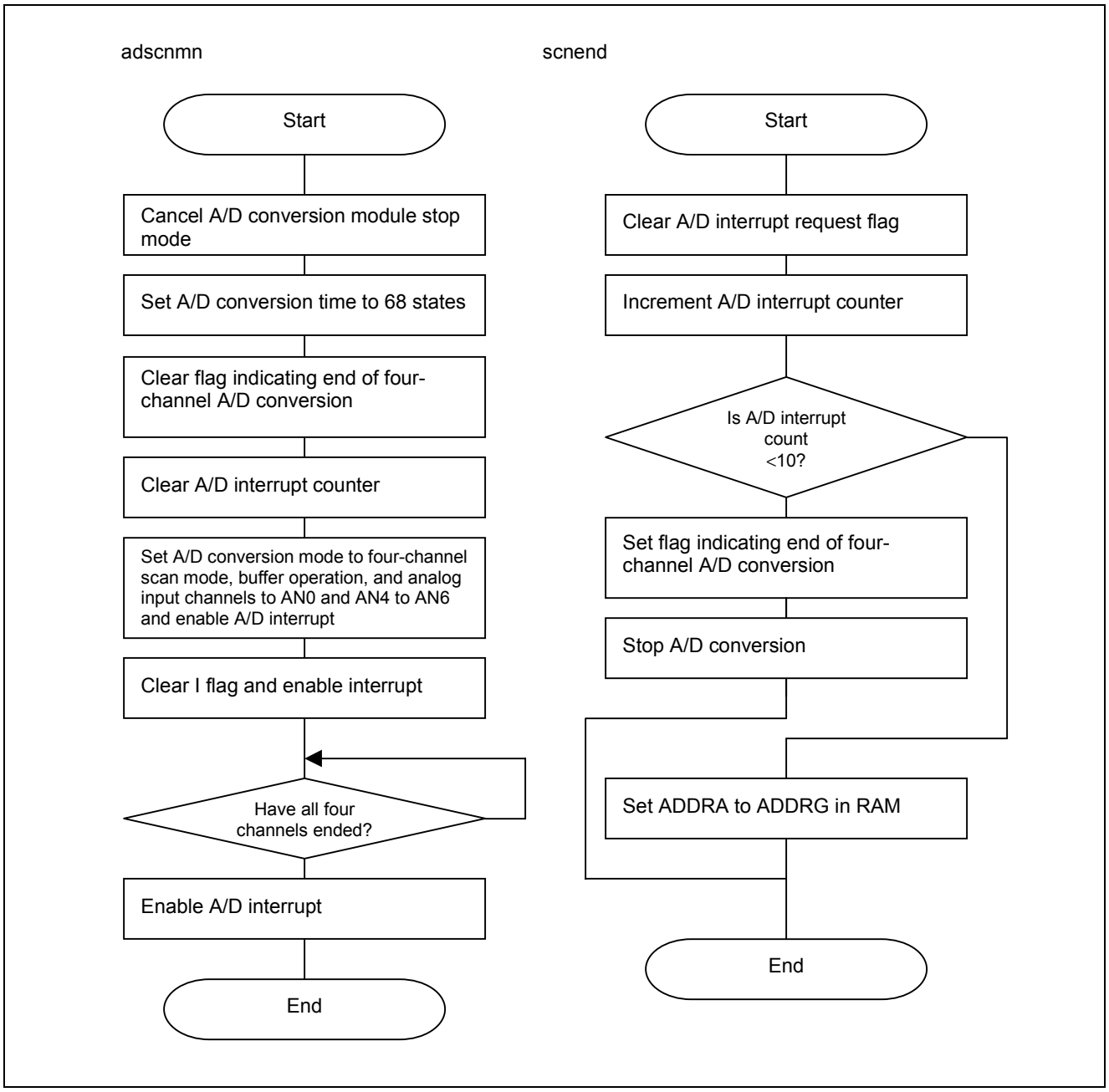
Argument	Description
None	—

Return value	Description
None	—

Example)

```
extern void  ad_scan( void );
void  main( void )                  // Main routine
{
   ad_scan();                       // Starts A/D conversion.
   while(1) ;
}
```

3.3 Flowchart



3.4 Program Listing

```
/************************************************************/
/* Include File                                             */
/************************************************************/
#include <machine.h>
#include "iodefine.h"

/************************************************************/
/* Function Prototype                                       */
/************************************************************/
void ad_scan(void);

/************************************************************/
/* RAM Allocation                                           */
/************************************************************/
static unsigned short scn[7];   // Result Of A/D Conversion
static unsigned char  scn_cnt;  // Work
static unsigned char  scn_endf; // A/D Conversion End Flag
static unsigned char  adi_cnt;
/************************************************************/
/* Function Definition(Main Program)                        */
/************************************************************/
void ad_scan(void)
{
   P_MSTPCRA.WORD = 0xFFF7;    // disable module stop mode

   scn_endf      = 0;          // A/D Conversion End Flag Clear
   scn_cnt       = 0;          // Work Clear
   adi_cnt       = 0;
   P_P1.DDR      = 0;
   P_P1.ICR.BIT.B3 = 1;
   P_AD.CR.BYTE  = 0xF0;       // Initialize CR
   P_AD.CSR.BYTE = 0x46;       // Initialize CSR
   set_imask_ccr(0);           // Enable Interrupt
   while(scn_endf==0);         // Check Conversion End
}

/************************************************************/
/* Function Definition(Interrupt Handler)                   */
/************************************************************/
#pragma interrupt (inthdr_adscan)
void inthdr_adscan(void)        // Conversion Interrupt Handler
{
   P_AD.CSR.BIT.ADF = 0;        // Clear ADF
   if(adi_cnt < 10)             // 10 Count
   {
       scn[scn_cnt++]=P_AD.DRA.BYTE;
       scn[scn_cnt++]=P_AD.DRB.BYTE;
       scn[scn_cnt++]=P_AD.DRC.BYTE;
       scn[scn_cnt++]=P_AD.DRD.BYTE;
       scn[scn_cnt++]=P_AD.DRE.BYTE;
       scn[scn_cnt++]=P_AD.DRF.BYTE;
```

```
        scn[scn_cnt++]=P_AD.DRG.BYTE;
        adi_cnt += 1;           // Counter Up
    }
    else                        // Under 10 Count
    {
        scn_endf = 1;           // Set Conversion End Flag
        P_AD.CSR.BIT.ADST = 0;  // ADST Clear
    }
}
```

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sept.19.03	—	First edition issued

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