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H8SX Family

A/D Conversion in Scan Mode

Introduction

A/D conversion is performed for voltage inputs on four channels, and the results are stored in RAM. A/D conversion is initiated by an external trigger.

Target Device

H8SX/1582F

Contents

1. Specifications 2
2. Conditions for Application 3
3. Description of Modules Used 4
4. Description of Operation 5
5. Description of Software 7

1. Specifications

- A/D conversion in scan mode is shown in figure 1.
- The voltage inputs on four channels are subjected to A/D conversion and the results are stored in RAM.
- A/D conversion is initiated by an external trigger.

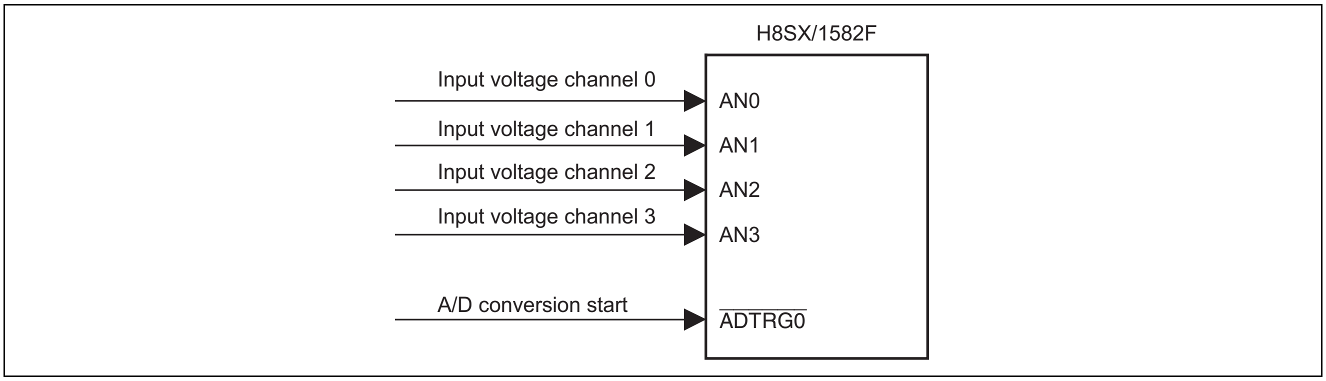


Figure 1 A/D Conversion in Scan Mode

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents
Operating frequency	Input clock: 5 MHz System clock (Iϕ): 40 MHz Peripheral module clock (Pϕ): 20 MHz External bus clock (Bϕ): 20 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)
Development tool	High-performance Embedded Workshop Version 4.00.02
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.00 (from Renesas Technology Corp.)
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF9000	B	Uninitialized data area (RAM area)

3. Description of Modules Used

Figure 2 shows a block diagram of A/D conversion for four channels. In this sample task, the following features of the A/D converter are used.

- To automatically perform A/D conversion for four channels (AN0 to AN3) without using software (scan mode)
- To start A/D conversion by means of the external trigger pin ($\overline{\text{ADTRG0}}$)
- To generate an interrupt when A/D conversion has finished

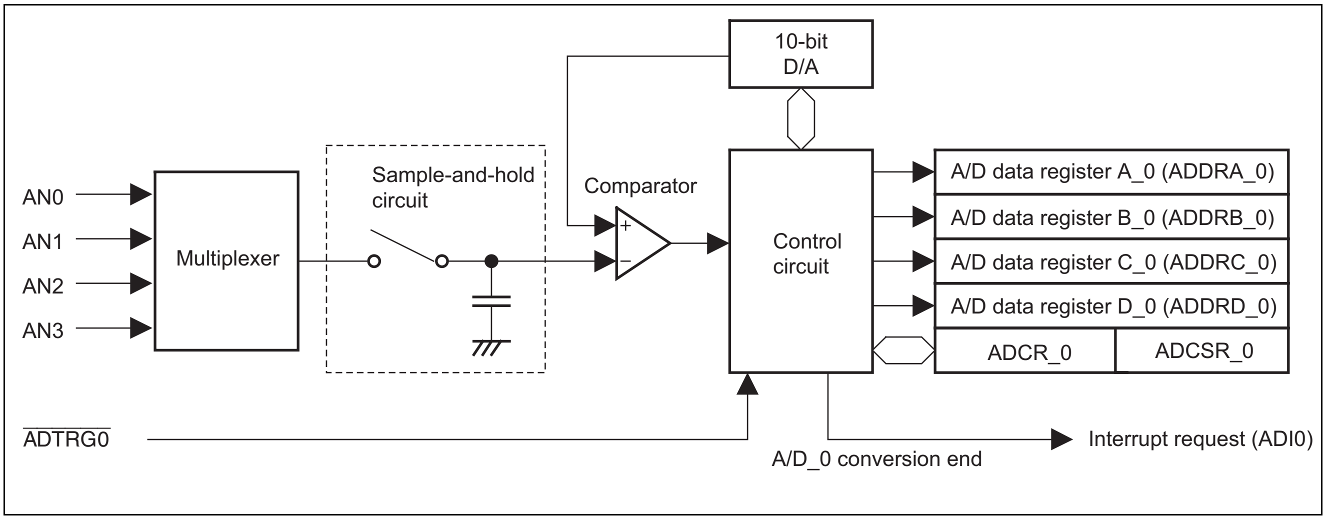


Figure 2 Block Diagram of A/D Converter

4. Description of Operation

4.1 Overview of Operation

Figure 3 illustrates an example of operation in scan mode. The hardware processing and software processing are shown in table 3 for describing figure 3.

- The A/D converter is activated by the external trigger $\overline{\text{ADTRG0}}$ and A/D conversion is performed repeatedly for the four channels of AN0 to AN3.
- The ADST bit stays 1 until it is cleared to 0 by software, and A/D conversion is repeated for the selected input channels during this period.
- The A/D-converted results stored in ADDRA to ADDRD are stored in RAM (array scn[]).

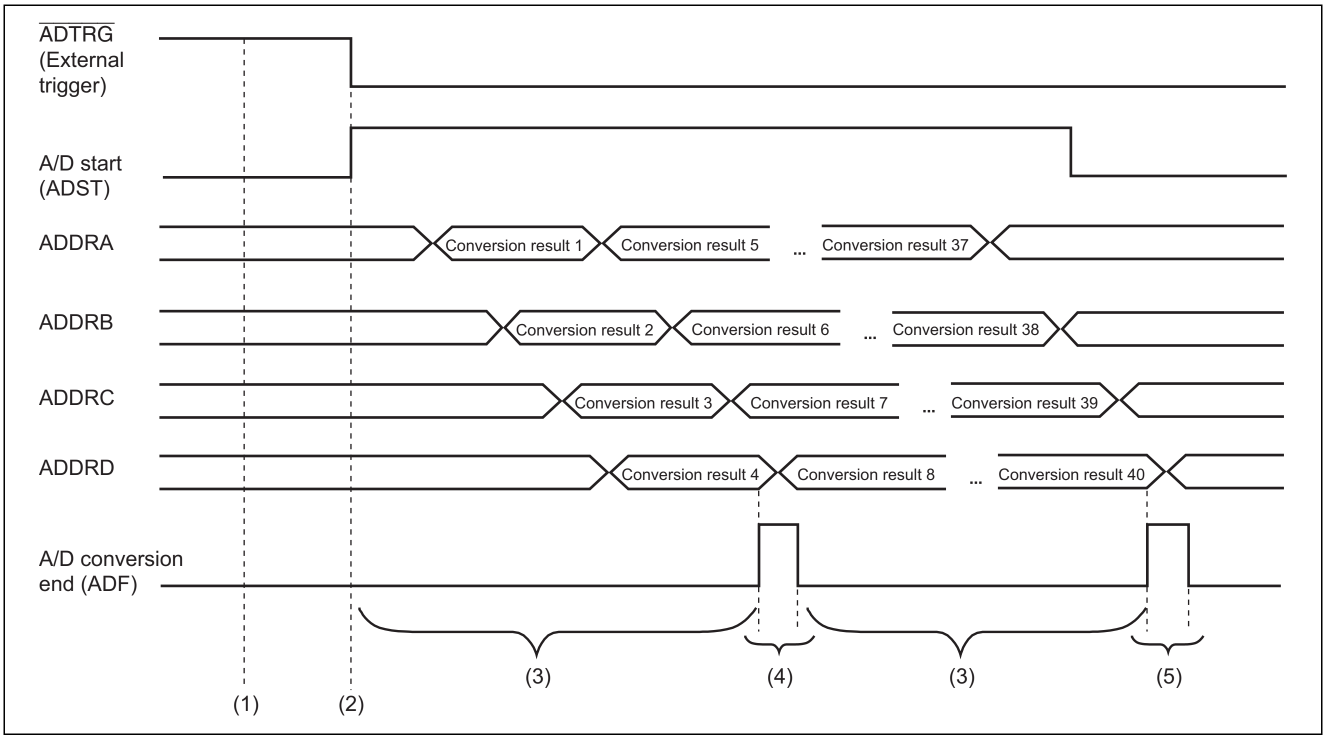


Figure 3 Principles of A/D Conversion in Scan Mode

Table 3 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	None	(a) Set up the A/D converter. • Set the conversion mode as scan mode. • Select analog input channels AN0 to AN3. • Set the conversion time as 256 cycles. • Enable the ADI interrupt. (b) Clear the ADI interrupt counter.
(2)	(a) Start A/D conversion by the external trigger pin ($\overline{\text{ADTRG}}$.)	None
(3)	(a) Perform A/D conversion for AN0 to AN3. (b) Store the A/D-converted results in ADDRA to ADDRD sequentially.	None
(4)	(a) Set the ADF bit (A/D conversion end flag). (b) Generate an ADI interrupt.	ADI0 interrupt processing (a) Clear the ADF bit. (b) Store the A/D-converted results for AN0 to AN3 in RAM. (c) Increment the ADI interrupt counter.
(5)	(a) Set the ADF bit. (b) Generate an ADI interrupt.	ADI0 interrupt processing (a) Clear the ADF bit. (b) Store the A/D-converted results for AN0 to AN3 in RAM. (c) Increment the ADI interrupt counter. (d) Stop A/D conversion.

5. Description of Software

5.1 List of Functions

The functions of this sample task are listed in table 4.

Table 4 List of Functions

Function Name	Functions
init	Initialization routine Cancels module stop mode, sets the clocks, and calls the main function.
main	Main routine Makes settings for A/D conversion.
adi_int	ADI0 interrupt processing Stores the A/D-converted results for 4 channels × 10 times in RAM.

5.2 Vector Table

The interrupt exception handling vector table of this sample task is shown in table 5.

Table 5 Interrupt Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	init
ADI0	86	H'000158	adi_int

5.3 RAM Usage

Table 6 RAM Usage

Label Name	Description	Memory Size	Used In
scn[4][10]	Stores the A/D-converted results for four channels.	80 bytes	adi_int
adicnt	ADI interrupt counter Counts the number of times an ADI interrupt has occurred.	1 byte	main, adi_int

5.4 Description of Functions

5.4.1 init Function

(1) Functional overview

Initialization routine which cancels module stop mode, sets the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the system clock frequency. The CPU, DMAC, and DTC modules are driven by the system clock.
8	ICK0	0	R/W	000: Input clock × 8
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 4
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC are the registers that control module stop mode. Setting the bits in these registers places the corresponding modules in module stop mode, and clearing the bits cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
4	MSTPA4	1	R/W	A/D converter (unit 1)
3	MSTPA3	0	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

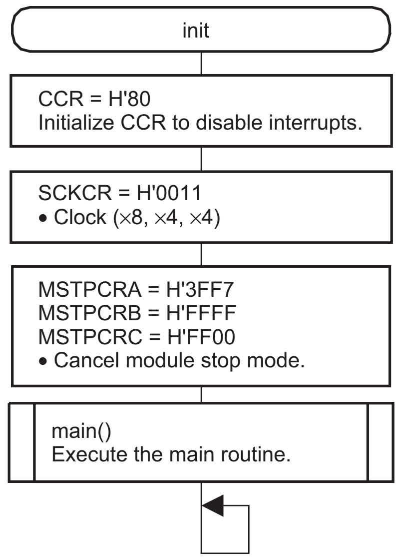
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communication interface_3 (SCI_3)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
10	MSTPC10	1	R/W	Synchronous serial communication unit 2 (SSU_2)
9	MSTPC9	1	R/W	Synchronous serial communication unit 1 (SSU_1)
8	MSTPC8	1	R/W	Synchronous serial communication unit 0 (SSU_0)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF9000 to H'FFBFFF)
0	MSTPC0	0	R/W	Always write the same value to the MSTPC1 and MSTPC0 bits.

(5) Flowchart



5.4.2 main Function

(1) Functional overview

Main routine which makes settings for A/D conversion.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- A/D control/status register_0 (ADCSR_0) Address: H'FFFFA0

Bit	Bit Name	Setting	R/W	Function
7	ADF	0	R/W	A/D Conversion End Flag 0: A/D conversion is in progress 1: A/D conversion has ended
6	ADIE	1	R/W	A/D Interrupt Enable 0: ADI interrupt is disabled 1: ADI interrupt is enabled
5	ADST	0	R/W	A/D Start 0: A/D conversion is stopped 1: A/D conversion is started
3	CH3	0	R/W	Channel Select
2	CH2	0	R/W	When SCANE and SCANS bits in ADCR = B'10,
1	CH1	1	R/W	0011: Analog input channels AN0 to AN3 are selected
0	CH0	1	R/W	

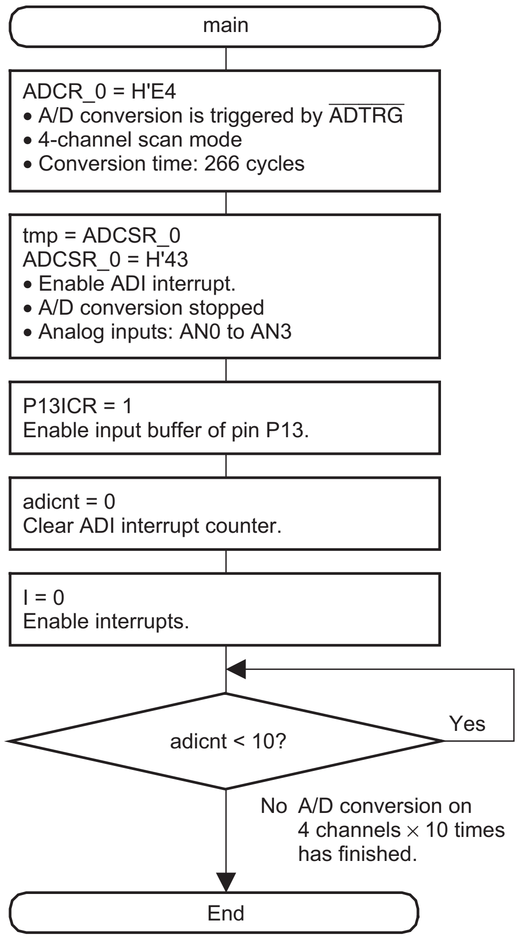
- A/D control register_0 (ADCR_0) Address: H'FFFFA1

Bit	Bit Name	Setting	R/W	Function
7	TRGS1	1	R/W	Timer Trigger Select 1, 0
6	TRGS0	1	R/W	11: A/D conversion is triggered by $\overline{\text{ADTRG}}$.
5	SCANE	1	R/W	Scan Mode
4	SCANS	0	R/W	10: Scan mode. A/D conversion is consecutively performed for one to four channels.
3	CKS1	0	R/W	Clock Select 1, 0
2	CKS0	1	R/W	01: A/D conversion time is 266 cycles (max.)

- Port 1 input buffer control register (P1ICR) Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Function
3	P13ICR	1	R/W	0: Input buffer of pin P13 is disabled 1: Input buffer of pin P13 is enabled

(5) Flowchart


main
ADCR_0 = H'E4
• A/D conversion is triggered by ADTRG
• 4-channel scan mode
• Conversion time: 266 cycles
tmp = ADCSR_0
ADCSR_0 = H'43
• Enable ADI interrupt.
• A/D conversion stopped
• Analog inputs: AN0 to AN3
P13ICR = 1
Enable input buffer of pin P13.
adicnt = 0
Clear ADI interrupt counter.
I = 0
Enable interrupts.
adicnt < 10?
Yes
No
A/D conversion on 4 channels × 10 times has finished.
End

5.4.3 adi_int Function

(1) Functional overview

ADI0 interrupt processing that stores the A/D-converted results for 4 channels × 10 times in RAM.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- A/D data registers A_0 to D_0 (ADDRA_0 to ADDRD_0) Address: H'FFFF90 to H'FFFF96
  ADDR are 16-bit read-only registers that store the results of A/D conversion. There are eight registers, ADDRA to ADDRH. Table 7 shows which ADDR stores the conversion result for each analog input channel.
  The 10-bit converted data is stored in bits 15 to 6 of ADDR, and the lower six bits will always be read as 0.
  The data bus between the CPU and ADDR is 16 bits and ADDR can be directly read by the CPU. ADDR must be accessed in 16-bit units. Access in 8-bit units is not allowed.

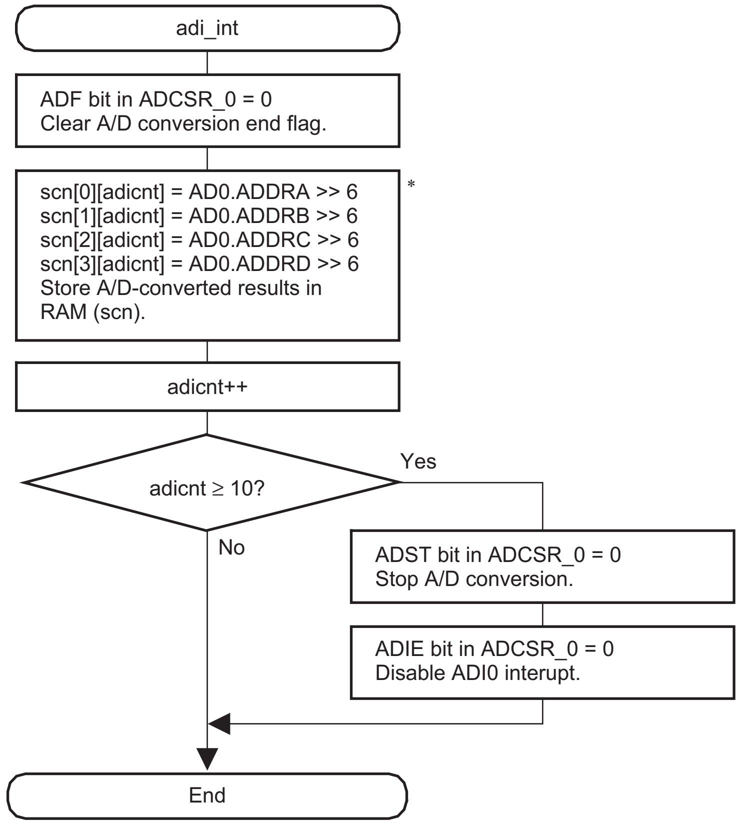
Table 7 Correspondence between Analog Input Channel and ADDR

Analog Input Channel	A/D Data Register Containing Conversion Result
AN0	ADDRA
AN1	ADDRB
AN2	ADDRC
AN3	ADDRD

- A/D control/status register_0 (ADCSR_0) Address: H'FFFFA0

Bit	Bit Name	Setting	R/W	Function
7	ADF	0	R/W	A/D End Flag 0: A/D conversion is in progress 1: A/D conversion has ended
6	ADIE	0	R/W	A/D Interrupt Enable 0: ADI interrupt is disabled 1: ADI interrupt is enabled
5	ADST	0	R/W	A/D Start 0: A/D conversion is stopped 1: A/D conversion is started

(5) Flowchart



Note: * The results of A/D conversion are stored in the upper 10 bits of ADDRA_0 to ADDRD_0. In this sample task, ADDRA_0 to ADDRD_0 are shifted six bits to the right and stored in RAM (scn).

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.10.06	—	First edition issued