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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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1. **Abstract**

In one-shot mode, the A/D converter performs a single A/D conversion on the input voltage of one pin from the following: AN_0 to AN_7, AN15_0 to AN15_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, or ANEX1.

2. **Introduction**

The application described in this document applies to the following MCU:

- MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.
3. **Application Example**

This section describes how to perform an A/D conversion on the input voltage of the AN_i pin (i = 0 to 7). The following conditions are necessary to perform conversion:

- Operation clock (\(\phi_{AD}\)): \(f_{AD}\) divided-by-2
- Resolution: 10-bit
- A/D conversion start condition: Software trigger
- Sample and hold function: Enabled
- DMAC operation mode: Disabled

3.1 **Explanation**

(1) After setting the ADST bit in the AD0CON0 register to 1 (A/D conversion started), the A/D converter starts the conversion.

(2) When conversion on the AN_i pin is complete, the value from the successive approximation register (conversion results) is transferred to the AD0i register (i = 0 to 7). At the same time, the IR bit in the AD0IC register becomes 1 (interrupt requested). Then, the ADST bit in the AD0CON0 register becomes 0 (A/D conversion stopped), and the A/D conversion stops.

The diagram below shows operation timing.

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**Figure 3.1 Operation in One-shot Mode**

- (1) A/D conversion started
- (2) A/D conversion completed
- 33 cycles (1)
- The signal becomes low when an interrupt request is accepted, or by setting this bit to 0.

i = 0 to 7

**Note:**
1. Number of cycles at 10-bit resolution with sample and hold function.
   Other cycle amounts are as follows:
   a) 59 cycles at 10-bit resolution with no sample and hold function
   b) 28 cycles at 8-bit resolution with sample and hold function
   c) 49 cycles at 8-bit resolution with no sample and hold function
3.2 Setting

This section shows the procedures and values to set the example in section 3.1 “Explanation”. Refer to individual MCU hardware manuals for details on individual registers.

(1) Set the A/D0 control register 0.

A/D0 Control Register 0 (AD0CON0)

- CH2 to CH0: Analog Input Pin Select Bit
  - 000b: AN_0
  - 001b: AN_1
  - 010b: AN_2
  - 011b: AN_3
  - 100b: AN_4
  - 101b: AN_5
  - 110b: AN_6
  - 111b: AN_7

- MD1 to MD0: A/D Operation Mode Select Bit 0
  - 00b: One-shot mode

- TRG: Trigger Select Bit
  - 0: Software trigger
  - 1: A/D conversion stopped

- ADST: A/D Conversion Start Bit
  - 0: A/D conversion stopped

- CKS0: Frequency Select Bit

Use the following bits to select the A/D converter operation clock (fAD):
- CKS0 bit in the AD0CON0 register
- CKS1 bit in the AD0CON1 register
- CKS2 bit in the AD0CON3 register

<table>
<thead>
<tr>
<th>CKS2</th>
<th>CKS1</th>
<th>CKS0</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>fAD divided-by-4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>fAD divided-by-3</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>fAD divided-by-2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>fAD</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>fAD divided-by-8</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>fAD divided-by-6</td>
</tr>
</tbody>
</table>

Only set the combinations listed above. When VCC is 5 V, set the fAD frequency to 16 MHz or less. When VCC is 3.3 V, set the fAD frequency to 10 MHz or less.

Continued on next page
(2) Set the A/D control register 1.

(A/D0 Control Register 1 (AD0CON1))

- SCAN1 to SCAN0: A/D Sweep Pin Select Bit
  - Disabled in one-shot mode. Set to 00b.
- MD2: A/D Operation Mode Select Bit 1
  - 0: Any mode other than repeat sweep mode 1.
- BITS: 8-/10-bit Mode Select Bit
  - 1: 10-bit mode
- CKS1: Frequency Select Bit
  - VREF Connect Bit
  - 1: VREF connected
- OPA1 to OPA0: External Operational Amplifier Connect Mode Bit
  - 00b: ANEX0 and ANEX1 not used

When rewriting this bit from 0 to 1, wait 1 μs before starting A/D conversion.

(3) Set the A/D control register 2.

(A/D0 Control Register 2 (AD0CON2))

- SMP: A/D Conversion Method Select Bit
  - 1: With sample and hold function
- APS1 to APS0: Analog Input Port Select Bit
  - 00b: AN_0 to AN_7, ANEX0, and ANEX1
- TRG0: External Trigger Source Select Bit
  - 0: ADTRG selected

Set to 0.

(4) Set the A/D control register 3.

(A/D0 Control Register 3 (AD0CON3))

- DUS: DMAC Operating Mode Select Bit
  - 0: DMAC operating mode disabled
- MSS: Multi-port Sweep Mode Select Bit
  - 0: Multi-port sweep port disabled
- CKS2: Frequency Select Bit
- MSF1 to MSF0: Multi-port Sweep Status Flag
  - Set to 0.

Continued on next page
(5) Set the A/D control register 4.

A/D0 Control Register 4 (AD0CON4)

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- MPS11 to MPS10: Multi-port Sweep Port Select Bit
- Set to 00b when using any mode other than multi-port sweep mode.

(6) Set the port P10_i function select register (i = 0 to 7).

Port P10_i Function Select Register (P10_iS)

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
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</tbody>
</table>

- PSEL2 to PSEL0: Port P10_i Output Function Select Bit
- 000b: I/O port P10_i
- ASEL: Port P10_i Analog Function Select Bit
  - 1: AN_i
- Set to 0.

(7) Set the port P10 direction register.

Port P10 Direction Register (PD10)

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
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<tbody>
<tr>
<td>1</td>
<td>0</td>
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</tbody>
</table>

- PD10_7 to PD10_0: Port P10_i Direction Bit
- Set the direction bit corresponding to the analog input pin selected by bits CN2 to CN0 in the AD0CON0 register to 0 (input).

(8) Start A/D conversion (set the A/D0 control register 0).

A/D0 Control Register 0 (AD0CON0)

<table>
<thead>
<tr>
<th>b7</th>
<th>b0</th>
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<tbody>
<tr>
<td>1</td>
<td>0</td>
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</tbody>
</table>

- ADST: A/D Conversion Start Bit
  - 1: A/D conversion started

(9) Wait for A/D conversion to complete.

(10) Read A/D conversion results (read the A/D0 register i).

A/D0 Register i (AD0i)

<table>
<thead>
<tr>
<th>b15</th>
<th>b14</th>
<th>b13</th>
<th>b12</th>
<th>b11</th>
<th>b10</th>
<th>b9</th>
<th>b8</th>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
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</tr>
</tbody>
</table>

- Lower 8 bits of A/D conversion results
- 10-bit Mode: Upper 2 bits of A/D conversion results
- 8-bit Mode: The read value is 0.
4. **Sample Program**
   A sample program can be downloaded from the Renesas Technology website.

5. **Reference Documents**
   Hardware Manual
   R32C/118 Group Hardware Manual Rev. 1.00
   The latest version can be downloaded from the Renesas Technology website.

   Technical Update/Technical News
   The latest information can be downloaded from the Renesas Technology website.

   C Compiler Manual
   R32C/100 Series C Compiler Package Ver. 1.02 Compiler User’s Manual Rev. 1.00
   The latest version can be downloaded from the Renesas Technology website.
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csc@renesas.com

<table>
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<tr>
<th>REVISION HISTORY</th>
<th>A/D Conversion in One-shot Mode</th>
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</thead>
<tbody>
<tr>
<td>Rev.</td>
<td>Date</td>
</tr>
<tr>
<td>1.00</td>
<td>Mar. 5, 2010</td>
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