9FGV100x

PhiClock OTP Procedure

Contents

1. Introduction 1

2. Operation Mode 2

2.1 I2C Mode 2

2.2 Configuration Mode 2

3. OTP Procedure 2

3.1 Power Supply Requirement 2

3.2 OTP Steps 2

4. Revision History 4

1. Introduction

The Phiclock family 9FGV100x contains four non-volatile 8-bit registers (see Figure 1). The non-volatile registers are One-Time Programmable (OTP), and are pre-programmed at the factory with a custom dash-code configuration.

The device operates according to the settings in the RAM registers. At power-up, a pre-programmed configuration is transferred from OTP to RAM registers. The device behavior can also be modified by reprogramming the RAM registers through I2C. This document explains how to program the four OTP banks.

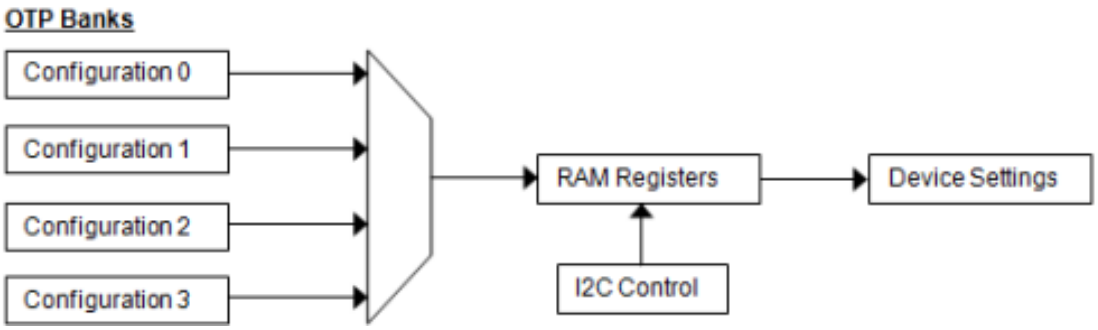

Figure 1. Register Maps

For information on product operation and register descriptions, refer to the product datasheet and product Register Descriptions and Programming Guide.

2. Operation Mode

The 9FGV100x can operate in I2C mode or Configuration mode, which is controlled using the vREF0_SEL_I2C# pin at power-up latched selection.

2.1 I2C Mode

Pin SEL0/SCL and SEL1/SDA will operate as the I2C bus. Register 0x00[1:0] is the load configuration number, 0~3, that will be loaded from OTP into the registers at power up. When changing these bits through I2C, it instructs the chip to load another configuration from OTP.

2.2 Configuration Mode

Pin SEL0/SCL and SEL1/SDA will operate as the select pins. These two select pins allow for hardware selection of the desired configuration. The user can configure any one of the four OTP configuration banks.

3. OTP Procedure

Each OTP bank contains register map, 0x01 to 0x27. All four OTP banks will share the same header information register 0x00. The user can configure any one of the four OTP configurations first, and configure other OTP configurations at other times. For first time OTP must configure the header information (see step 3 in Section 3.2).

3.1 Power Supply Requirement

The I2C bus operates only at 2.5V and 3.3V (VDDDp and VDDAp supply 2.5V or 3.3V). The OTP_VPP pin needs 6.5V during the OTP. After OTP, OTP_VPP will be the same as VDDDp.

3.2 OTP Steps

1. Apply 6.5V to the OTP_VPP pin.
2. Program the OTP banks.

Header Information			
	addr	data	Description
[slave 0xD0] wr	00	80	Register 00 fixed value 0x80

Config 0			
	addr	data	Description
[slave 0xD0] wr	01	reg data	Register 01 to 27
[slave 0xD0] wr	1A	20	
[slave 0xD0] wr	1A	A0	Calibration
[slave 0xD0] wr	2E	00	CSR_RD_ADDR
[slave 0xD0] wr	2D	00	CSR_BN_ADDR
[slave 0xD0] wr	29	80	AUX_TST_UP
[slave 0xD0] wr	2A	00	OTP_Start_addr
[slave 0xD0] wr	2B	00	OTP_END_ADDR[8]
[slave 0xD0] wr	2C	27	OTP_END_ADDR[7:0]
[slave 0xD0] wr	28	08	Wait for at less 200us before program 00
[slave 0xD0] wr	28	00	

Config 1			
	addr	data	Description
[slave 0xD0] wr	01	reg data	Register 01 to 27
[slave 0xD0] wr	1A	20	
[slave 0xD0] wr	1A	A0	Calibration
[slave 0xD0] wr	2E	01	CSR_RD_ADDR
[slave 0xD0] wr	2D	01	CSR_BN_ADDR
[slave 0xD0] wr	29	80	AUX_TST_UP
[slave 0xD0] wr	2A	28	OTP_Start_addr
[slave 0xD0] wr	2B	00	OTP_END_ADDR[8]
[slave 0xD0] wr	2C	4E	OTP_END_ADDR[7:0]
[slave 0xD0] wr	28	08	Wait for at less 200us before program 00
[slave 0xD0] wr	28	00	

Config 2			
	addr	data	Description
[slave 0xD0] wr	01	reg data	Register 01 to 27
[slave 0xD0] wr	1A	20	
[slave 0xD0] wr	1A	A0	Calibration
[slave 0xD0] wr	2E	01	CSR_RD_ADDR
[slave 0xD0] wr	2D	01	CSR_BN_ADDR
[slave 0xD0] wr	29	80	AUX_TST_UP
[slave 0xD0] wr	2A	4F	OTP_Start_addr
[slave 0xD0] wr	2B	00	OTP_END_ADDR[8]
[slave 0xD0] wr	2C	75	OTP_END_ADDR[7:0]
[slave 0xD0] wr	28	08	Wait for at less 200us before program 00
[slave 0xD0] wr	28	00	

Config 3			
	addr	data	Description
[slave 0xD0] wr	01	reg data	Register 01 to 27
[slave 0xD0] wr	1A	20	
[slave 0xD0] wr	1A	A0	Calibration
[slave 0xD0] wr	2E	01	CSR_RD_ADDR
[slave 0xD0] wr	2D	01	CSR_BN_ADDR
[slave 0xD0] wr	29	80	AUX_TST_UP
[slave 0xD0] wr	2A	76	OTP_Start_addr
[slave 0xD0] wr	2B	00	OTP_END_ADDR[8]
[slave 0xD0] wr	2C	9C	OTP_END_ADDR[7:0]
[slave 0xD0] wr	28	08	Wait for at less 200us before program 00
[slave 0xD0] wr	28	00	

3. Program the Header Information (for the first time OTP).

Header Information			
	addr	data	Description
[slave 0xD0] wr	00	80	Customer register 0 value. It can be any value
[slave 0xD0] wr	2E	00	CSR_RD_ADDR
[slave 0xD0] wr	2D	00	CSR_BN_ADDR
[slave 0xD0] wr	29	80	AUX_TST_UP
[slave 0xD0] wr	2A	00	OTP_Start_addr
[slave 0xD0] wr	2B	00	OTP_END_ADDR[8]
[slave 0xD0] wr	2C	00	OTP_END_ADDR[7:0]
[slave 0xD0] wr	28	08	Wait for at less 200us before program 00
[slave 0xD0] wr	28	00	
[slave 0xD0] wr	1A	20	
[slave 0xD0] wr	1A	A0	Calibration

4. Set the register back to normal.

	addr	data	Description
[slave 0xD0] wr	2B	00	OTP_END_ADDR[8]
[slave 0xD0] wr	2E	00	CSR_RD_ADDR
[slave 0xD0] wr	2D	00	CSR_BN_ADDR
[slave 0xD0] wr	29	00	AUX_TST_UP

5. Apply VDDDp to the OTP_VPP pin.

4. Revision History

Revision	Date	Description
1.0	May.05.20	Initial release.

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