Introduction

The 82P337xx/8xx/9xx System Clock (OSCI) supports eight (8) common frequencies: 10MHz, 12.8MHz, 13MHz, 19.44MHz, 20MHz, 24.576MHz, 25MHz or 30.72MHz. Although 30.72MHz is a common 3G reference clock available as a TCXO or OCXO, another common frequency is 19.2MHz; which is not natively supported by the 82P337xx/8xx/9xx.

Fortunately, the device's System APLL has flexibility to allow support of this frequency. This application note describes a tested procedure to program the System APLL to allow the 82P337xx/8xx/9xx to use a 19.2MHz System Clock.

Procedure to Program System APLL

The System APLL support eight (8) frequencies, which are set via HW pins XO_FREQ[2:0].

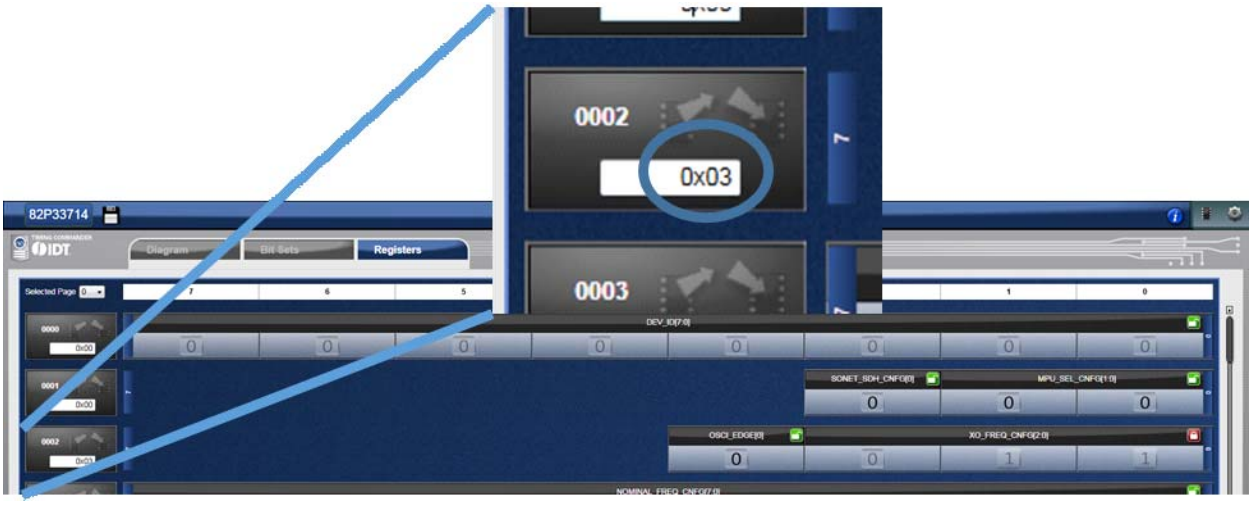
Figure 1. 82P337xx/8xx/9xx XO_FREQ[2:0] Pins

XO_FREQ0/ LOS0 XO_FREQ1/ LOS1 XO_FREQ2/ LOS2	I pull-down	CMOS	**XO_FREQ0 ~ XO_FREQ2:** These pins set the oscillator frequency. XO_FREQ[2:0] Oscillator Frequency (MHz) 000 10.000 001 12.800 010 13.000 011 19.440 100 20.000 101 24.576 110 25.000 111 30.720 **LOS0 ~ LOS2 -** These pins are used to disqualify input clocks. See input clocks section for more details. After reset, these pins take on the operation of LOS0-2.

To support 19.2MHz, the System Clock frequency needs to be initial set to 19.44MHz. Although a 19.2MHz clock will be seen at OSCI, the 82P337XX/8XX/9XX will still power-up and support the microprocessor interface (SPI, I2C, UART or EEPROM).

The XO_FREQ setting can be confirmed via the read-only XO_FREQ_CNFG[2:0] bits (Page 0, Register 0x002).

Figure 2. XO_FREQ[2:0] Pins Set to 19.44MHz (as seen via XO_FREQ_CNFG[2:0] bits)



After power-up, the System APLL VCO needs to be configured for the new System Clock frequency. This is done via the following registers on Page 5, Addresses 0x1D to 0x25.

- SYS_DIVN_FRAC_CNFG[20:0] = 0x022222 (139810)
  #Fractional

  WriteReg 5 0x1D 0x22

  WriteReg 5 0x1E 0x22

  WriteReg 5 0x1F 0x02
- SYS_DIVN_DEN_CNFG[15:0] = 0x004B (75)
  #Denominator

  WriteReg 5 0x20 0x4B

  WriteReg 5 0x21 0x00
- SYS_DIVN_NUM_CNFG[15:0] = 0x000A (10)
  #Numerator

  WriteReg 5 0x22 0x0A

  WriteReg 5 0x23 0x00
- SYS_DIVN_INT_CNFG[5:0] = 0x11 (17)
  #Integer

  WriteReg 5 0x25 0x11

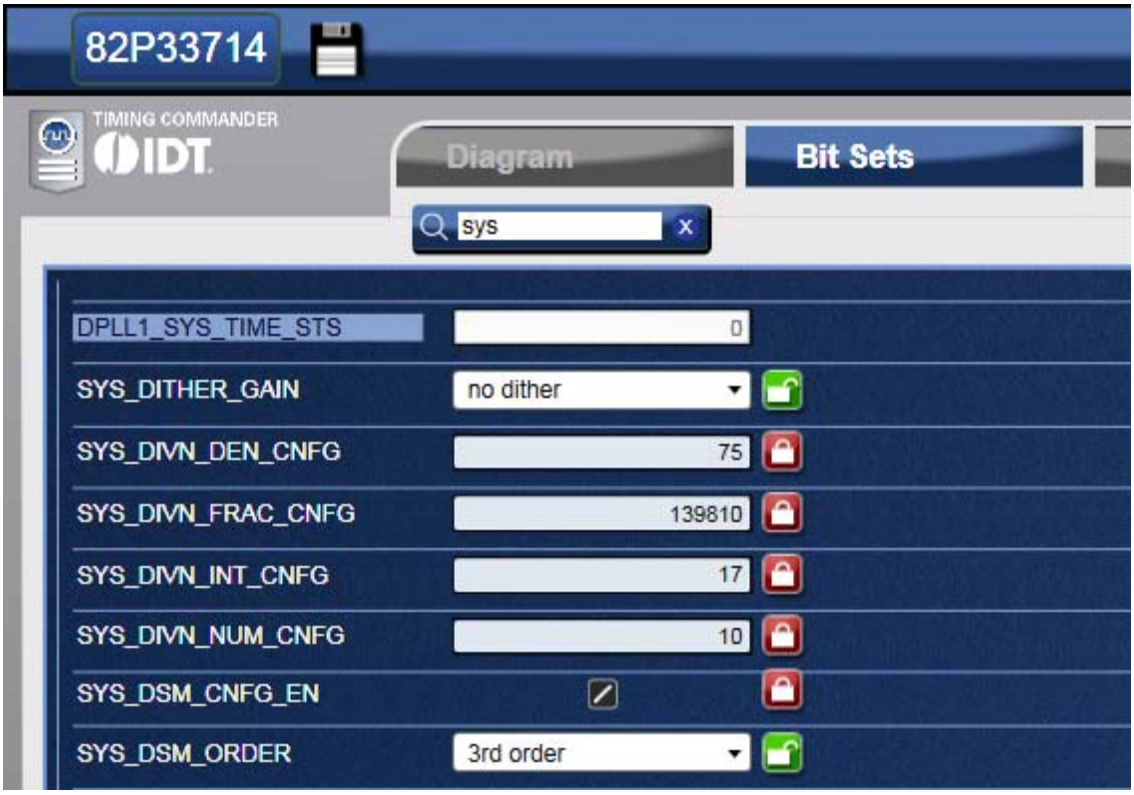
Once the VCO is configured, the new configuration must be enabled.

- SYS_DSM_CNFG_EN = b'1 (Enable)
  #Enable

  WriteReg 5 0x24 0x13

These settings are summarized in the figure below, as seen through the Timing Commander "Bit Sets" view of the 82P337xx/8xx/9xx Personality.

Figure 3. Figure 3: Settings for System APLL VCO



The above registers can also be programmed via EEPROM, to simplify the power-up/reset procedure.

For questions related to device configurations, please contact IDT application support at support-sync@idt.com

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