Using the Reference Layout

The P9235A-R-EVK reference layout is a full feature four-layer design optimized for high-performance, small-size, and ease-of-use. The purpose is to minimize design-in effort and risk by providing a proven solution that can be imported into an existing system design. The P9235A-R-EVK board layout is divided into two parts; the main function layout (core layout) and the layout for test purpose. When imported into an existing system, only the core layout is necessary.

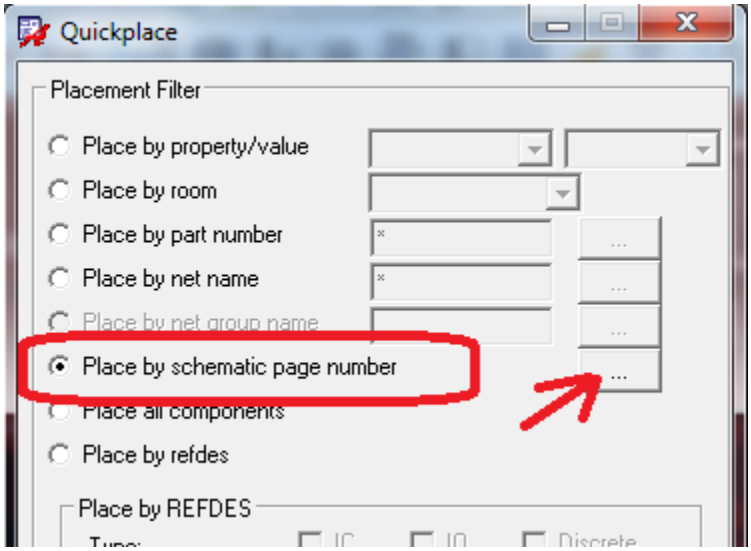
The layout has only two layers – top and bottom. The core layout has a minimum space and trace width of 5 mils. The minimum finished VIA size is 6 mils, assuming 1 mil plating thickness. The minimum spacing between components is 10 mils. Only through-hole VIAs are used and no blind or buried VIAs. When circumstances permit, it is highly recommended to copy the reference layout.

Importing the Reference Layout

The P9235A-R-EVK reference design was created using Cadence PCB design software. This software has been used to generate layout modules which can be rapidly deployed onto PCB designs using Cadence OrCAD CIS and Cadence Allegro PCB Editor. The P9235A-R layout module is labeled P9235A-R-EVK.mdd and will load into an existing or new PCB design file by following these instructions:

1. Use or copy the P9235A-R-EVK schematic file (.dsn) and export the netlist to a PCB file.
2. Move the file P9235A-R-EVK.mdd to the same directory as the PCB design file.
3. Import the netlist into the PCB file (.brd).
4. Open the PCB design file (.brd) and click on the menu Place→Quickplace…
   a. Select Place by Page Number and select the page the P9235A-R circuitry resides on.

Figure 1. Cadence Quickplace option box used for placing the IDT Layout module by page number.



   b. Click Place. Click Ok.
5. Select the parts that were placed from the schematic that matches the schematic used from the P9235A-R-EVK.
   a. In the Find Filter, select Symbols, then left click and drag to highlight all of the components that were just placed.
   b. Right click on any of the highlighted parts and select “Place Replicate Apply→Browse…”
   c. Select the P9235A-R-EVK.mdd file and select Ok.
   d. Components should be matched, if unmatched manually identify and match component reference designators based on schematic location.
6. Enter the coordinates(x,y location) in the command window where the P9235A-R circuit should be located at or left click where the P9235A-R should be placed.

Connecting Power

The reference board layout has been designed such that the DC input is easily accessible when being imported on to a system board. The input voltage traces are designed to accept a surface mount micro USB power plug. Wide, low-impedance traces are recommended to minimize the DC voltage drop on its way to and from the device.

Connecting Inputs / Outputs

All input and outputs on the reference board are placed near the edges of the reference layout such that they can be easily connected to other parts of the system board. After placing the module in the specific design, use the labeled VIAs as connection points for new traces on either the top or bottom layer.

Manufacturing Notes

PCB should be made with a minimum of 1 oz. copper foil weight per square foot or heavier.

Additional Resources

All support files and collateral for the P9235A-R-EVK reference board can be found at **www.IDT.com/WP3W-RK**. Files include: schematics, layout files, datasheets, user manual, etc.

Custom Layout Guidelines

The P9235A-R wireless power transmitter is an integrated device consisting of multiple high-power blocks along with noise sensitive circuits all controlled by an internal microprocessor. When designing the printed circuit board (PCB) there are multiple considerations and often some tradeoffs associated with managing the critical current paths. In order to optimize the design, components should be placed based on circuit function to guarantee best performance when the schematic is implemented into a PCB design. Furthermore, the thermal management of the application is important to the product's performance and should be optimized during PCB design. By following the guidelines set forth in this document, efficient operation will be obtained for each circuit function.

At the time that the layout is started the following guidance should be used to place the most critical parts in order of priority. There are three main categories of circuitry: (1) Power Circuits, (2) Sensitive Circuits, and (3) Non-Sensitive Circuits.

Layout Priority Checklist:

1. Route the power connections sufficient wide depending on the expected current. For 1 oz. copper, 15 mils are recommended for 800 mA with less than 20°C temperature rise. These connections include:
    - The power input path: VIN_USB (input power connection node), Q1 (in rush current protection FET), VIN_5V, R6 (current sense resistor), V_BRIDGE (power rail to the external H bridge), GND_BRG (H bridge ground pin), EPGND.
    - The Cin connected to the V_BRIDGE node (this supplies the power to the H bridge that drives the LC tank): C10, 11, 12, 30, 31
    - The transmitter LC tank: Q2 (half of the FET H bridge, 2 N channel FETs), Q3 (the other half of the H bridge), C15, 17, 23, 25 (tank series capacitance), L2_1, L2_2 (connections to the tank series inductance)
    - The input voltage to the LDOs: VIN_LDO node
    - The step down (buck) regulator components: Cin (C18,19), L1 (inductor), Cout (C20, 21)
2. Use the next closest layer to the P9235A-R device as a solid GND plane.
3. Avoid unnecessary layer transitions of the power connections (V_BRIDGE; CINs; the outputs of the H Bridge to the LC Tank: Q2 pin 4, 5 node and Q3 pin 4, 5 node and finally the IC pin GND_BRG). Use at least 6 mil finished size VIAs for any layer transitions of these connections for 400 mA load current.
4. Attempt to place the P9235A-R as close as possible to the center of the allocated layout area.
5. The external power FETs (Q2, Q3) will dissipate the most heat. Connect at least 3 6 mil finished VIAs to each of the PGND connections of the external FET pairs (Q2, Q3, pin 2) to insure good heat sinking through the bottom ground plane. Place as much

solid ground plane in those areas as possible. For additional heat dissipation, insure that the drain and source connections of the FET pairs (Q2, Q3, pins 1,4,5) are as thick as possible (For example: For the IDT layout, the average thickness of the Q2 bridge connection, pins 4 and 5, is 90 mils, and it is 540 mils long from pin to the farthest series capacitor, C15. For a rms current of 1A, this gives a temperature rise of less than 2°C.).

6. For P9235A-R IC heat dissipation: Connect at least twelve 8 mil finished VIAs under the Exposed Pad and nearby area. Have a solid, continuous PGND plane under these PGND on the bottom layer. This helps to spread the heat from the IC to PCB.
7. Follow the placement and routing suggestions outlined in the remainder of this document.
8. Use low ESR series resonance capacitors (Cs - C15, 17, 23, 25) to decrease losses in the LC current path. IDT recommends using components with less than 300 mΩ impedance at **100 kHz** operating frequency.

Power Circuits

Figure 4 shows the simplified circuit with key external components of the P9235A-R IC. The loops formed by these external components (shown in Figure 3 and Figure 4) need to be adressed first to achieve best performance.

The optimal P9235A-R orientation relative to the transmitter coil (LTX) and the input micro USB connector physical locations are presented in Figure 7: The main power current path is considered the connection from the micro USB connection (J1), through the in rush current protection FET (Q1), through the current sense resistor (R6), through the H bridge FETs (Q2, 3), and finally through the LC tank series capacitance (C15, 17, 23, 25) and the LC tank inductor (L2_2, L2_1) connections.

Figure 2. P9235A-R Schematic

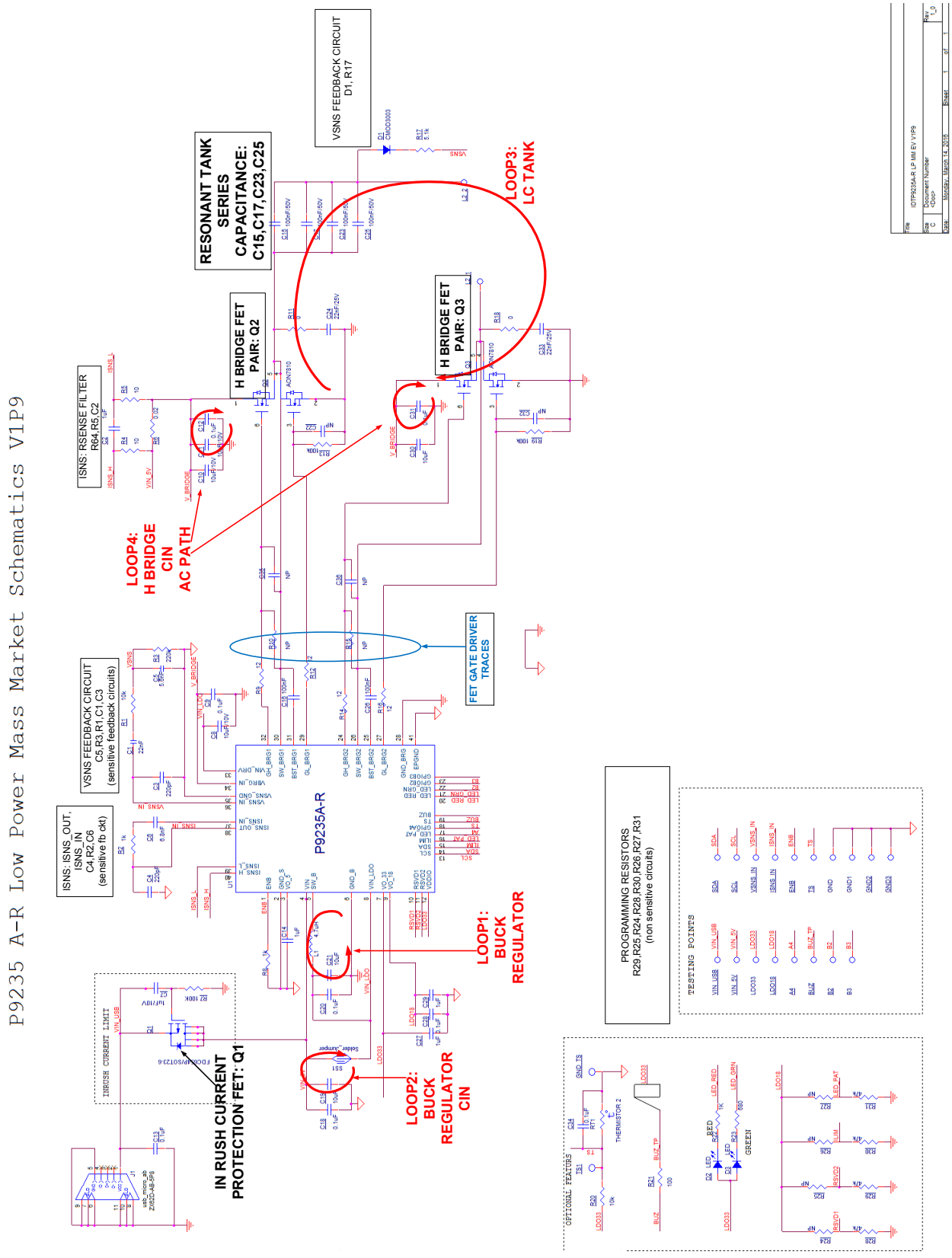
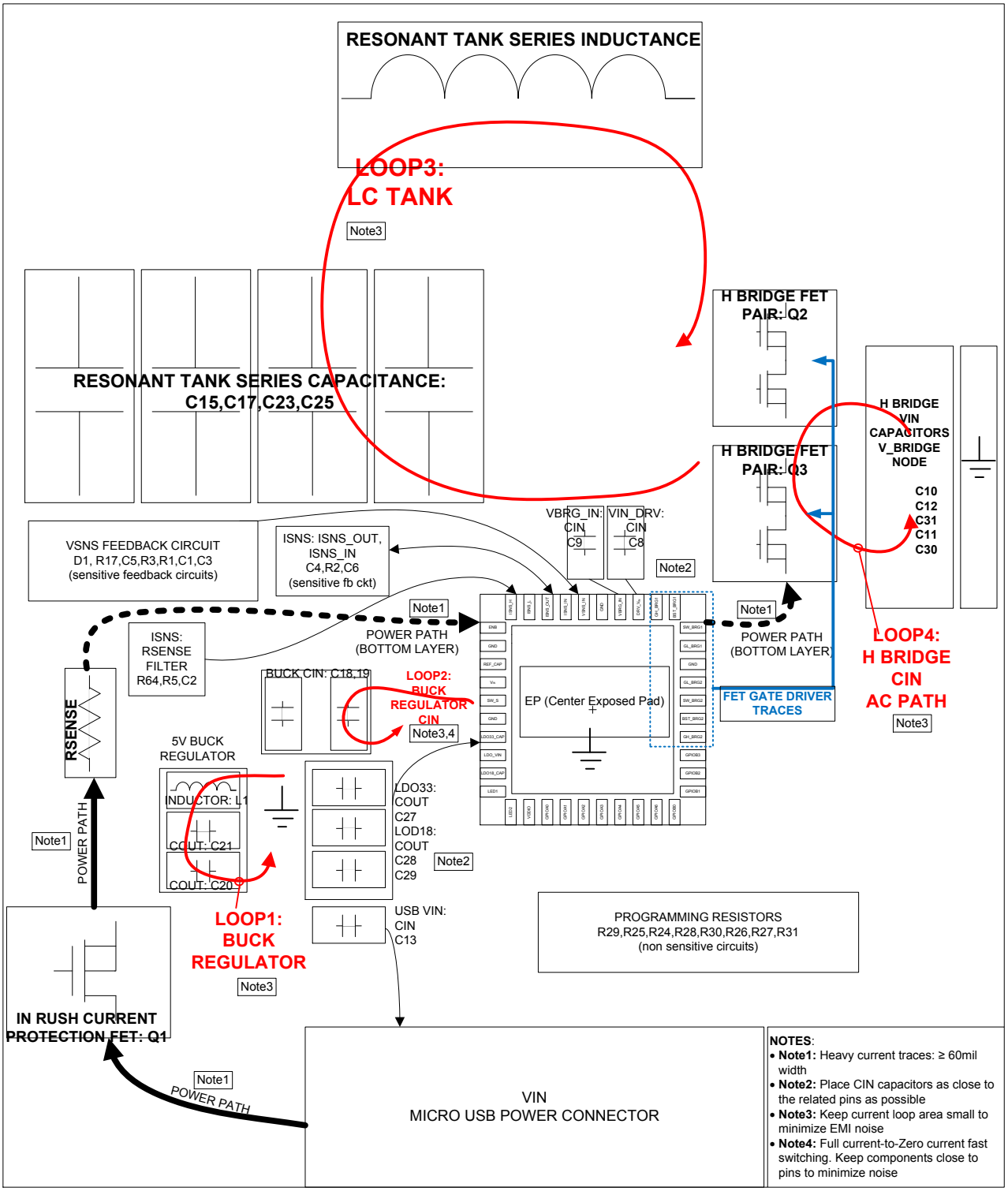


Figure 3. Block diagram of physical positioning and main current loops of the P9235A-R layout.



As soon as the final shape of the PCB has been determined (based on system constraints), the connection points for the transmitter coil (L_{TX}) should be determined. Next, the P9235A-R should be placed as close to the center of the allocated PCB area as possible. The orientation of the device should be determined based on the ability to route connections and place the necessary components in the following order of priority:

1. **H Bridge**: Place H bridge FETs (Q2, Q3)and LC tank capacitance (C15, C16, C23, C25) close to each other, to form a small current loop, to avoid EMI emissions.
2. **H Bridge Cin**: Place the V_BRIDGE (schematic net name) Q2, Q3 H Bridge capacitors (C10, 11, 12, 30, 31), such that the traces are short. This is the large DC and AC current path.
3. **Gate driver circuit**: The gate driver circuit consists of many components that must be placed in close proximity to the related H bridge FETs (Q2, Q3) to avoid noise issues. These include:
    a. Low Side Gate RC filters (Q3: R19, C32; Q2: R13, C22),
    b. High Side Gate RC filters (Q3: R15, C36; Q2: R10, C35) and
    c. Output RC Snubbers (Q3: R18, C33; Q2: R11, C24)
4. **Gate driver traces**: The gate driver traces must be tightly coupled. They should run parallel and close to each other. Make these traces short. Running under the switch nodes (Q2 pins 4 and 5 node, Q3 pins 4 and 5 node) should be avoided. Run these traces under the relatively quiet V_BRIDGE node instead. Surround these traces with the ground plane to provide a tight loop AC signal return path to avoid EMI noise.
5. **CIN**: Place all IC pin input voltage capacitors close to their related pins (VIN: C18, C19, VIN_DRV: C8, VBRG_IN: C9).
6. **COUT**: Place all IC pin output voltage capacitors (C14, C27, C28, C29) close to their related pins (VO_5: C14, VO_33: C27, VO18: C28, C29).
7. **Current Sense**: Place the bridge input current sense resistor (R6) and the filtering components (R4, R5, C2) tightly together, and close to their related pins (ISNS_H, ISNS_L). Use a Kelvin connection to connect the filter components to the current sense resistor. A differential pair is recommended to connect the filter output and the related pins, in order to reduce measurement noise.
8. **Current Demodulation**: Place the current demodulation circuit components (C4, R2, C6) tightly together and close to their related IC pins (ISNS_OUT, ISNS_IN).
9. **Voltage Demodulation**: Place the voltage demodulation circuit components (D1, R17, R3, C5, R1, C1, C3) tightly together and close to their related IC pins (VSNS_IN, VSNS_GND).
10. **Buck Regulator Cin**: Place the buck regulator input capacitance (C18, C19) close to the related pins (VIN, GND_B). These components see instantaneous switching between full load and no load, causing noise issues if these traces are not as short as possible.
11. **Buck Regulator L, Cout**: Place the buck regulator inductance and output capacitance such that they form the smallest possible current loop to minimize EMI transmissions (L1; C20, 21).

Thermal Performance: Keep the ground plane below the P9235A-R IC as intact as possible. This will improve thermal performance as a solid ground plane will allow heat to leave the IC much more effectively than a fragmented ground plane.

Transmitting coil and LC Tank Circuit

The transmitter LC tank circuit consists of the transmitter coil, (connected to L2_2, L2_1), the series resonant capacitor, Cs (C15, C17, C23, C25). The current running through the loop formed by these components contains high frequency harmonics and it is essential to minimize the loop area to reduce the EMI noise induced by the current. Place the loop on the top layer with the traces close to each other to minimize the loop area. Lay a ground layer under this loop to further shielding the unwanted EMI filed. Figure 5 shows the recommend layout, which is captured from P9235A-R EV Kit layout.

Figure 4. P9235A-R Top Layer – LC Tank Current Path

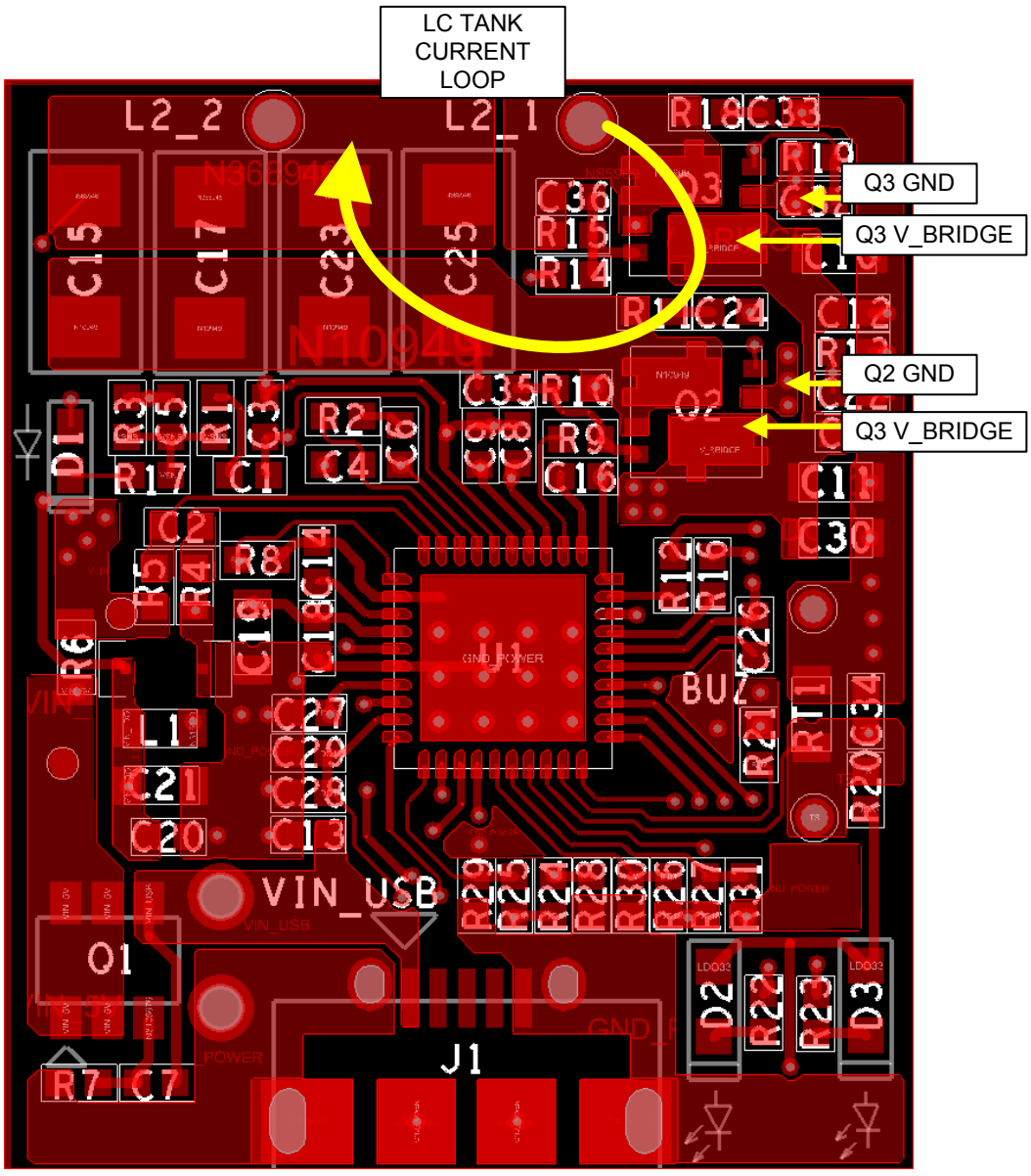
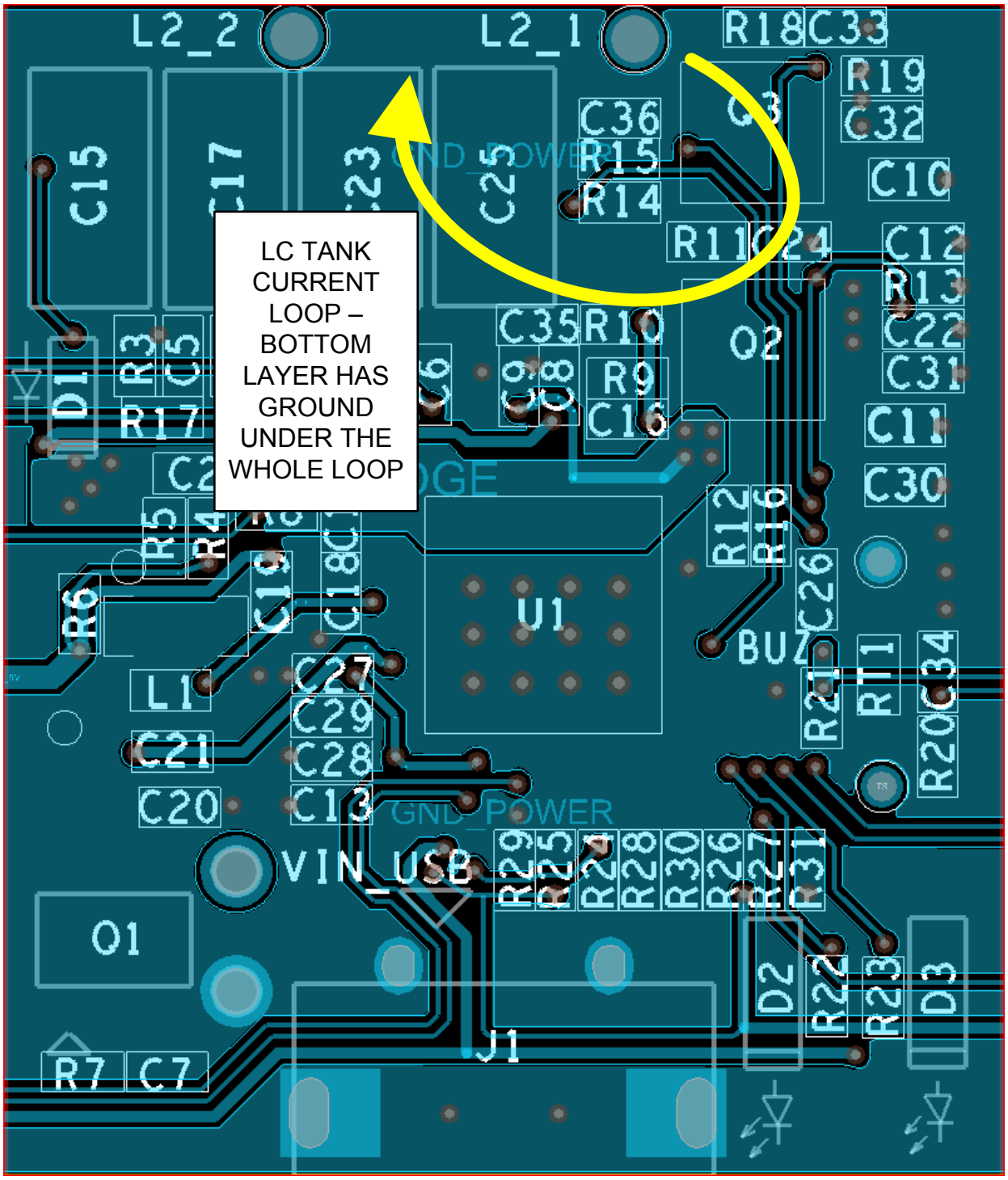


Figure 5. P9235A-R Bottom Layer – LC Tank Current Path GND



Main Current Path

The main current path consists of the inrush current protection FET (Q1), the current sense resistor (R6), the H bridge FETs (Q2, Q3), the resonant tank series capacitors (C15, C17, C23, C25), the resonant tank inductor (connected to L2_2, L2_1). After the sense resistor, the power path is transferred to the bottom layer until it arrives at the power FETs (Q2, Q3). This isolates the LC resonant tank current loop from the current loops of other parts of the circuit. This provides a much quieter environment.

Figure 6. P9235A-R Top Layer – Main Power Path

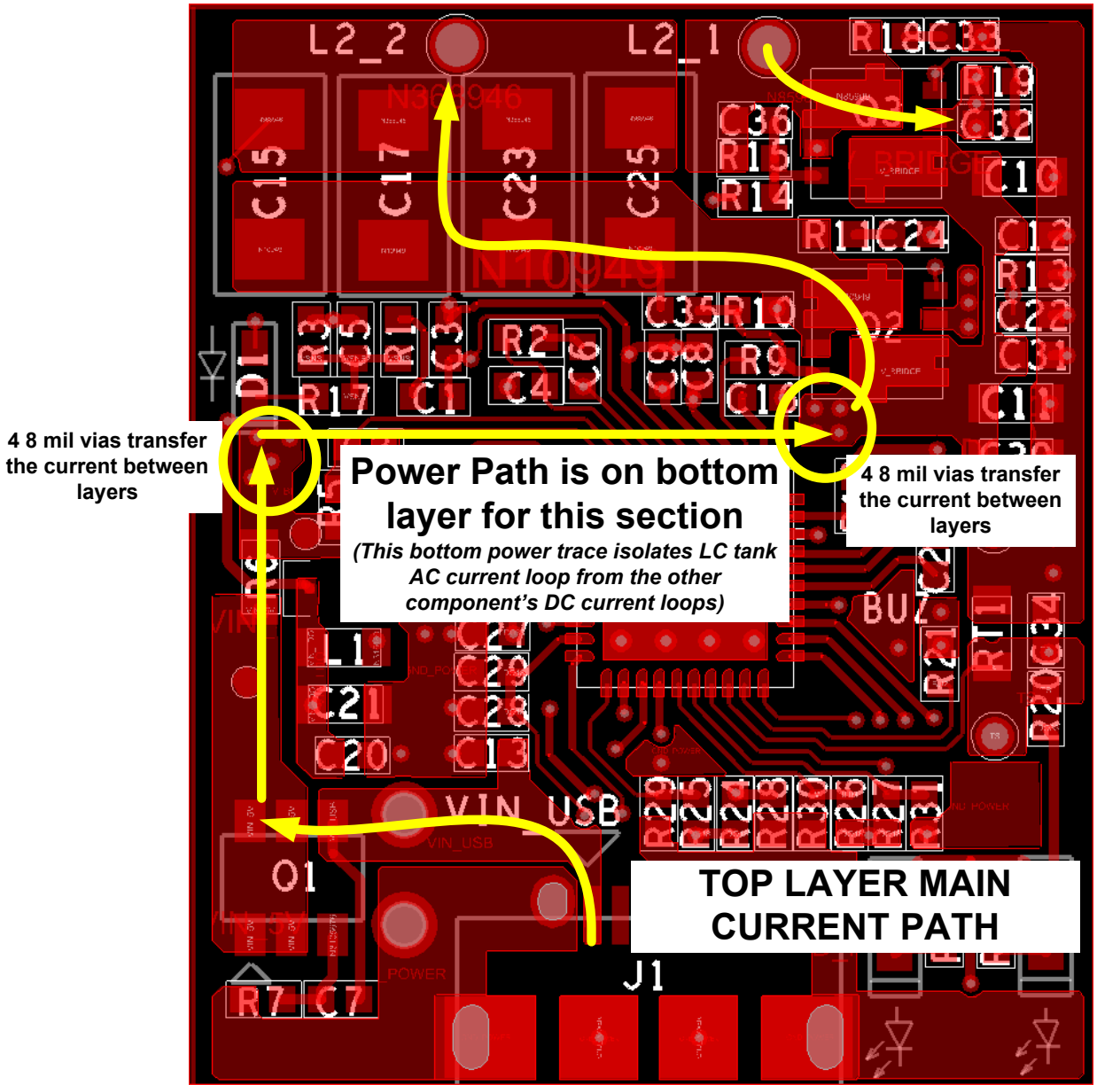


Figure 7. P9235A-R Bottom Layer – Main Power Path

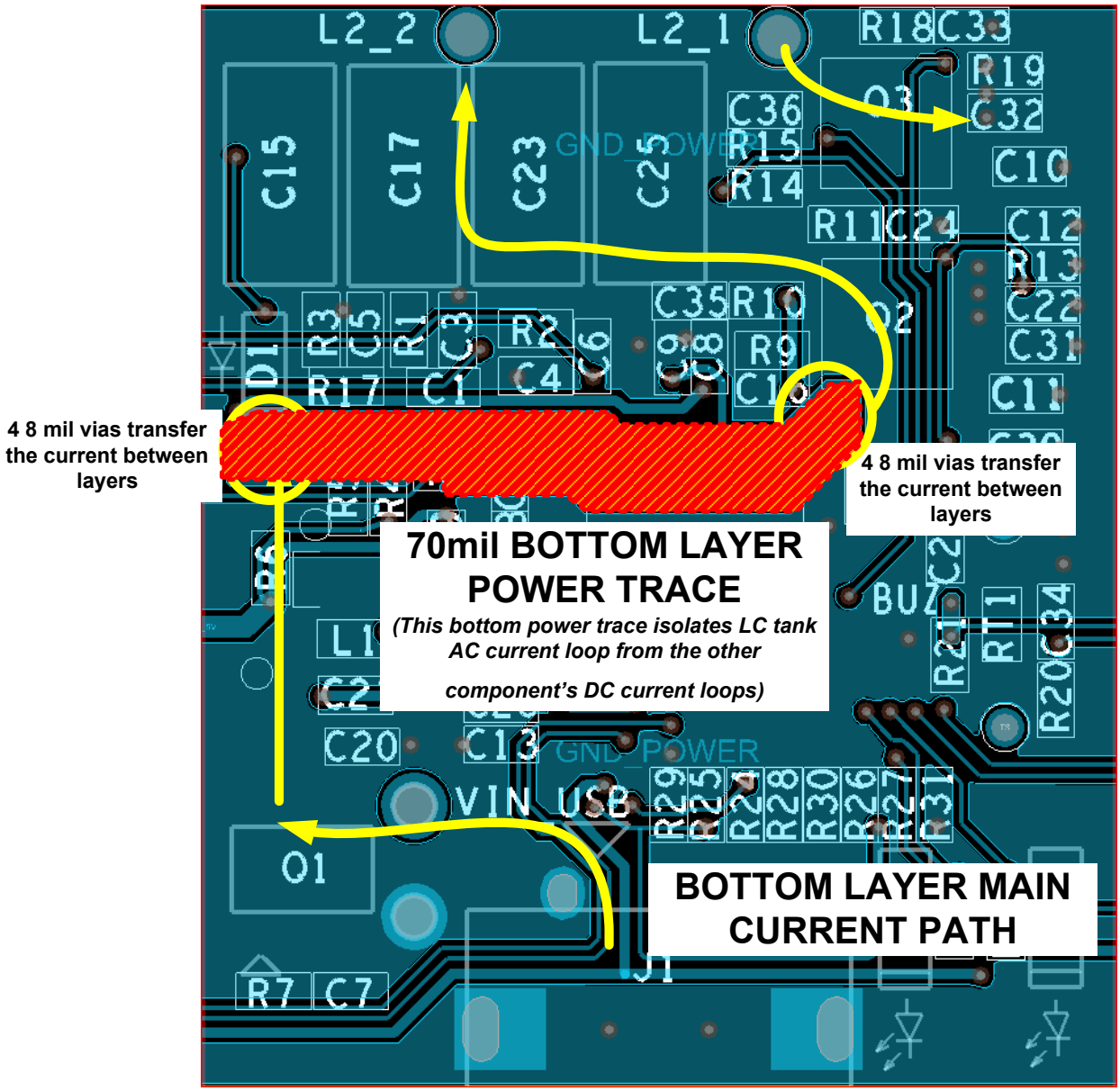
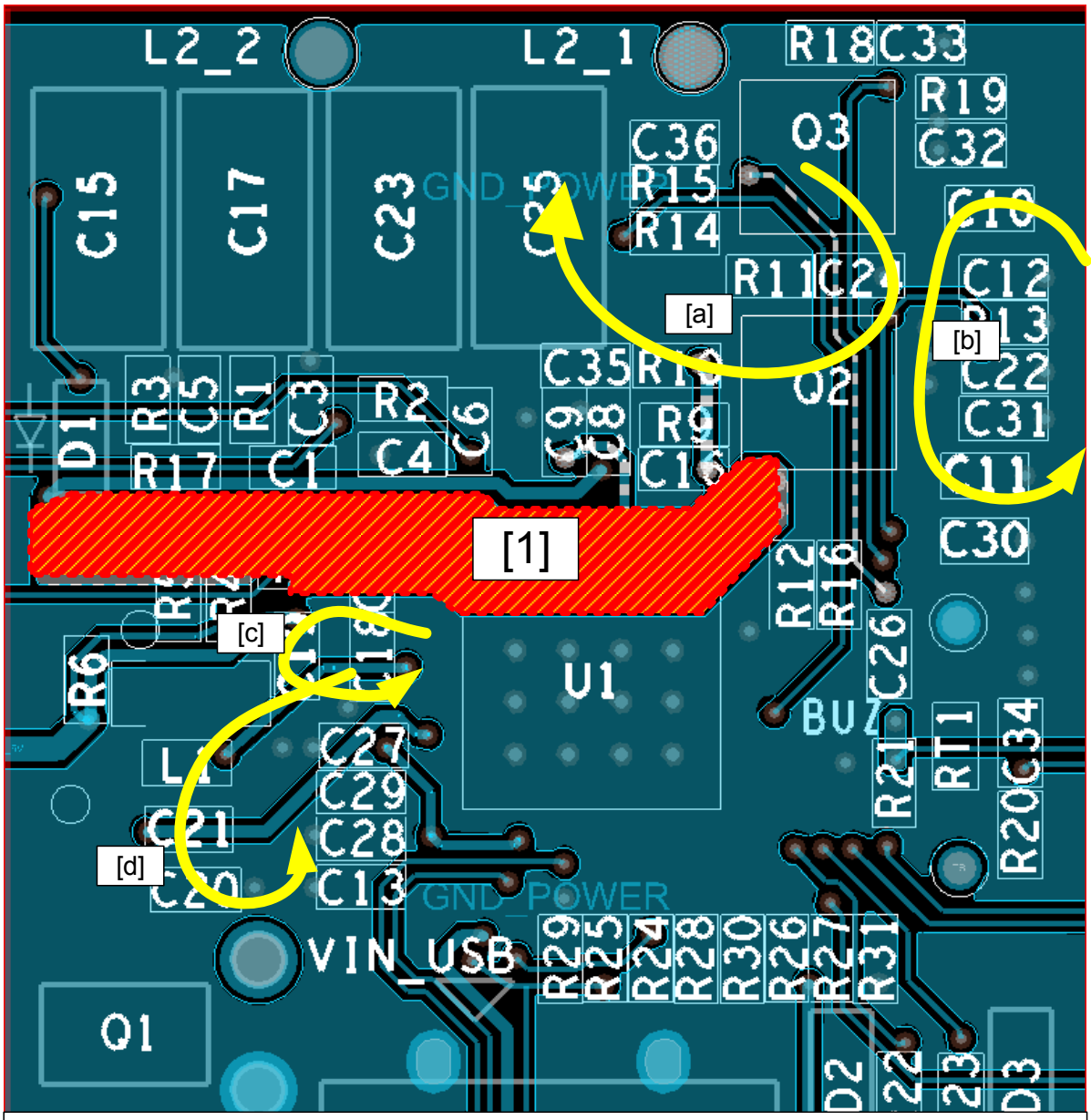


Figure 8. P9235A-R Bottom Layer – Resonant Tank Current Loop Isolation

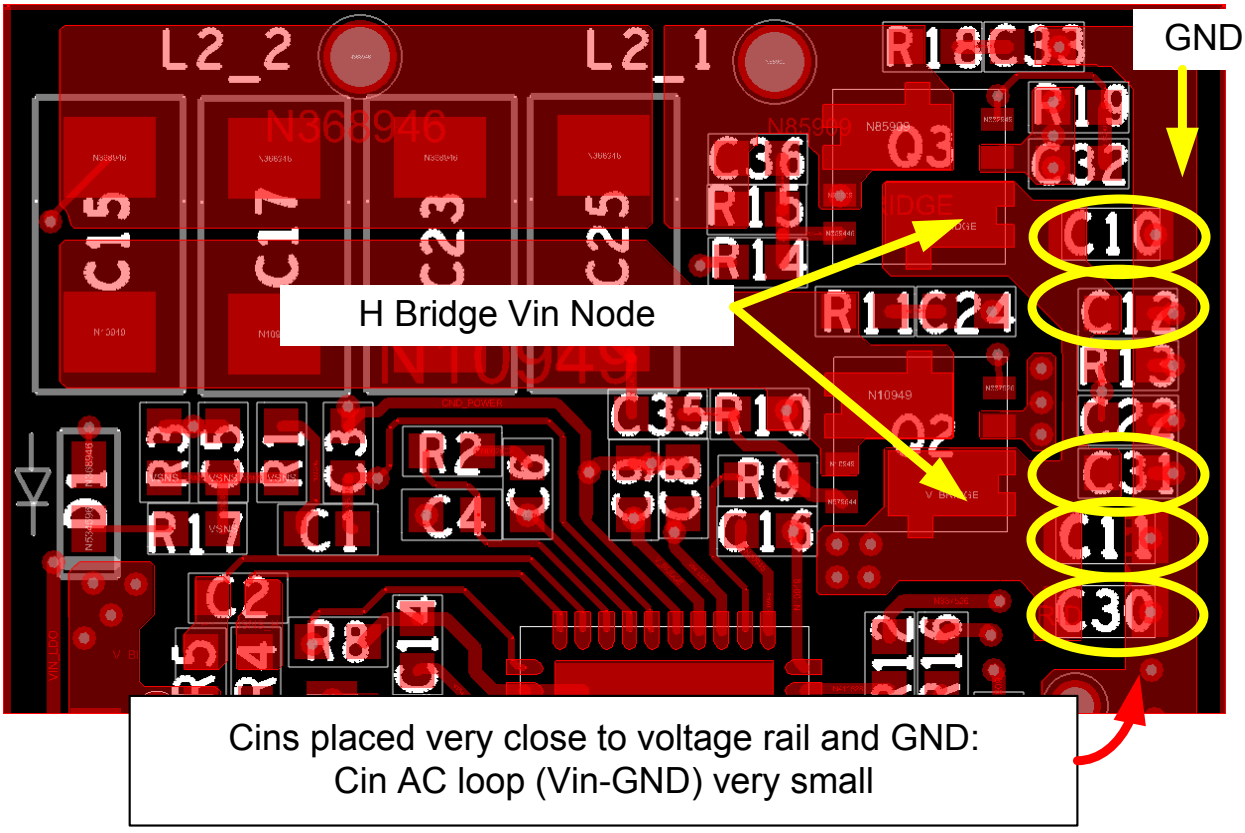


[1] Power Path is on bottom layer for this section.
This bottom power trace isolates LC tank AC current loops
[a] and
[b: Cin,H_brige]
from the other component's current loops such as:
[c: Buck Cin Loop] and
[d: Buck Cout Loop]

H Bridge FET Circuit – CIN, Q2, 3

Place the H bridge input voltage capacitors very close to the related FET leads and to GND. Make sure the traces are short for tight (smallest) AC current loops.

Figure 9. P9235A-R Top Layer – Input Capacitance Physical Placement



H Bridge FET Circuit – Critical Component Placement

There are many filter components that need to be placed next to their respective pins in order to condition the waveforms. These include high (R15, C36, R10, C35) and low side gate RC filters (R19, C32, R13, C22) as well as output RC snubbers (R18, C33, R11, C24). On the other hand place the boost capacitors (C26, C26) close to the IC. Finally, in line gate series resistance (R14, R16, R9, R12) is non sensitive and can be place in trace at a convenient location.

Figure 10. P9235A-H Bridge FET RC Filter and Snubber Placement

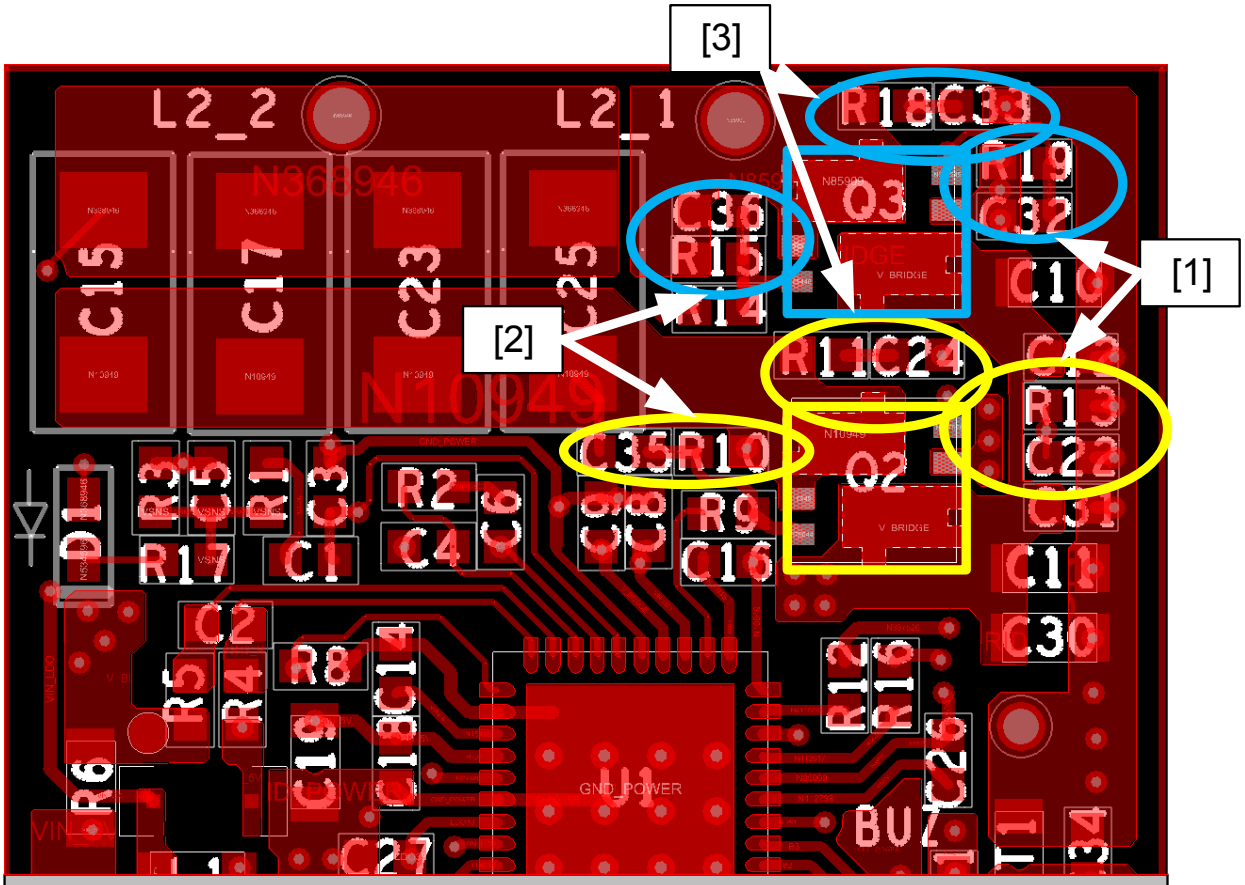
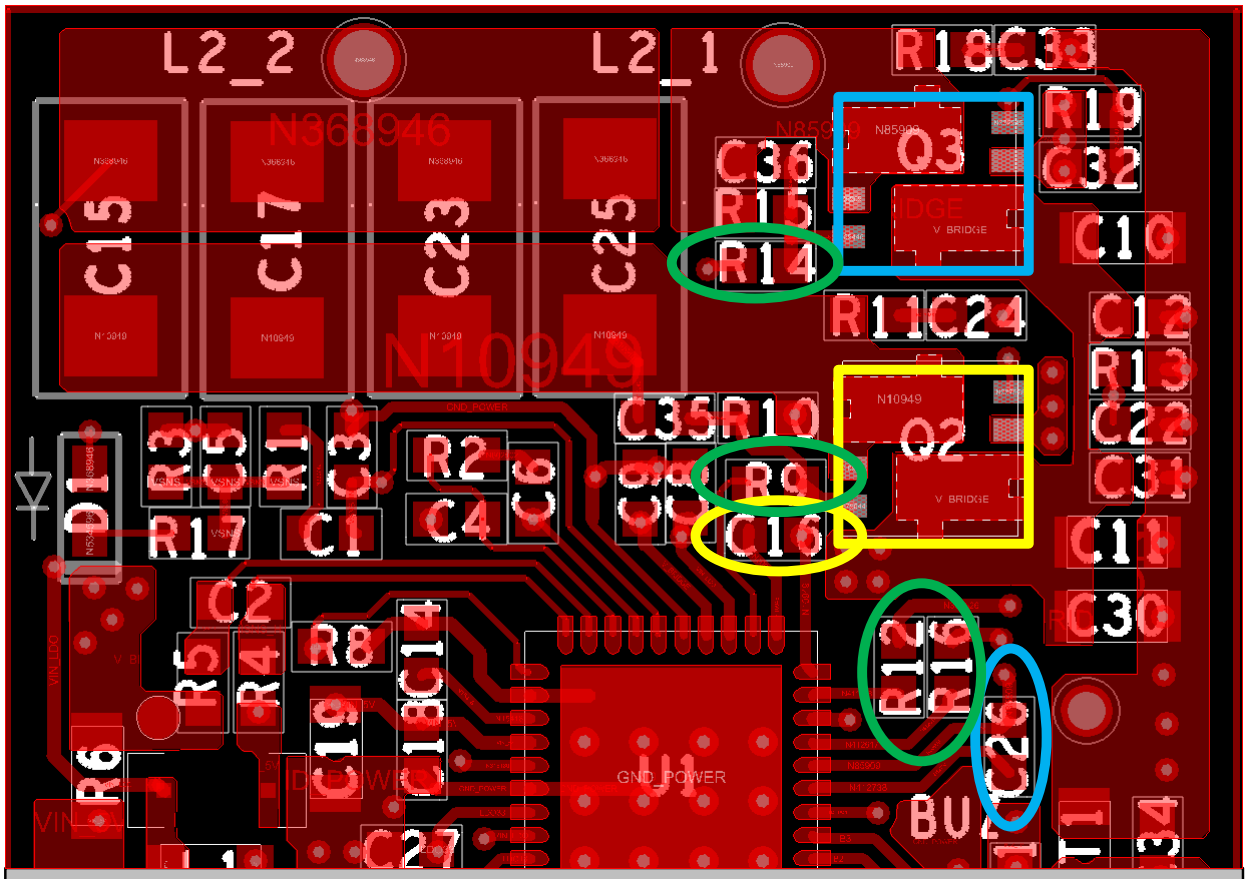


Figure 11. P9235A-R Boost Capacitor and non sensitive gate drive component placement.

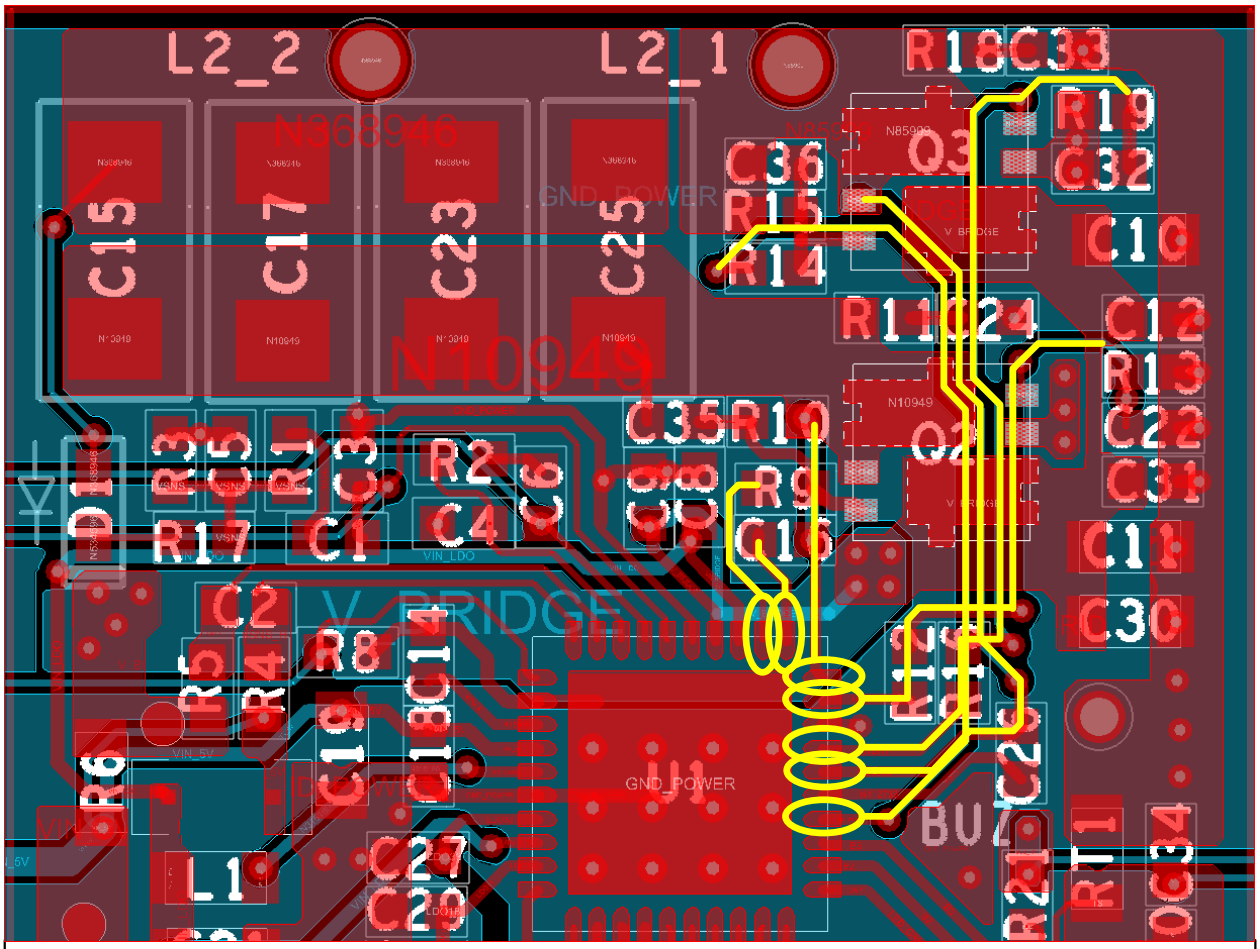


Place the Boost Capacitors (Q3: C26, Q2: C16) close to the IC Gate trace series resistance (Q3: R14, R16, Q2: R9, R12) is non critical. It can be placed in line, in a convenient location.

Gate Drive Trace Placement

The gate driver traces must be tightly coupled. They should run parallel and close to each other. Make these traces as short as possible. Running under the switch nodes (Q2 pins 4 and 5 node, Q3 pins 4 and 5 node) should be avoided. Run these traces under the relatively quiet V_BRIDGE node instead. Surround these traces with the ground plane, to provide a tight loop AC signal return path, to avoid EMI noise.

Figure 12. P9235A-R Top Layer Gate Drive Signals



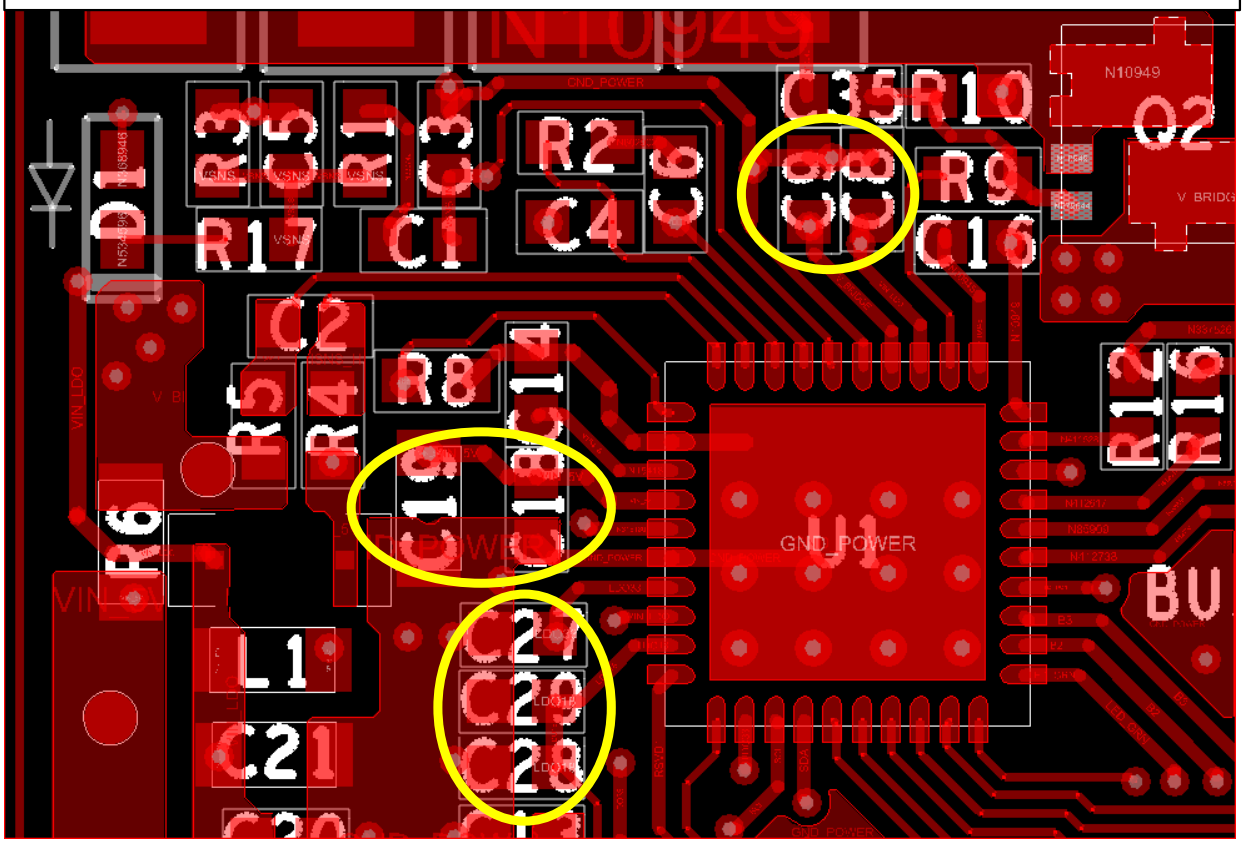
Rout Q2, Q3 Gate drive signals shortest distances possible.
Tightly couple the gate drive signals by running close together in parallel.
When possible avoid routing under the switch nodes (Q2, 3; Pins 4, 5).

Input Capacitance – VIN_5V, VBRG_IN, VIN_DRV, Output Capacitance – VO_5, VO_33, VO_18

Place all IC pin input voltage capacitors close to their related pins (VIN: C18, C19, VIN_DRV: C8, VBRG_IN: C9). Place all IC pin output voltage capacitors (C14, C27, C28, C29) close to their related pins (VO_5: C14, VO_33: C27, VO18: C28, C29).

Figure 13. P9235A-R Top Layer – General Cin, Cout Physical Placement

All Cin and Cout are placed as close to the associated pin as possible (C9: VBRG_IN, C8: VIN_DRV, C18, C19: VIN, C27: VO_33, C28, C29: V0_18).

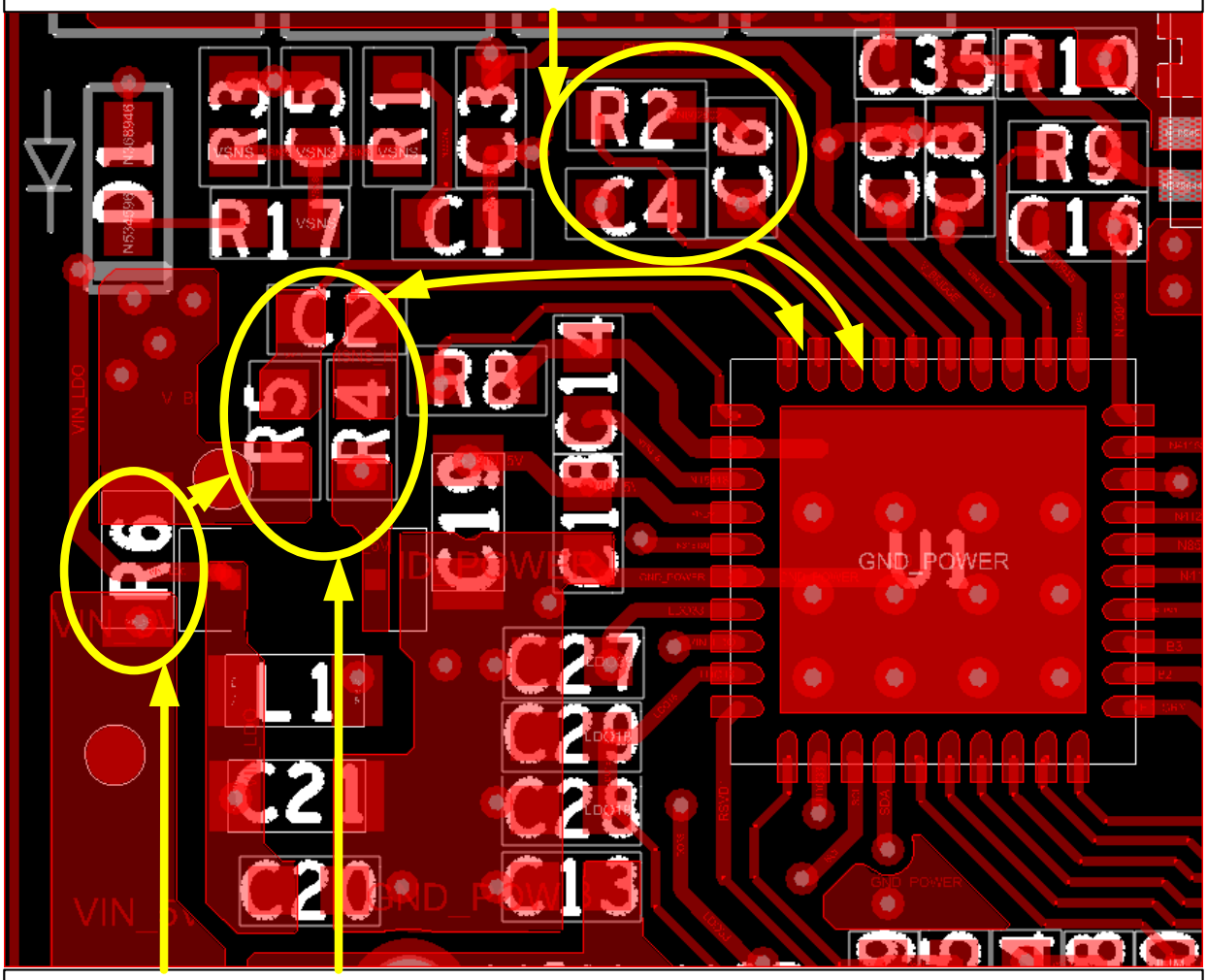


Current Sense Demodulation

Place the current demodulation circuit components (C4, R2, C6) tightly together and close to their related IC pins (ISNS_OUT, ISNS_IN).

Figure 14. P9235A-R Top Layer – Current Sense and Demodulation Physical Placement

The post Rsense conditioning components (C4 ,6; R2) are tightly coupled and placed in close proximity to their related pins (ISNS_OUT, ISNS_IN).



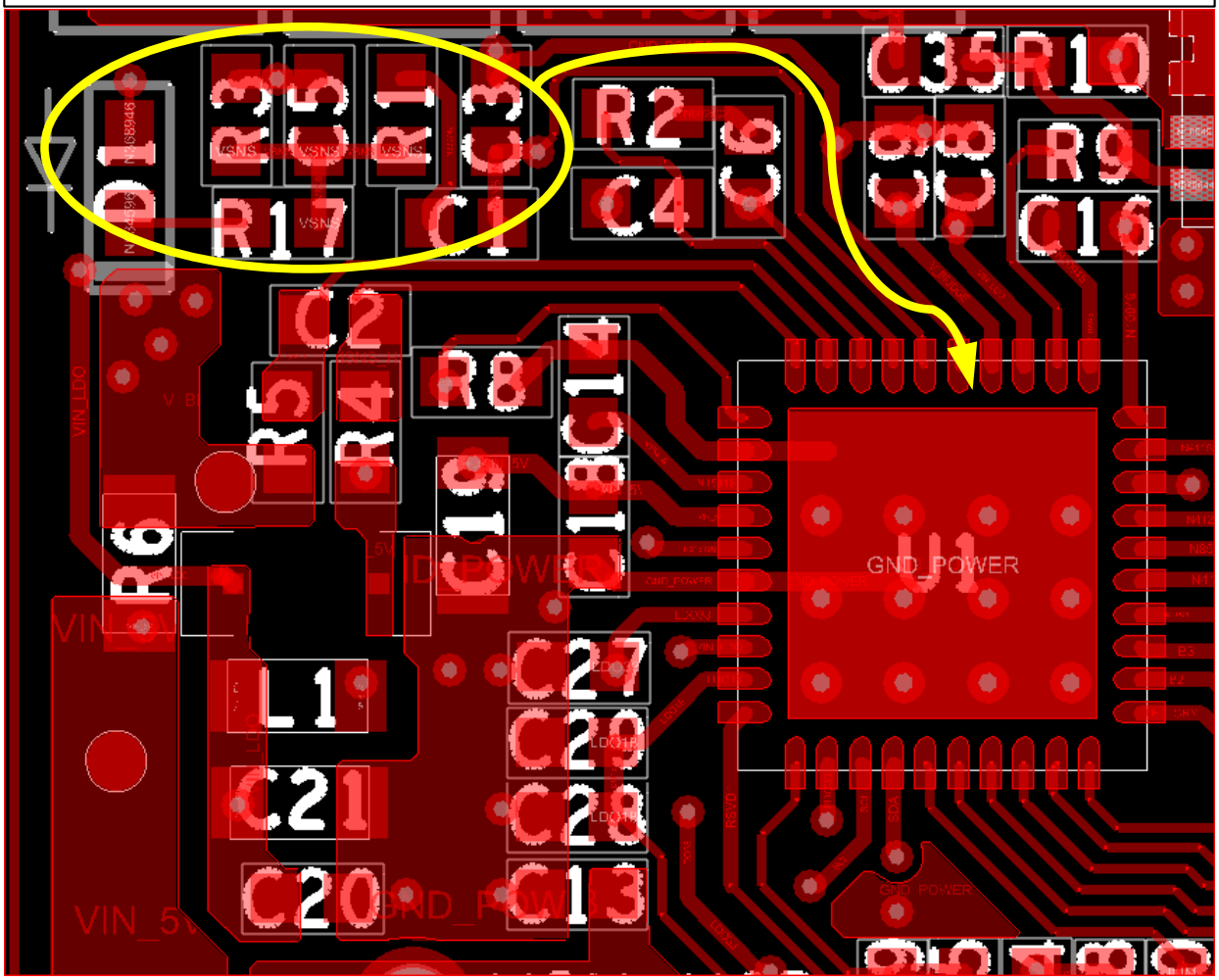
Rsense (R6), RC filter (R4, 5; C2), and the related pins (ISNS_H, ISNS_L) are all placed in close proximity and tightly coupled.

Voltage Sense Demodulation

Place the voltage demodulation circuit components (D1, R17, R3, C5, R1, C1, C3) tightly together and close to its related IC pins (VSNS_IN, VSNS_GND).

Figure 15. 9235A-R Top Layer – Voltage Sense and Demodulation Physical Placement

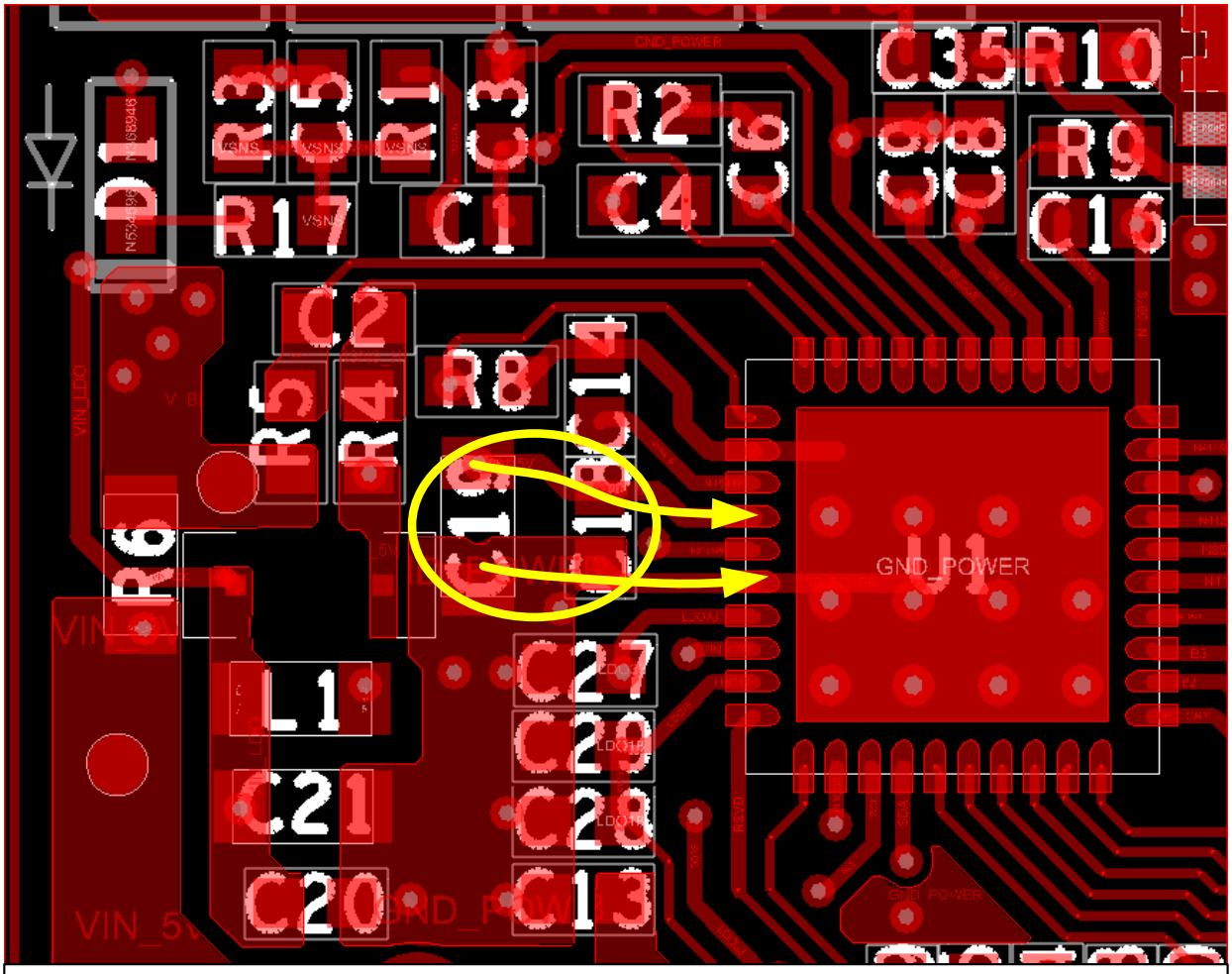
The voltage communication demodulation components (D1, R17, R3, C5, R1, C1, C3) are grouped tightly together and placed near their related pins (VSNS_IN, VSNS_GND).



Buck Regulator Component Placement

Place the buck regulator input capacitance (C18, C19) as close to the related pins (VIN, GND_B) as possible. These components see instantaneous switching between full load and no load causing noise issues if these traces are not as short as possible.

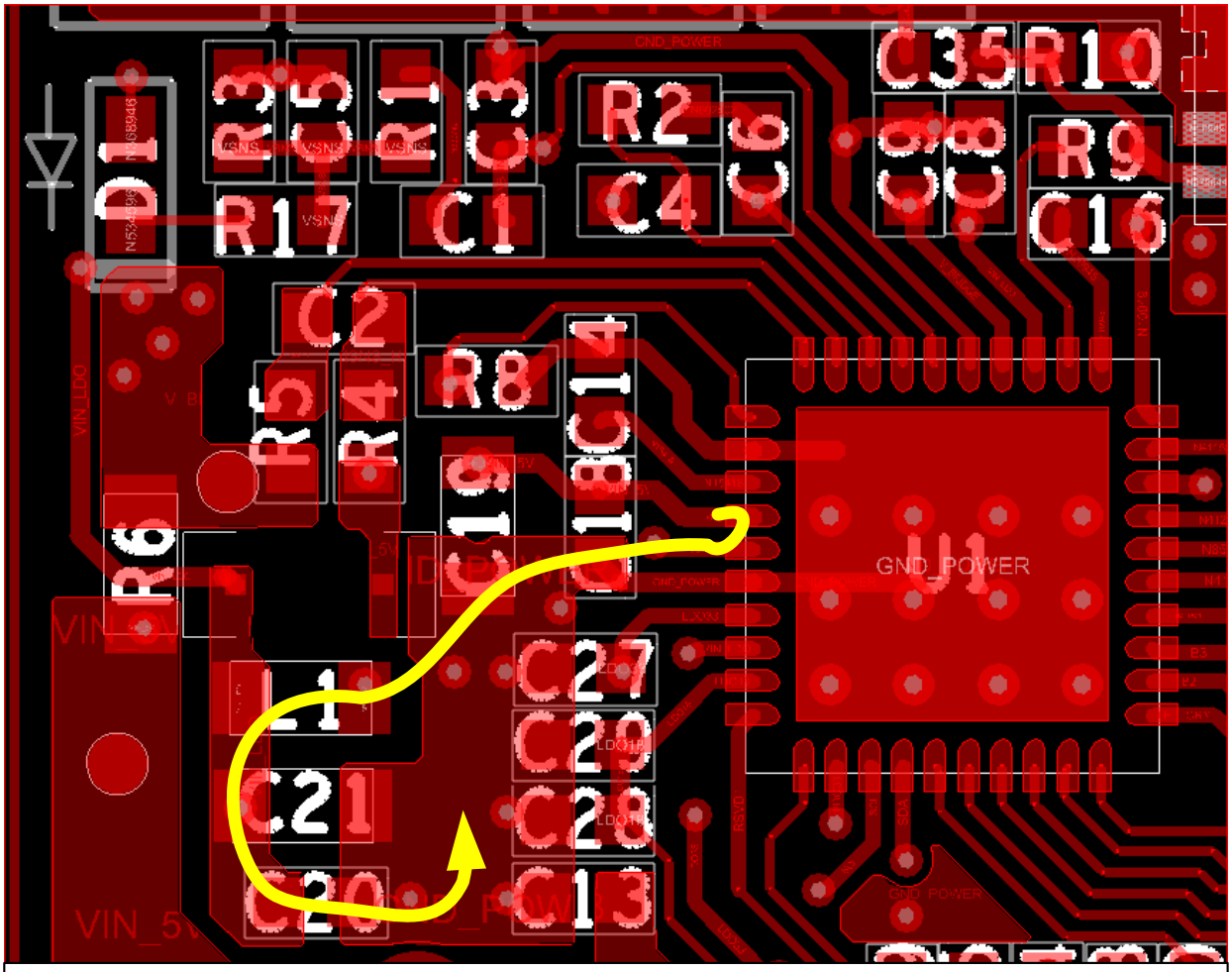
Figure 16. P9235A-R Top Layer – Buck Regulator Cin Physical Placement



Buck Regulator Cin (C18, C19): It is very important to place the input capacitance as close as possible to the related pin (VIN) to insure the smallest AC current loop and the shortest traces. The current in these traces instantaneously switches between full and no current causing noise issues unless these Cin are tightly coupled to the input voltage pin (VIN) and ground power pin (GND_B).

Place the buck regulator inductance and output capacitance such that they form the smallest possible current loop to minimize EMI transmissions (L1; C20, 21).

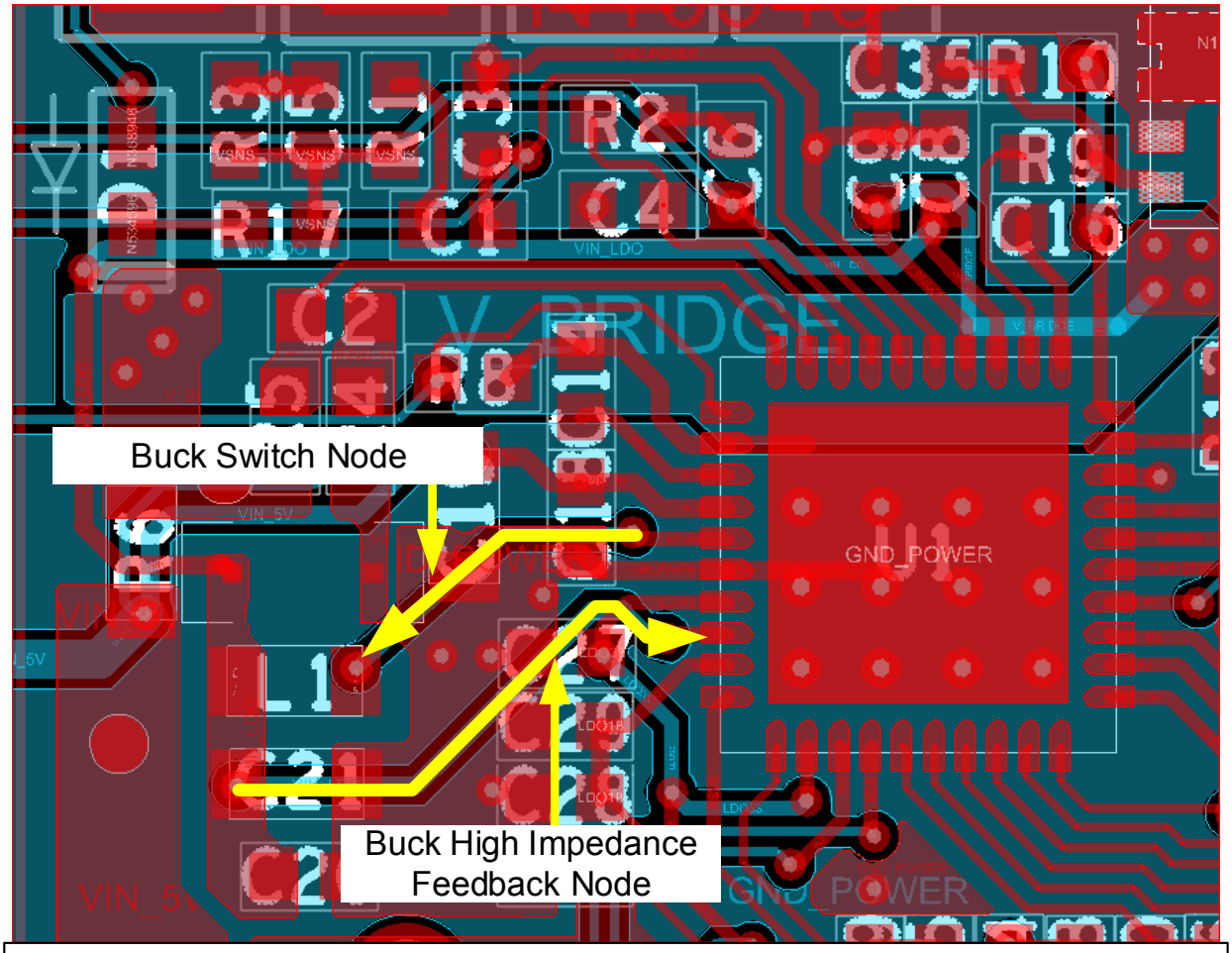
Figure 17. P9235A-R Top Layer – Buck Regulator L, Cout Current Loop



Buck regulator current loop is small and the traces are short.
Components (Cin: C18, C19, L1, Cout: C21, C20) are placed to insure the smallest AC current loop and the shortest traces.

Keep the buck switch node away from the high impedance feedback node. If needed to route under another node then route under the buck's Vin node.

Figure 18. P9235A-R Top Layer –Buck Switch Node Routing

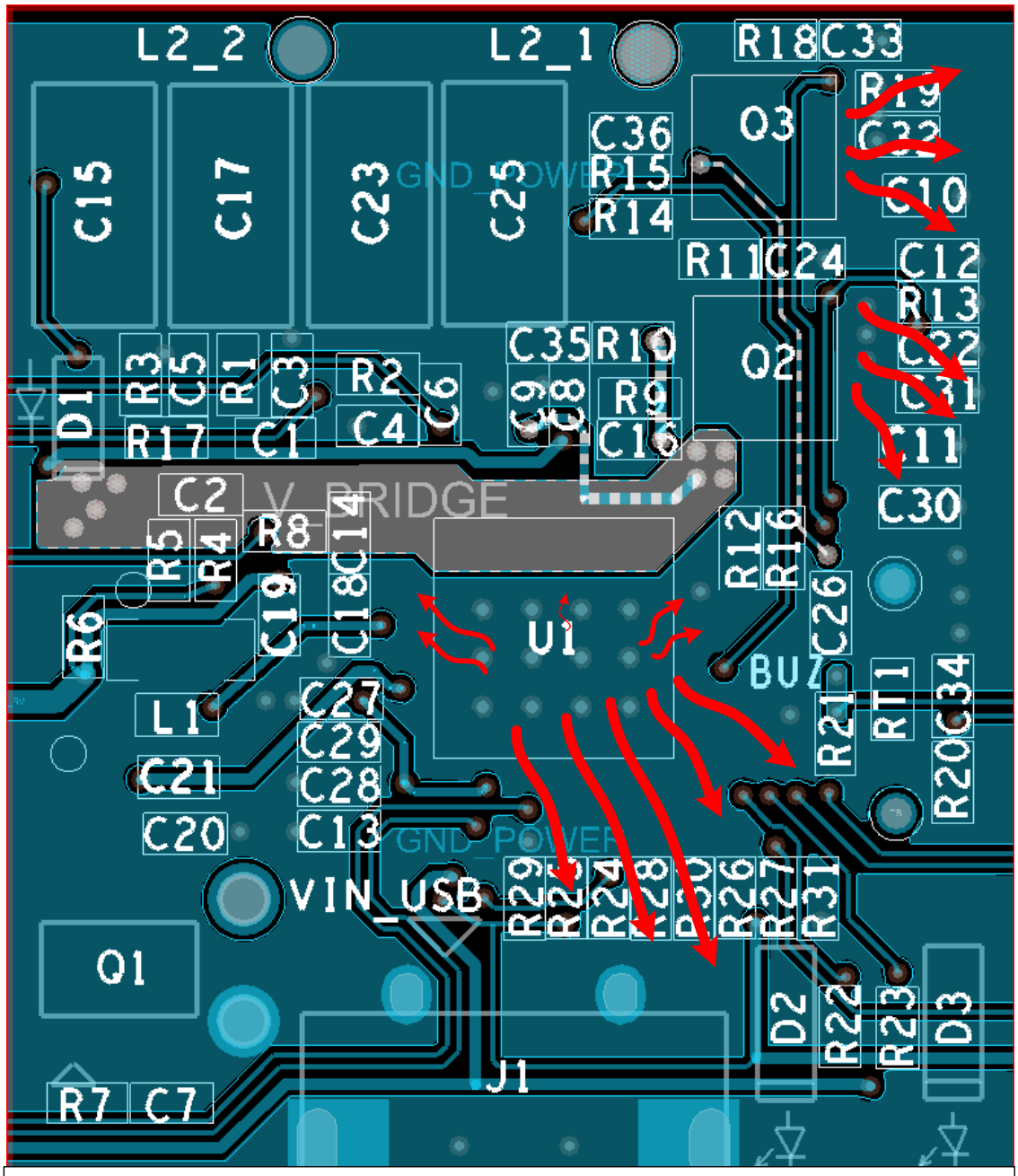


The buck regulator switch node only passes under the ground plane. This node is noisy, keep it away from the feedback node as in this example.

Ground – Thermal Requirements

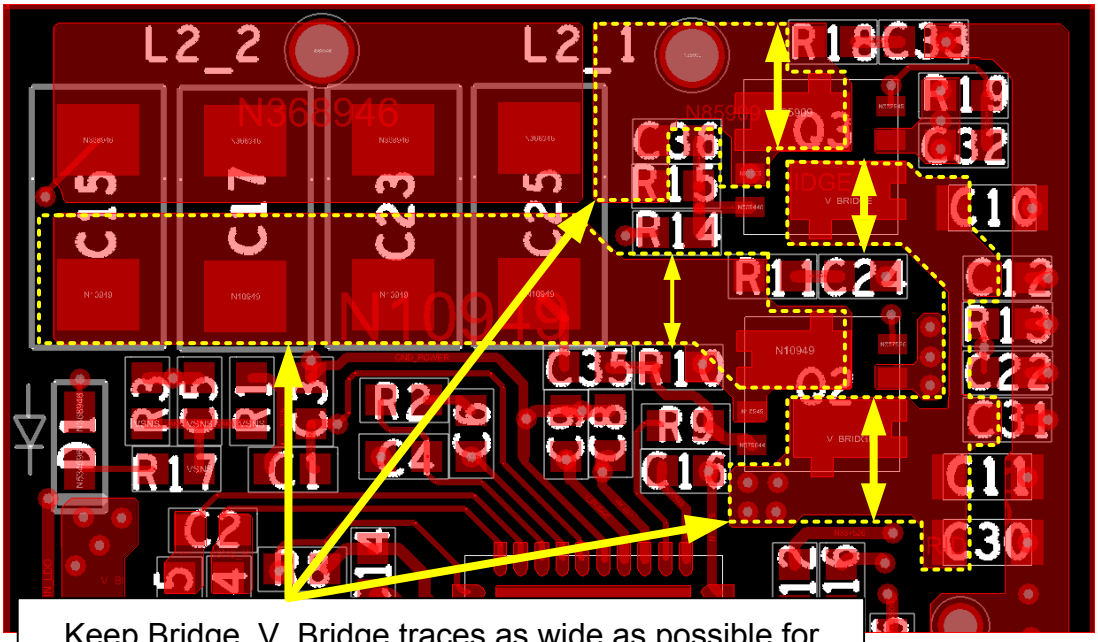
Keep the ground plane below the external FET pairs (Q2, Q3) and below the P9235A-R IC as intact as possible. This will improve thermal performance as a solid ground plane will allow heat to leave the IC much more effectively than a fragmented ground plane.

Figure 19. P9235A-R Solid Intact Ground Provides the Best Thermal Performance.



The solid cooper GND poor under the external FETs (Q2, Q3) and below the IC create an effective heat sink for quick heat removal from the IC area.

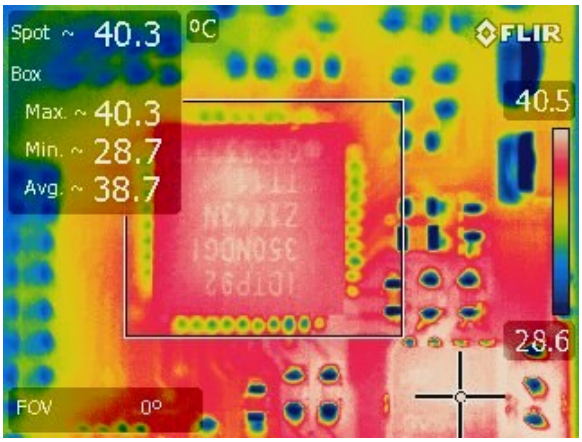
Figure 20. P9235A-R Wide Power Traces for the External FET Pairs Provide the Best Thermal Performance.



Keep Bridge, V_Bridge traces as wide as possible for thermal dissipation. These traces carry significant current.

Figure 21 shows the P9235A-R delivering 2W to a receiver. Notice the maximum temperature is 40.3°C. The ambient temperature is 25°C.

Figure 21. P9235A-R Thermal Image: Delivering 400 mA, 5 V (2 W) to a receiver.



Audible Noise Suppression

Wireless power transmitter solutions have been observed to produce audible noise. If sound is detected there are several steps that can be taken to reduce or eliminate the noise. The first priority should be identifying the source. It is recommended to use the recommended coils to avoid audible noise from the receiving coil.

When small form factor capacitors (0402) are used, it is more likely audible noise will be generated. This is due to the WPC communication signals being generated in the audible frequency range and the use of small form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors contract and expand while providing the communication pulses and this noise is amplified as it flexes the PCB.

The primary solution to this issue is to use low-acoustic noise capacitors. If that's not feasible, higher voltage rated components often have superior piezoelectric properties which can reduce the audible noise.

If swapping out the components is not possible, placing the capacitors on both sides of the PCB (directly above and below each other) can counter the piezoelectric forces applied to the PCB, thus eliminating the noise. Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. Lastly, some have reported success by placing additional lower-capacitance value components in parallel (such as eighteen 1 uF capacitors instead of four 4.7 uF capacitors) to reduce the mechanical force of the piezoelectric effect per component.

Revision History

Revision Date	Description of Change
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