Introduction

The 82P33x13 **S**ynchronization **M**anagement **U**nit (SMU) for IEEE 1588 and Synchronous Ethernet (SyncE) provides tools to manage timing references, clock sources and timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks. In its power-up default state the 82P33813 enables certain unused functional blocks that consume power. This application note describes the power dissipation of the 82P33813 in its power-up default state; and it describes how to disable the unused functional blocks and the power dissipation of the device after the unused blocks have been disabled. It also presents the power dissipation of 82P33813 for a typical configuration example.

Power-up Default State

Upon power-up, if there is no external EEPROM available, then the 82P33813 loads its register configurations from the metal defaults. The 82P33813, when configured as a master and with a 12.8MHz oscillator, will exhibit typical power dissipation as shown in Table 1.

Table 1. Typical Power Dissipation for 82P33813 with Power-Up Default Configuration

	3.3V/1.8V (Nominal VDD)		3.63V/1.98V (VDD+10%)	
Supply Rail	**Measured Current (A)**	**Power (W)**	**Measured Current (A)**	**Power (W)**
IDDA	0.322	1.064	0.323	1.173
IDDD	0.029	0.096	0.030	0.109
IDDD1p8	0.045	0.080	0.050	0.100
IDDDO	0.042	0.138	0.043	0.157
IDDAO	0.116	0.381	0.116	0.422
Total:		**1.759**		**1.962**

Disabling Unused Functional Blocks to Reduce Power Dissipation

The unused functional blocks in 82P33813 can be disabled and powered down by following the power-down procedure described below either by using the serial interface (I2C/SPI) or by configuring from an external EEPROM after reset:

Set the following control register bits to **1**:

Control Register bit 4 at offset address 0x381

Control Register bit 0 at offset addresses 0x330, 0x33C and 0x348

Control Register bit 1 at offset addresses 0x330 and 0x33C

This power-down procedure is automatically implemented by IDT's Timing Commander Software using the 82P33813 personality.

After powering-up in the default state and after implementing the power-down procedure, the 82P33813, when configured as a master and with a 12.8MHz oscillator, will exhibit typical power dissipation as shown in Table 2.

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Table 2. Power Dissipation for 82P33813 after Disabling Unused Blocks

	3.3V/1.8V (Nominal VDD)		3.63V/1.98V (VDD+10%)	
Supply Rail	**Measured Current (A)**	**Power (W)**	**Measured Current (A)**	**Power (W)**
IDDA	0.216	0.712	0.216	0.784
IDDD	0.030	0.098	0.029	0.104
IDDD1p8	0.049	0.088	0.056	0.111
IDDDO	0.029	0.096	0.031	0.111
IDDAO	0.059	0.195	0.060	0.217
Total:		**1.189**		**1.327**

Power Dissipation Example for 82P33813 in a Typical Configuration

The Timing Commander personality for 82P33813 disables all unused functional blocks to reduce power dissipation. The 82P33813 power dissipation for a specific application will depend on its configuration. Figure 1 shows an example 82P33813 configuration and Table 3 summarizes the power dissipation of this example.

Figure 1. Typical Example Configuration

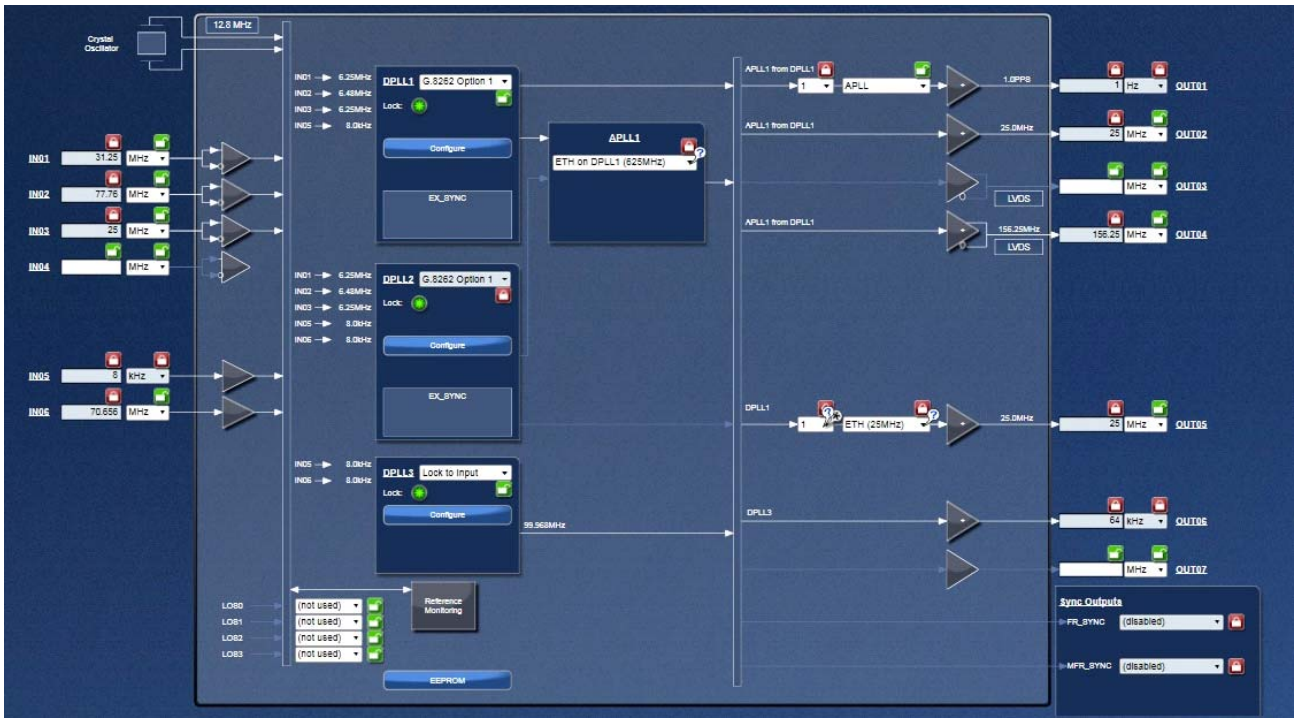

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Figure 2. DPLL Status for the Typical Configuration

Table 3. Power Dissipation for 82P33813 in a Typical Configuration

	VDD = 3.3V/1.8V (Nominal VDD)		VDD = 3.63V/1.98V (VDD+10%)	
Supply Rail	**Measured Current (A)**	**Power (W)**	**Measured Current (A)**	**Power (W)**
IDDA	0.214	0.707	0.215	0.779
IDDD	0.018	0.058	0.019	0.068
IDDD1p8	0.059	0.106	0.066	0.131
IDDDO	0.022	0.072	0.022	0.081
IDDAO	0.057	0.189	0.058	0.210
Total:		**1.132**		**1.269**

For questions related to device configurations, please contact IDT application support at support-sync@idt.com

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