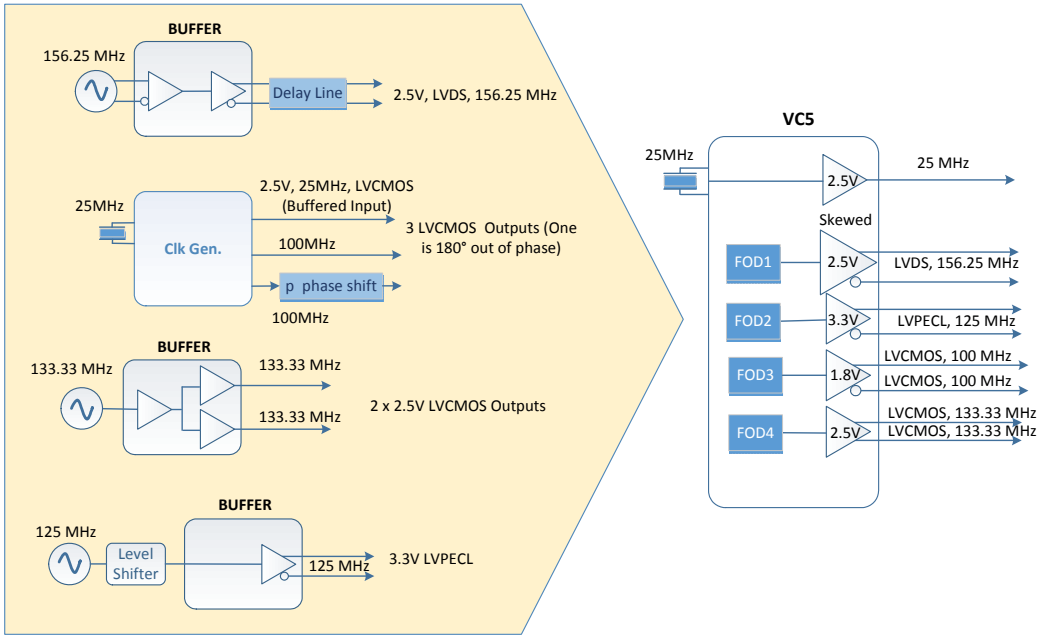
1 Introduction

This application note provides general layout design guidelines and recommendations for 5P49V5901/5P49V6901, IDT's fifth and sixth generation of programmable clock technology (VersaClock® 5/6). Although VersaClock 5/6 are the devices mentioned throughout this document, its coverage includes other devices such as VersaClock 3S (5P35021/23) – 3-PLL third generation of programmable clocks.

VersaClock 5/6 devices generate highly configurable outputs from a single reference clock that can be selected in a glitch free manual manner between two input clocks. Configurability includes spread spectrum, output termination as LVCMOS single or differential, standard differential LVDS, LVPLECL or HCSL as well as slew rate, loop bandwidth, and individual output enable. VersaClock 5 family of devices is intended for high performance consumer, networking, industrial, computing, and data-communications applications. Up to 4 different configurations can be stored and selected using two select pins or through I2C. VersaClock 5's excellent jitter performance enables it to land itself in a wide range of applications including PCIe Gen 1, 2 and 3, USB 3.0, 1 and 10 GbE applications. As shown in Figure 1, VersaClock 5 device family can enable a major BOM reduction and board simplification with not much more layout effort.

Figure 1. VersaClock 5 Replacing Multiple Timing Components



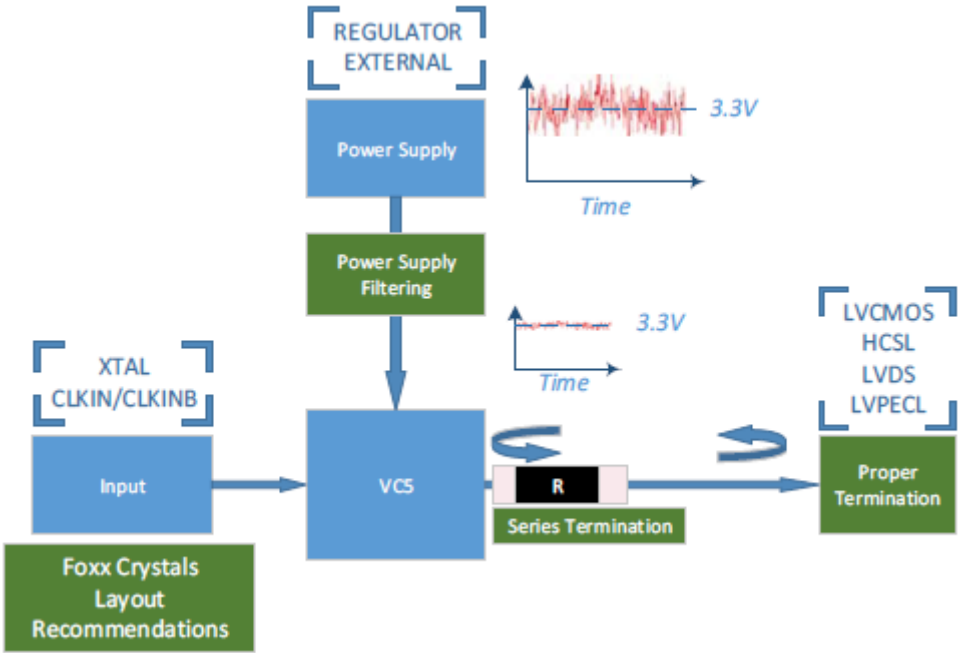
Single ended LVCMOS input reference and output frequencies can range from 1 MHz to 200 MHz. Differential (HCSL, LVPECL and LVDS) input reference and output clocks can range from 1 MHz up to 350 MHz. Although IDT recommends using 25MHz Crystal (see IDT 603-25-150), any fundamental mode Crystal from 8 MHz to 40 MHz can be used.

VersaClock 5 family offers multiple parts with different number of outputs. The 5P49V5923, 5P49V5925, 5P49V5927 provide options for up to 3, 5, 7 and 9 single ended LVCMOS outputs. An integrated Xtal version of VersaClock 5 is also offered with the 5P49V5933 and 5P49V5935 devices. Other devices with more configurable outputs satisfying the performance requirement of PCI-Express and various applications such as 1 Gb and 10 Gb Ethernet, PCI-Express Gen 1/2/3 etc. are available, such as 5P49V5907 and 5P49V5908. To accommodate these frequency ranges, few principles and recommendations are provided when designing VersaClock 5 clocks into a printed circuit board for best results.

In this document, we will discuss some layout recommendations and best practices in designing PCB planes and traces with IDT clock devices in general and VersaClock 5 generation in particular, to ensure solid pathway to power system and good signal integrity and hence get the best performance out of IDT Clock devices. These best practices and recommendations land

themselves into three major areas as illustrated in Figure 2: power supply filtering, signal trace and terminations as well as crystal input reference and quality crystal sourcing recommendations for optimal performance.

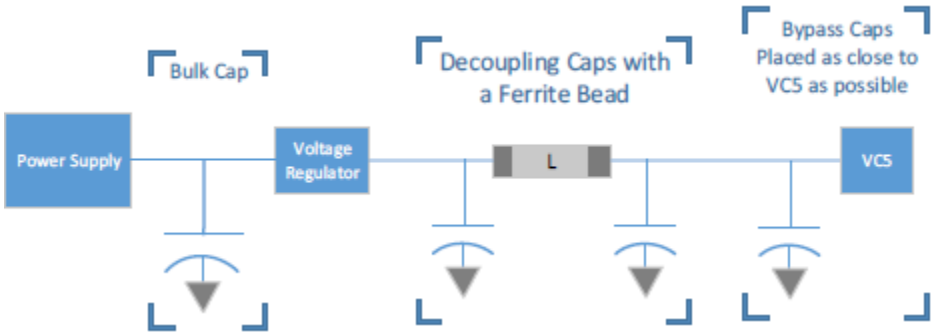
Figure 2. Block Diagram of the Three Categories Covered in the Application Note



2 Power Supply Filtering

Power filtering is one of the most important measures to prevent power supply noise from coupling to the device outputs, adversely affecting performance, especially when using switched power supplies. IDT recommends power supply filtering with a parallel combination of Bulk, decoupling and bypass capacitors as shown in Figure 3. In this section, the roles of different filtering caps will be briefly outlined.

Figure 3. VersaClock 5 Power Supply Filtering Block Diagram



2.1 Bulk Capacitance

These are usually large size capacitors. Their benefits include limiting supply surge currents.

2.2 Decoupling Capacitors

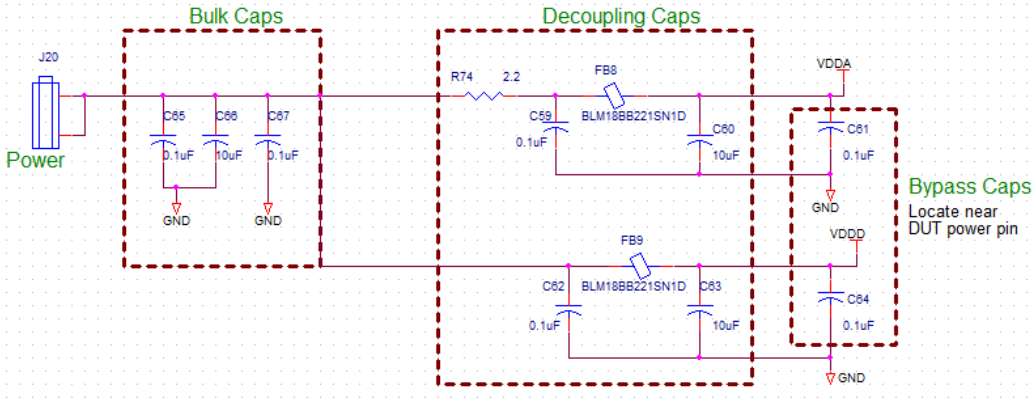
Multiple types of regulators (Linear and Switching) are often used to shift voltage levels and to reject power supply ripple and provide a clean power to the device. Power supply decoupling is achieved with a ferrite bead (or a resistor) and capacitors forming a pi-low pass filter topology (as shown in Figure 3). The benefits include:

- Preventing the transmission of noise from power supply to the device
- Acting as a low pass filter
- Assisting the bypass role

2.3 Bypass Capacitors

Bypass caps, often small size caps and placed close to the device, are used to shunt the high-frequency noise to ground.

Figure 4. Isolating VDDA and VDDD in VersaClock 5

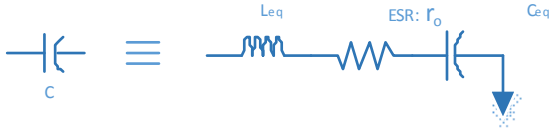


Because of their ubiquitous presence in circuits, it is important to understand the frequency response of a capacitor over a wide range of frequencies.

2.4 Capacitor Model

In light of the structure of the capacitor, an intuitive model would suggest a series inductor (leads), a series resistance associated with the leads (unless the connections are made out of supra-conductors) and a 2-plate capacitor. Having a good understanding of the capacitor model will help grasp their use, the filtering role they play, and will allow better power supply filtering.

Figure 5. Capacitor Model



$$C = r_o + j\left(\omega L_{eq} - \frac{1}{\omega C_{eq}}\right) \qquad (1) \qquad (2)$$

Examining equation (2), at low frequencies both r_o and ωL_{eq} are negligible in front of the quantity $\frac{1}{\omega C_{eq}}$ which rolls off at -20 dB/decade.

The frequency at which resonance occurs $\omega L_{eq} = \frac{1}{\omega C_{eq}}$ or $f = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}}$, the capacitor looks just like r_o.

Above this frequency, ωL_{eq} starts dominating with a positive 20 dB/decade growth as shown in Figure 6 below illustrating an example for C=0.01µF, Leq: (1,5,10)nH and r_o = 0.1Ω resulting in f_r =50.82*MHz* and Min(Mag) =10Log_{10}(0.1) = -23.01 for Leq=1nH.

Figure 6. a) Log plot of the complex impedance of a 0.01µF, 2W and 1µH Capacitance model b) zoom into the resonance 20log(2)=6dB

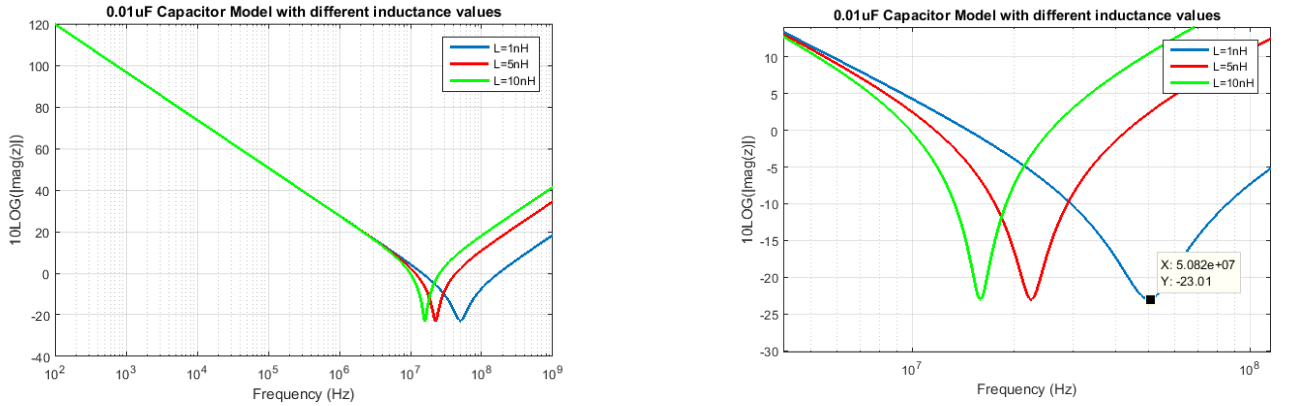


Figure 7 and Figure 8 show the role of each element in the power supply filter. These graphs show that designing power filtering for various purposes is possible. Examples are attenuating a specific frequency component or providing modest spread attenuation over a wide frequency range.

We recommend to place bypass capacitors as close to the device as possible. Figure 6 illustrates the effect of increasing the parasitic inductance of the capacitor model (for a copper micro-strip it's about 1nH/mm trace). The resonance frequency above which the capacitor starts acting like an inductor drops.

To remove high frequency energy that may be present on the supply lines due to various sources, Ferrite beads are recommended in line with the filtering capacitors. These can be seen as high frequency resistors (attenuators) that can allow DC to pass while absorbing the RF energy, dissipating it in the form of heat.

Figure 7. Ferrite Bead's Role along with 3 other Capacitors (varying R and C1)

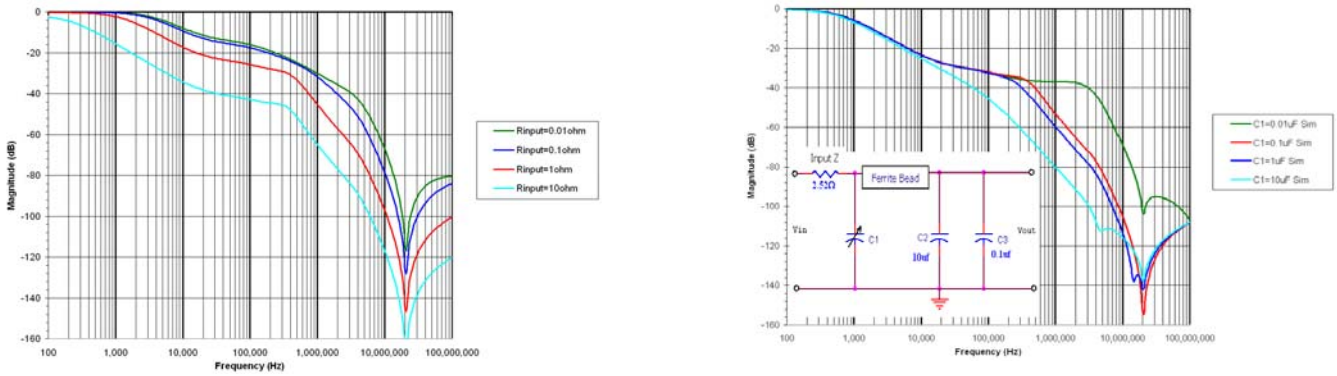


Figure 8. Ferrite Bead's Role with 3 other Capacitors (varying C2 and C3)

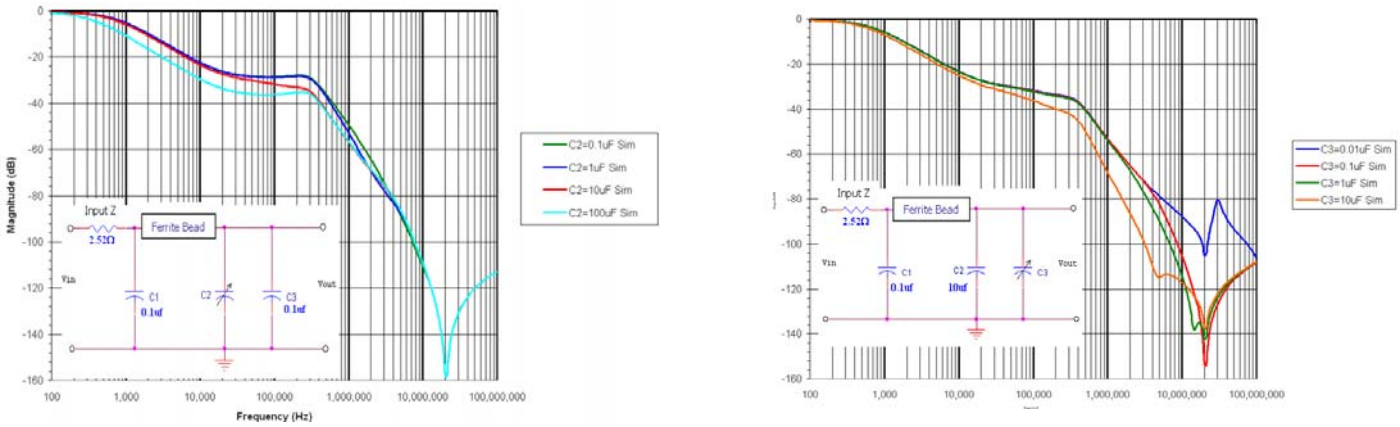


Figure 8 illustrates the importance of a ferrite bead the device power filtering. Ferrite Bead advantages include:

a. High impedance values removes a broad range of RF energy
b. Closed magnetic circuit eliminating cross talk
c. Inherent shielding
d. Great current carrying capacity
e. Spurious circuit oscillations are reduced because of their resistive feature to RF energy
f. Great selection of frequency ranges and resistance values

In order to choose the proper bead to use, the following are items that should be considered:

a. Range of unwanted frequencies on the power supply
b. Source of EMI contamination
c. Amount of contamination
d. Size and real estate depending on application
e. Typically, their impedance is specified only at 100 MHz, but the board designer should consider studying several graphs from the datasheet to properly select the right bead.

VersaClock 5 has multiple power pins; digital circuitry supply VDDD and analog PLL power supply VDDA. It is important to provide a degree of isolation so noise emanating from the digital supply will not pollute VDDA and prevent negative impact on PLL performance.

Figure 9. Power Filter Impedance with Individually Varying each Component

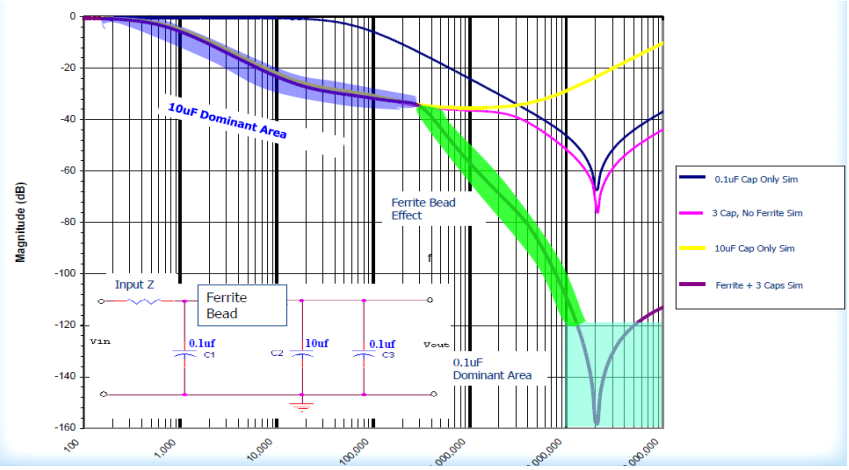
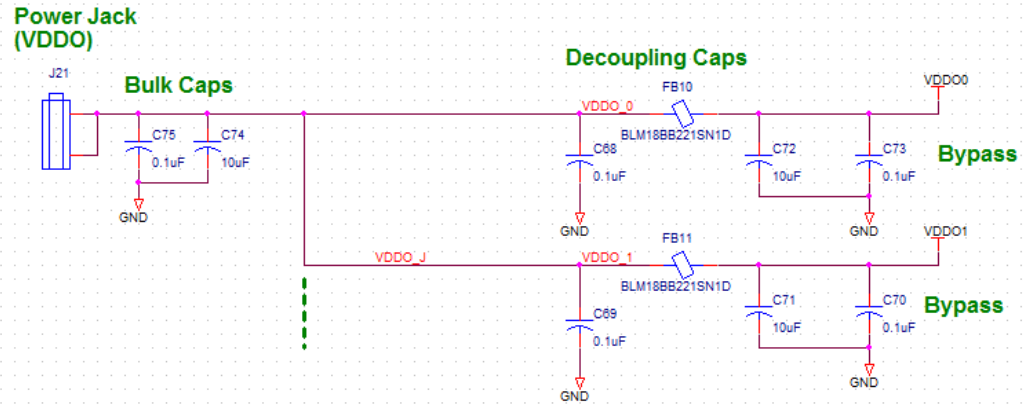


Table 1. Recommended Ferrite Beads for VersaClock 5 Power Supply Filtering

Manuf.	Part Number	Z@ 100MHz	Pkg Size	DC Res.	I (mA)
muRata	BLM18AG601SN1	600	0603	0.50	200
muRata	BLM18BD601SN1_PB	600	0603	0.65	200
Ceratech	HB-1T1608-601	600	0603	0.50	200
TDK	MMZ1608R301A	300	0603	0.20	500

Figure 10 shows an example of deriving VDDO [0, 1…] from a single supply source.

Figure 10. Output Clk0 VDD (VDDO0)



2.5 Methodology for Computing Bypass Values to use

In this section, a methodology to figure out the bypass capacitance to use is outlined. The method depends on multiple board/design specific parameters such as total number of gates (output drivers and buffers), wiring trace length the device, slew rates, load caps of the outputs, etc.

Assume that:

- VersaClock 5 shares VDD with other circuitry,
- The number of switching gates is N=30 (output buffers and drivers)

- The average amount of load capacitance per driver is 20 pF
- The average slew rate is 3 ns
- Inductance, L, for the wiring of the power supply to the DUT is known to be 100 nH
- Assume a power supply of 3.3V and a noise margin to be Vn = 100 mV which is the maximum tolerated noise level

Then the methodology outlined in “Appendix A: Methodology for Computing Bypass Values” shows that a 4.7 µF bypass cap is needed for power supply operating frequency above 241 kHz. With an ESL (Equivalent Series Inductance) of 1 nH, this capacitor is effective up to 24.1 MHz.

3 VersaClock 5 Inputs

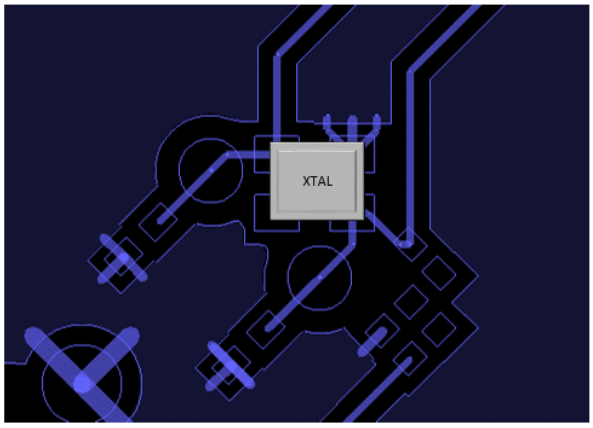
VersaClock 5 has two input reference options. Refer to the datasheet on how to multiplex between Xin/Xout Crystal input or an external differential input.

3.1 Xin/Xout

Xin/Xout are the crystal oscillator circuit interface pins. The following recommendations should be kept in mind when using a crystal:

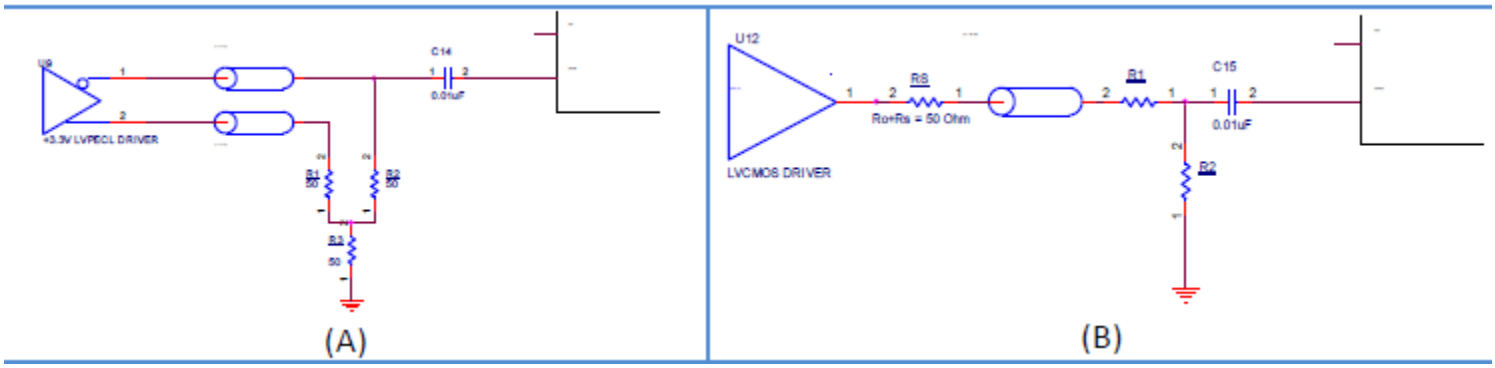
1. Place the crystal as close as possible to the crystal pins on the IC to minimize crystal trace length, in order to minimize parasitic capacitance and interference. For the same reason, avoid using vias in the crystal traces.
2. When using capacitors on each crystal pin to set the load capacitance value, connect the ground side of the two capacitors close together and close to the ground connection of the IC ground. The reason is to minimize noise coupling from the ground plane.
3. With on-chip capacitors, for making a load capacitance of 8pF or larger, it is preferred to use a crystal with that load capacitance to avoid using external capacitors.
4. Treat crystal component area as a keep out area for signal routing on other layers.

Figure 11. Example of a Crystal Footprint



5. Follow the directions for the load capacitance in the datasheet. A load capacitance mismatch results in a frequency offset (refer to the VersaClock 5 Evaluation Board User Guide). Also, higher load capacitance values mean lower oscillator gain so when adding external capacitors, be careful not to exceed the maximum load capacitance in the datasheet to assure enough oscillator gain margin. Refer to the datasheet and VersaClock 5 programming user guide) for proper way of setting the internal load capacitance values).
6. Route Xin and Xout traces as non-coupled high impedance traces. Separate them by at least 3 times the trace width.
7. Xin pin can be driven by a single ended LVCMOS signal or one AC-coupled end of a differential pair, provided that the amplitude remain between 500 mV and 1.2V and a slew rate of at least 0.2V/ns. In this case, the internal load cap should be set to a minimum value.

Figure 12. Driving Xin Pin (A) LVPECL input, (B) LVCMOS Driver



A separate input buffer for a differential input is also available and can be multiplexed with the crystal inputs externally and through I2C.

3.2 IDT recommended Crystal for VersaClock 5

The following table summarizes IDT-recommended crystal characteristics:

Table 2. Crystal Recommendation for VersaClock 5 Product Family

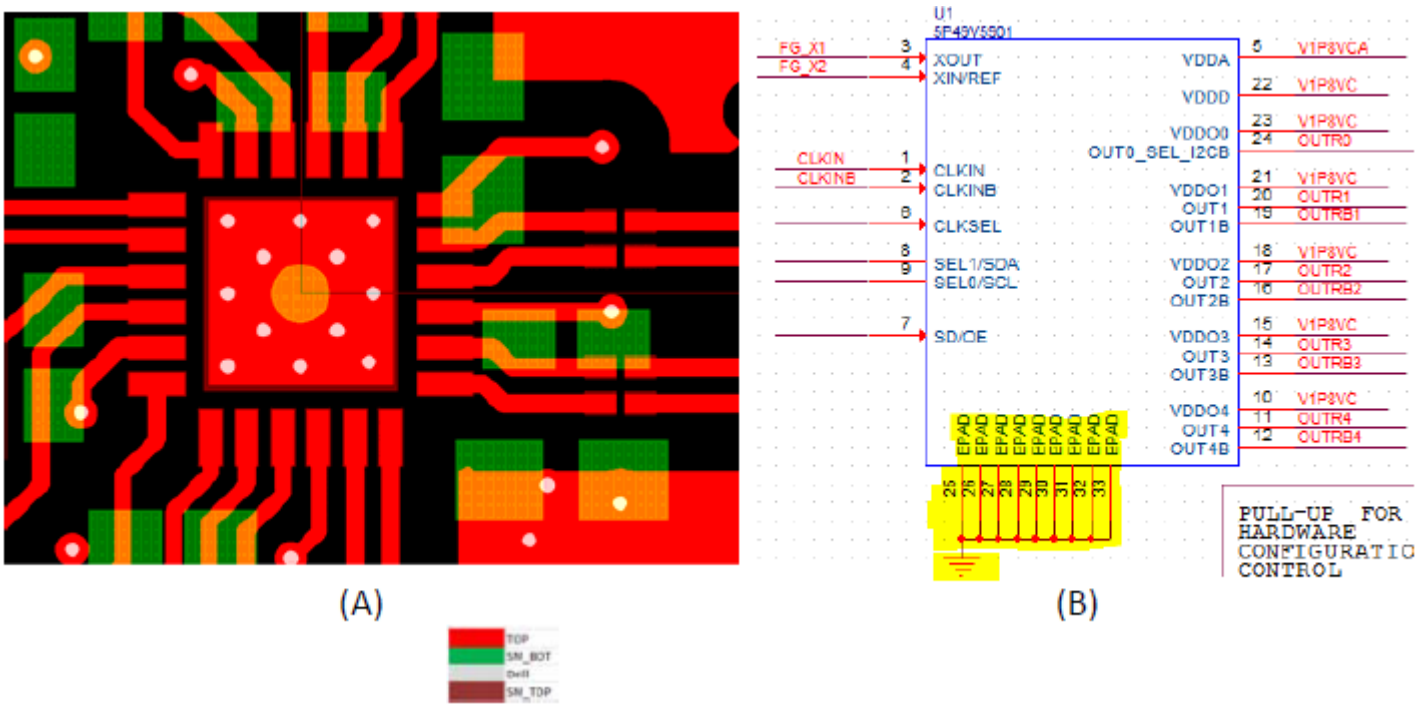
Feature	Recommended Value
Recommended Part	603-25-150JA4I
Frequency (MHz)	25
Frequency Tolerance @ 25°C	±20 PPM Max
Frequency Stability, ref @ 25°C Over Operating Temperature Range	±20 PPM Max
Operating Mode	Fundamental Mode
Load Capacitance (C_L)	8 pF
Equivalent Series Resistance (ESR)	50 ohms or less
Operating Temperature (°C)	Commercial: 0 to 70ºC Industrial: -40ºC to +85ºC

4 Device Electrical & Thermal Pad

IDT VersaClock 5 Frequency generators and buffers come with an Epad, a ground island directly beneath the device on the same layer the DUT is soldered on, which is to be connected to GND. Short traces are then drawn from there to the ground pin as shown in Figure 13. These traces should be made as wide as possible.

The ground island is then stapled with equally spaced vias to the inner ground plane as illustrated below in Figure 13. For more details on EPADs and Ground Vias, refer to Ref. [12] and Ref. [13].

Figure 13. (A) QFN package with a GND Island (B) Part Symbol

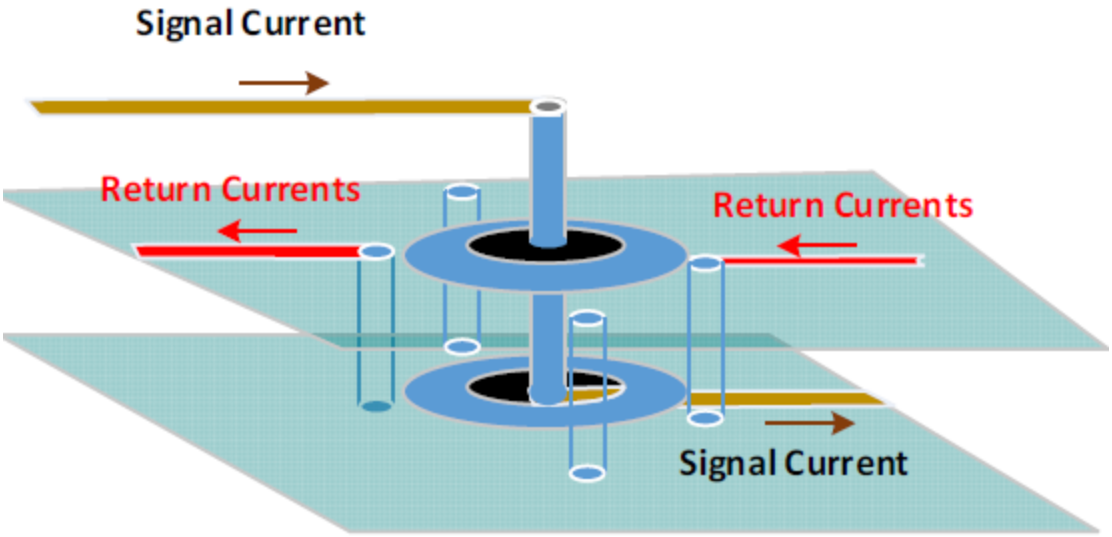


VDD traces are filtered with ferrite beads prior to the connection to the power plane. The ferrite bead and its associated bulk and decoupling capacitors should be as close to the power source as possible. Bypass capacitors should be placed as close to the device power pins as possible.

5 Recommendations for Optimal Return Path (cutouts in GND planes)

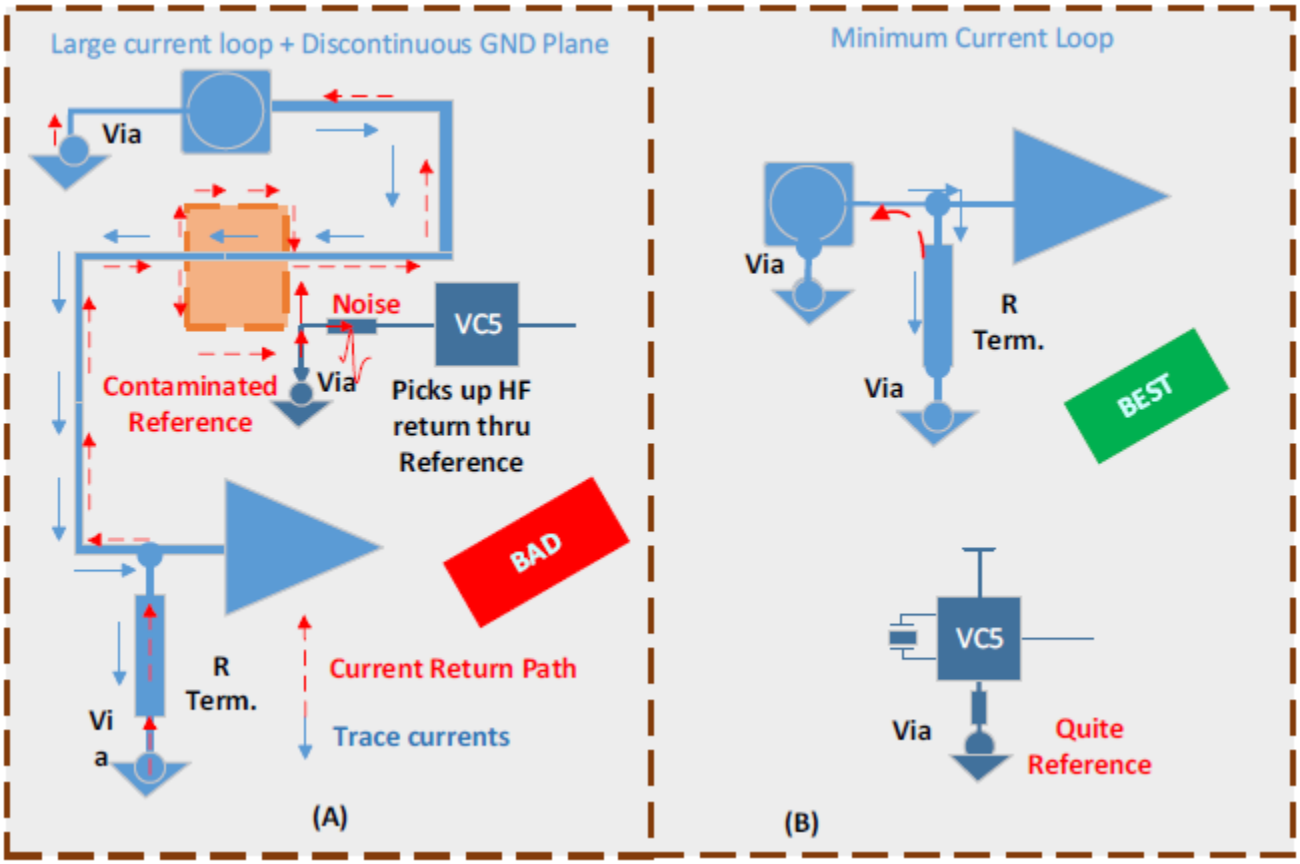
Considering their density, current return paths can be thought of as fictitious wires directly beneath or above the actual signal traces.

Figure 14. Signal Return Path



Hence, any obstruction to traces such as cutouts in GND plane (see Figure 15 A) should be avoided.

Figure 15. Illustration of Problems that can occur with Current Return Paths



These problems are those ghost issues, and often how up during new board bring up when the performance differs from that seen in simulations. Figure 15 illustrates this point.

6 Output Signal Integrity

VersaClock 5 output drivers can be configured for various output termination configuration; Traditional HCSL (see AN-879), LVDS, LVPECL and single ended or differential LVCMOS outputs. Details of these terminations are well documented and written about in other literature and are beyond the scope of this application note.

In order to avoid signal reflections, signal transmission lines must be terminated with an impedance equal to the transmission line characteristic impedance. A trace is considered as a transmission line whenever the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster). For example, a 2 inch micro-strip line, over a dielectric of $\mathcal{E}_r$ = 4.0, would have a delay of about 270 ps. Using the above rule, termination would be appropriate whenever the signal fastest transition time is less than 500 ps.

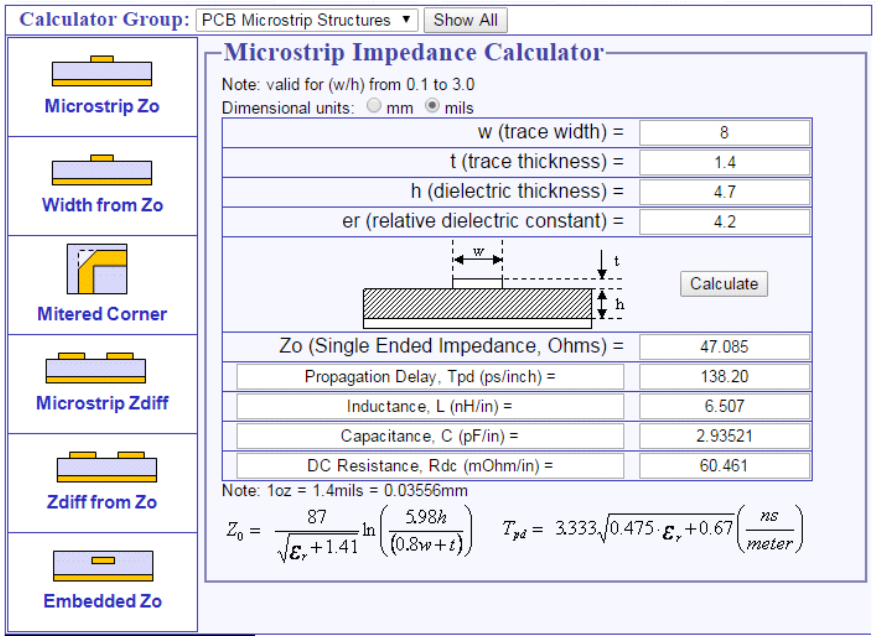
A 2 ns/ft. propagation delay (average between Microstrip and Striplines) is another conservative rule.

Stubs can be unterminated as long as their length (L(in)) does not exceed the signal rise time (tr(ns)) or when the prop delay has to be less than 1/3 of the 10% to 90% rise time. If multiple stubs are used to distribute the clock signal, all stub lengths must be made equal to avoid skew issues.

6.1 Trace Length Considerations

A question often arises: what is the maximum trace length can I drive with my clock? This question is not complete unless the type of the clock, frequency, trace geometry, type of PCB, the dielectric used (and so on) are specified. Figure 16 [Mantaro website] shows a calculation of r, L and C per inch for a micro-strip (see Ref. 13).

Figure 16. Transmission Line Distributed Parameter Calculation for a Microstrip



It is tempting to ignore L and C for the ranges of frequencies of VersaClock 5 and compute the resistive part of the trace impedance $(r = \rho L/A)$ and to figure out what length of that trace results in a 30% drop in voltage. This reasoning is incorrect because we would be using a lumped parameter formula to perform computations in the distributed model case.

The question is what is the maximum trace length of a trace before termination becomes crucial.

As a rule of thumb, this distance is given by [Ref. 3]:

$L_{max} = 9 \times t_r$ (Microstrip topology, in cm)

$L_{max} = 7 \times t_r$ (Stripline topology, in cm)

Where t_r is the rise time in Nano-seconds. If possible, layout the traces below these max limits. Reflections would be significantly reduced.

For example, for a 300 ps rise time, the maximum unterminated Microstrip trace is: 9x(0.3) = 2.7 cm and 7x(0.3) = 2.1cm for a Stripline trace.

For traces above this max value, the clock can drive very long traces, in comparison to the usual PCB dimensions, as long as proper recommended terminations are taken care of. Loss through PCB dielectric starts becoming significant in the Giga-Hz range, which is unlikely for VersaClock 5.

In very high frequencies, among other factors, dielectric dissipation (Df) is one of the major factor contributing to RF loss of signal. These are usually not the case in the frequency range of VersaClock 5 outputs. Insertion loss as a function of frequency, for different dielectrics, is well documented in the literature. This is usually given in dB/Inch and is typically less than 0.1 dBc/Inch for most dielectric constants and trace sizes. If we take this as a conservative limit, than in order to have 30% loss in the signal (3dB point), one would have to have a trace (3/0.05=60 inches). The day you have to lay a board with a 60 inch trace, you can worry about the trace length for the distributed case, otherwise, correct termination is the only thing one needs to concern oneself with.

6.2 Guidelines for Routing VersaClock 5 SE traces

- Keep clock traces as straight as possible. Use arc-shaped traces instead of right-angle bends.
- Do not use multiple signal layers for clock signals
- Do not use vias in clock transmission lines. Vias can cause impedance mismatch resulting in reflection.
- Place a ground plane next to the outer layer to minimize noise. If you use an inner layer to route the clock trace, sandwich the layer between ground planes.
- Properly terminate clock signals to minimize reflections

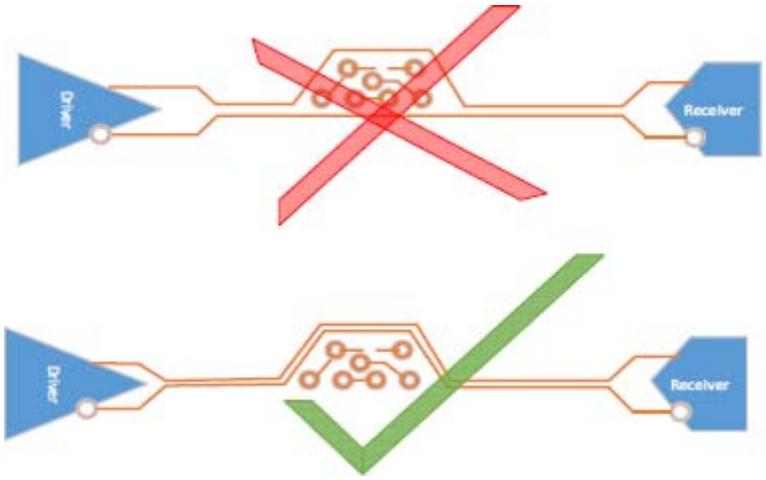
6.3 Routing VersaClock 5 Differential Traces

VersaClock 5 clocks are highly configurable. They feature 4 totally independent Fractional Output Dividers (FOD's). The output drivers can be configured for different types of termination including HCSL, LVDS, LVPECL or as two in phase or out of phase LVCMOS outputs. This section includes some guidelines to keep in mind when routing differential traces.

Differential traces should always be routed together (side-by-side). This keeps any noise injection into the signal a true common-mode noise which gets rejected by the receiver. If the differential traces part away from each other at any point, noise can only get into one line and not the other, hindering its rejection at the receiver. In addition, in order for the signals not to arrive at the receiver at different times which cause serious performance degradation, the lengths of both differential traces must be kept identical.

Figure 17 illustrates a scenario where it's attempting to deflect one trace from another to go around an obstacle.

Figure 17. Avoid separating differential line traces for any reason



6.4 EMI

Any conductor under certain conditions can become a great antenna. PCB traces are no exception to this aspect and can act as small antennas to the clock signals on the traces. This happens when the length of an unshielded conductor (trace) approaches and exceeds one tenth of the signal wavelength. Always take steps to minimize antenna effect and, hence, reduce Electro-Magnetic Emission (EMI).

EMI also happens when the signal's power is concentrated on a single frequency. VersaClock 5 allows spreading the signal energy over a certain frequency interval by virtue of Spread Spectrum available that can be turned on or off for each output independently.

7 Conclusion

It is not uncommon to design a board, simulate it, and have the highest confidence that the board will work when it comes back from production. When it does, bringing it up and debugging it gives its designer grief with some of the weirdest behaviors. Often times, these issues are caused by layout aspects, many of which are covered in this document and others in subsequent ones. These included traces, vias, power planes, ground loops, return paths, cross talk, radiation etc. Understanding these layout guidelines and some of the layout element behaviors at different frequencies will help designing more sound PCB boards, achieve greater performance, and decrease risks of multiple revisions.

Appendix A: Methodology for Computing Bypass Values

In this section, a methodology to figure out the bypass capacitance is outlined. The method depends on multiple board/design specific parameters such as total number of gates (output drivers and buffers), wiring trace length the device, slew rates, load caps of the outputs, etc.

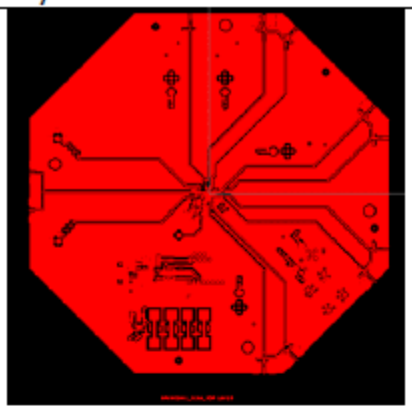
Assume that VersaClock 5 shares VDD with other circuitry, assume the number of switching gates to be (N=30 output buffers, and drivers) and the amount (average) load capacitance (e.g. 20 pF) each drives and the average slew rate it does it with (e.g. 3 ns).

Then, a good estimate of the inductance for the wiring of the power supply to the DUT is known (say L is 100 nH). Assume a power supply of 3.3V and a noise margin to be Vn = 100 mV which is the maximum tolerated noise level.

1. We compute the current (di) as $\frac{V_{CC}}{\left(\frac{dt}{nC}\right)} = \frac{nCV_{CC}}{dt}$, (dt is switching time). With the numbers chosen here, dI = 0.66 A
2. Compute the max impedance: $Z_{\max} = \frac{V_n}{dI} = 0.1515\Omega$
3. Compute the frequency above which power supply wiring needs bypass caps: $F_{psw} = \frac{Z_{\max}}{2\pi L} = \frac{0.1515}{2 \cdot 3.14 \cdot 100e^{-9}} = 241kHz$
4. If the operating power supply frequency is higher than 241 KHz, then a bypass capacitor is needed. That is calculated as follows:
5. $C_{bypass} = \frac{1}{2\pi F_{psw}} = 4.356\mu F$. Since this is not common cap, $4.7\mu F$ would do.
6. If the capacitor used has an ESL (Equivalent series inductance) of 1 nH, the max frequency up to which this value will work effectively can be computed as follows:

. $F_{bypass} = \frac{1}{2 \cdot \pi \cdot ESL} = 24.1MHz$

Appendix B: Board Layout

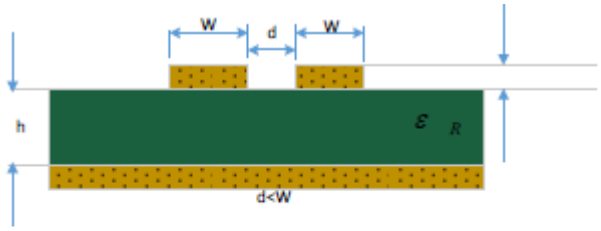
Typical Layer Stack up	Layer	Layout
1* ASSY.art 2+ L1_TOP.art 3+ L2_GND.art 4+ L3_POWER.art 5+ L4_POWER.art 6+ L5_GND.art 7+ L6_BOTTOM.art 8* PM_BOTTOM.art 9* PM_TOP.art 10* SILKSCREEN_BOTTOM.art 11* SILKSCREEN_TOP.art 12* SM_BOTTOM.art 13* SM_TOP.art 14* FAB.art	L1_TOP	
	L4_POWER	
	L5_GND	
	L3_POWER	

Appendix C: Impedance of Common Transmission Lines

Microstrip

This is the most commonly used layout. Microstrip lines have less propagation delay than their Stripline counterparts with the same dielectric material. Because Microstrips are on the outer layer (unshielded), they can radiate more RF to the external world. Their advantage is that only two PCB layers are required.

Figure 18. MICROSTRIP Differential Line Impedance



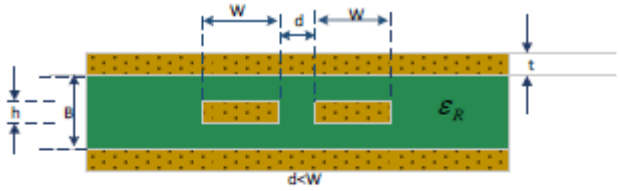
$$Z_{diff}(\Omega) \cong 2 \cdot Z_O\left(1 - 0.48e^{\frac{0.96d}{h}}\right) \quad (3)$$

$$Z_O(\Omega) \cong \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{6h}{0.8W + t}\right) \quad (4)$$

Stripline

Striplines are traces sandwiched or buried between two other layers. While these lines have better noise immunity/radiation, they exhibit more propagation delays. The drawback of this kind of traces is that they require at least 3 layers and may be harder to control Z_O.

Figure 19. Differential Line Impedance in a Stripline

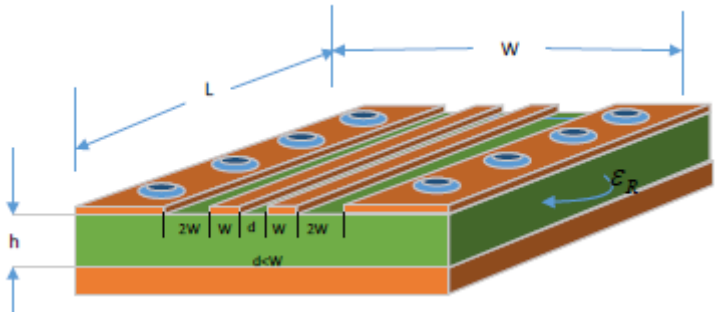


$$Z_{diff}(\Omega) \cong 2 \cdot Z_O\left(1 - 0.347e^{\frac{2.9d}{B}}\right) \quad (5)$$

$$Z_O(\Omega) \cong \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9h}{(0.8W + t)}\right) \quad (6)$$

In cases where ground pour is on the same layer as the differential pair, it's important to keep a distance at least twice the trace width from the ground. This minimizes the capacitance of the plane which can dramatically alter the characteristic impedance of the trace. To minimize current loop area, it is recommended, in this case to place vias on the ground copper pour to connect to the bottom ground layer as shown in Figure 20. The distance between vias should not be more than 0.1".

Figure 20. Running Differential Traces Surrounded with GND Layer



Trace Inductance and Capacitance

Figure 21 shows a trace running on the top layer of the PCB. A trace has both, inductance and capacitance, in addition to resistance, that are given by the following:

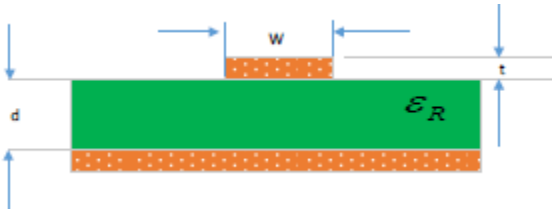
$$L(nH) = 2 \cdot x \cdot \ln\left(\frac{5.98h}{0.8W + t}\right) \quad (7)$$

$$C(pF) = 0.264 \cdot x \cdot \left(\frac{\varepsilon_R + 1.41}{\ln\left(\frac{5.98h}{0.8W + t}\right)}\right) \quad (8)$$

$$Z_0(\Omega) = 31.6\frac{L(nH)}{C(pF)}, \quad T_P(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

Where *X* is the length of the trace, W: Width of the trace, t: thickness of the trace, d: thickness of the dielectric material and ε_R is its relative dielectric permittivity.

Figure 21. PCB Trace Running on the Top Side of the Board



Example: A 0.8mm (0.031") copper trace on 0.8mm (0.031") thick PCB (FR-4) would show approximately 4nH and 0.8pF per cm trace (10nH and 2.0pF per inch) (FR-4: $(\varepsilon_R = 4.5)$

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