# 1 Introduction

82P33714/31 SETS (**S**ynchronous **E**quipment **T**iming **S**ource) and 82P33810/14/31 SMU (**S**ynchronization **M**anagement **U**nit) can be configured to implement a clock protection scheme for SYNC-E, SONET and SDH synchronization systems on the timing card. Two devices should be used together in order to:

- Enable system protection against single chip failure;
- Guarantee no service interrupt during system maintenance, such as software or hardware upgrade.

All SEC (**S**ONET/SDH **E**quipment **C**locks), EEC (synchronous **E**thernet **E**quipment **C**locks), and PEC (Packet-based Equipment Clocks) output frequencies are derived from internal PLL systems. The frequency being used for locking within the PLL will always be in phase lock. It is expected that an NE (Network Element) will use the T0 output for its internal operations. The phase of the outputs from the T4 path will not be aligned, unless the T4 outputs are locked to the T0 outputs. In many applications, the clocks supplied into the system are required to be aligned not only in frequency, but also in phase between the Master and Slave devices. This ensures minimal disturbance when any clock sink switches between Master and Slave.

# 2 Timing Card Master-Slave System Configurations

This configuration is used when the output SECs/EECs/PECs (& SYNC if required) from the two devices are required to track each other with a known phase alignment. The SEC/EEC/PEC and FRSYNC/MFRSYNC outputs from the device designated the Slave will track the SEC/EEC/PEC and FRSYNC/MFRSYNC outputs from the device designated the Master. This relationship is maintained even if all the external references fail and the Master enters holdover. This mode provides for output SEC/EEC/PEC and SYNC alignment between the Master and Slave.

To achieve a Master-Slave clock protection system, 82P33xxx (including 82P33714/31 SETS and 82P33814/10/31 SMU devices) provides both software and hardware Master & Slave modes.

## 2.1 Master–Slave Configuration

Master-slave mode can be configured by hardware or software (writing a register bit). Hardware master mode is the default setting for 82P33xxx. This mode is where all the settings of the device operate exactly as programmed when the MS/SL pin on the device is "high". Hardware Slave mode is entered when the MS/SL pin is driven "low". This is intended to allow external hardware monitoring and control to determine which device is Master and which device is Slave independent of the software configuration.

Master/Slave mode can also be individually controlled by software control when MS/SL pin is either "high" or "low". Software control is accomplished by writing register bit MS_INVERT (0x382, bit 0). The mode (master of slave) of the device is determined by a combination of MS/SL pin and MS_INVERT bit listed in the table below.

See Table 1 combination of hardware pin and MS_INVERT bit to determine device master/slave operation.

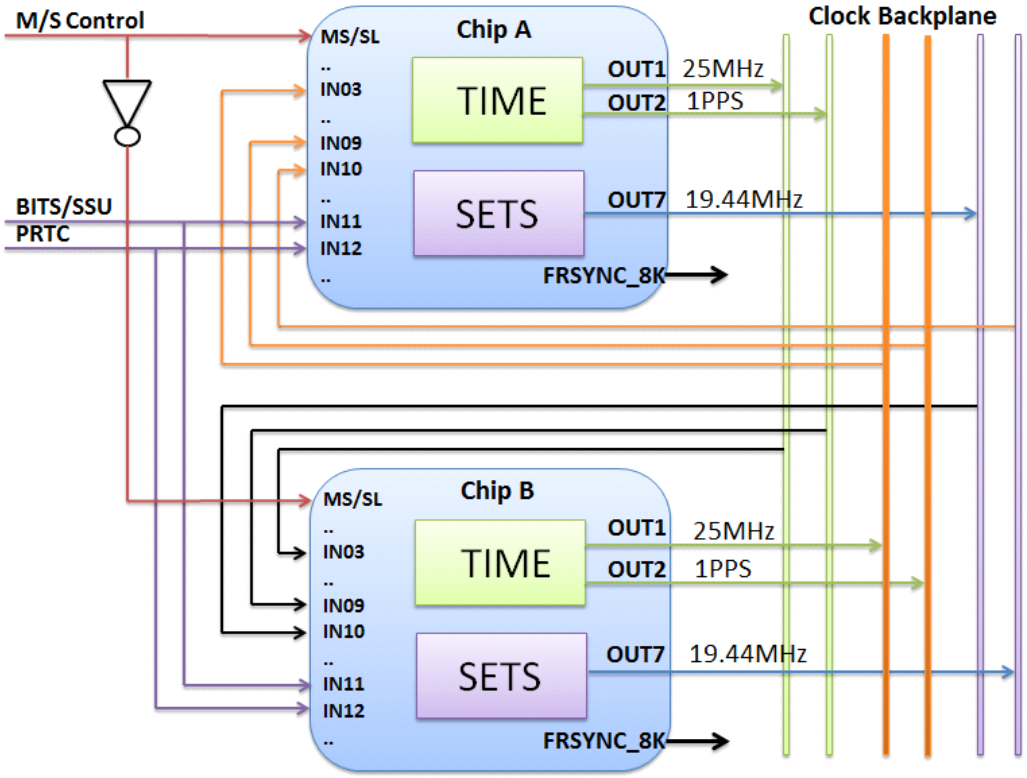
**Table 1: Combination of Hardware Pin and MS_INVERT Bit**

| Master/Slave Control | | Result |
|---|---|---|
| **MS/SL Pin** | **MS_INVERT** | |
| High | 0 | Master |
| | 1 | Slave |
| Low | 0 | Slave |
| | 1 | Master |

As indicated in Table 1, if register bit MS_INVERT is fixed at "0", then master or slave mode of a device is only determined by logic level of MS/SL pin: master when MS/SL = "1" and slave when MS/SL = "0". We refer this as hardware control of master/slave mode. Please note: MS/SL selection will apply to both DPLL1 and DPLL2 in 82P338xx. In other words, DPLL1 and DPLL2 will operate in master or slave mode per MS/SL selection of the chip. DPLL3 (T4), however, does not have master or slave capability.

A typical master/slave application scenario is illustrated in Figure 1 below, followed by device configurations in Master and Slave mode, respectively, in Timing Commander™ GUI window.

**Figure 1. Typical Setup for a Master/Slave Configuration**



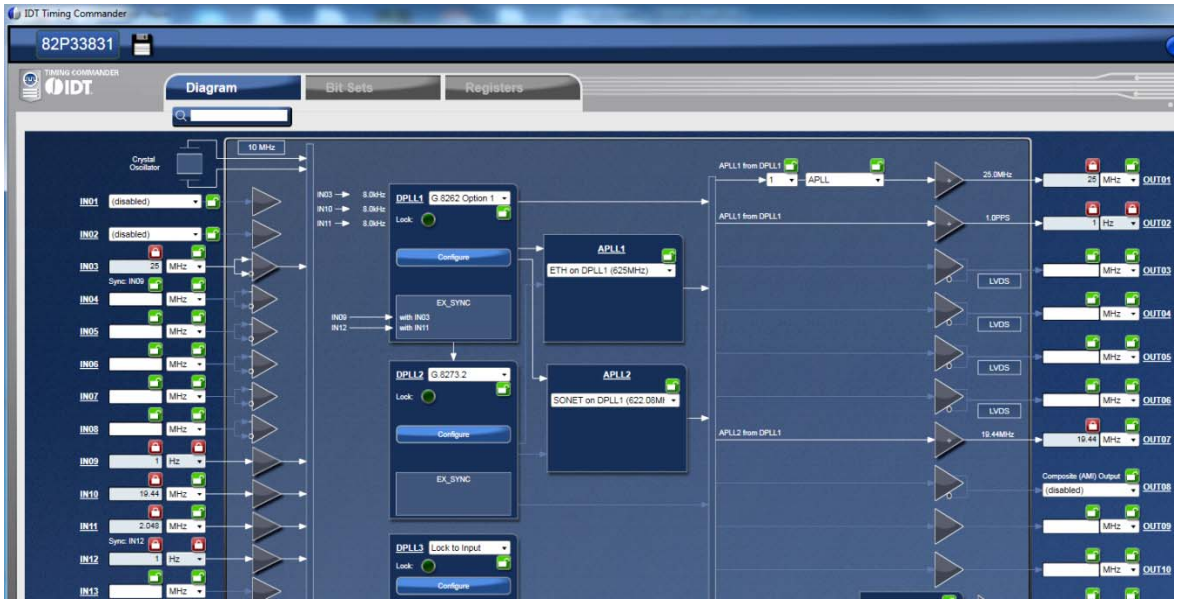

**Notes**: SETS = Synchronous Equipment Timing Source; TIME = 1588-based phase/time; BITS = Building Integrated Timing Supply; SSU = Synchronous Supply Unit; PRTS = Primary Reference Time Clock

In the above setup, specific reference arrangements are as the follows:

- BITS or SSU clock goes to IN11 of both chips as input clock when the device is in Master mode;
- A PRTC-referenced clock, i.e., 1PPS, goes to IN12 of both chips as SYNC input, that may be associated with each respective input clock (IN11), when the device is in Master mode;
- 25MHz and 1PPS are output at OUT1 and OUT2 from "TIME" (1588-path), respectively, from both devices;
  - 25MHz from OUT1 goes to IN03 of both chips as input clock when the device is in Slave mode;
  - 1PPS from OUT2 goes to IN09 of both chips as SYNC input associated with each respective input clock (IN03);
- 19.44MHz at OUT7 from "SETS" (Sync-E path) goes to IN10 of both devices as another input reference when the devices is in Slave mode;
  - FRYSNC_8KHz can optionally output 8KHz used as a Frame input associated with the SETS input clock (IN10). In this example, it is not used.

The input clock and Sync connections above are reflected in Timing Commander settings as shown below. When in Master mode, other inputs can be enabled with lower priority than IN11 as alternative inputs when IN11 fails. When in Slave mode, a forced input (IN03 in this example) is selected.

**Figure 2. Timing Commander Input and Sync Arrangements for an Application Scenario Illustrated in Figure-1**

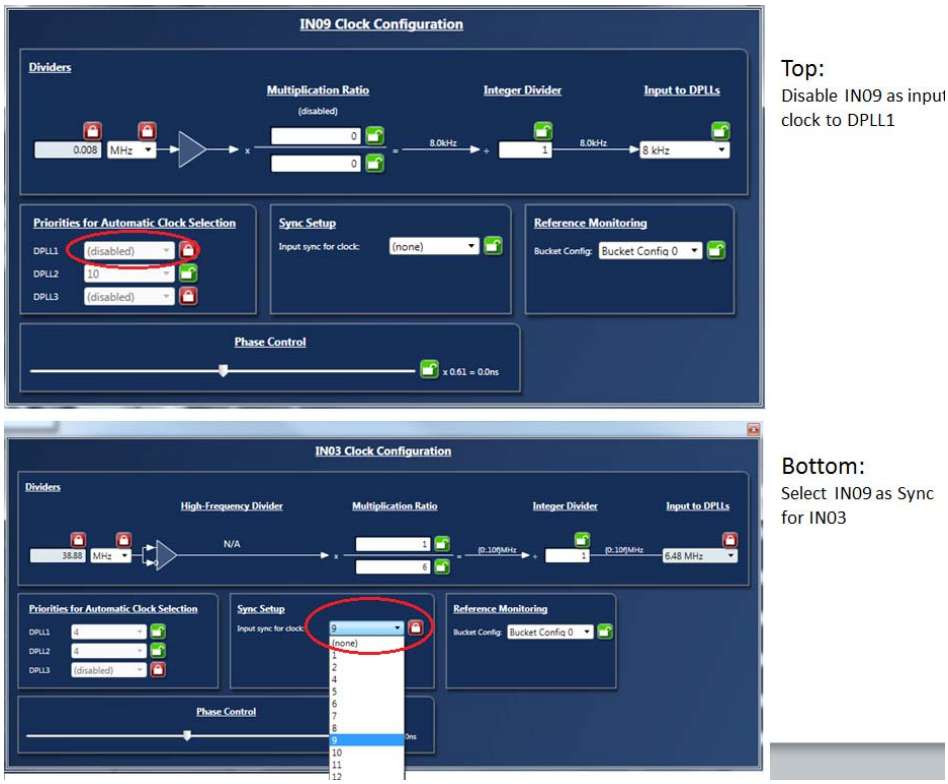



To associate a Sync input with an input clock, use the following two steps:

1. Disable the Sync as an input clock to the working DPLL (DPLL1 in this case).
2. In the Input clock configuration window, select the input where Sync pulse is connected to.

For example, to associate IN09 (used as Sync) with input clock at IN03, we first disable IN09 as an input clock to DPLL1 (DPLL1_IN09_PRIORITY, 0x11C, bits [3:0]). See **Top** of Figure 3 below for Timing Commander setting; then select IN09 in Sync Setup window for IN03 (IN03_SYNC_SEL, 0xB5, bit [3:0]). See **Bottom** of Figure 3 below for Timing Commander setting.

**Figure 3. Configuration Hints for Defining Input Clock and Sync Pulse**



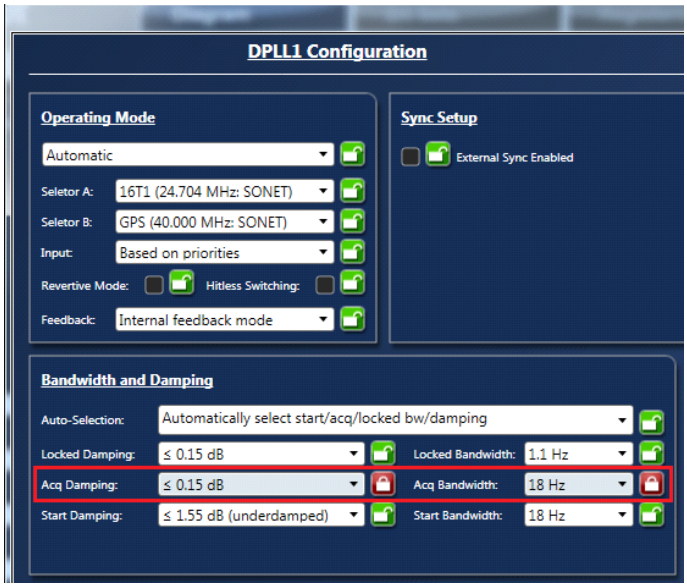

Similar operations are required to associate IN12 as a Sync pulse with input clock at IN11.

**NOTE**: By default, IN03 has a higher priority than IN11 which is meant as an input clock for the device when in Master mode. Thus, in order to ensure IN11 (and its associated Sync input in IN12) is selected when the device is switched to Master mode, IN11's default priority must be replaced by a priority higher than IN03. This can be done by setting priority register DPLL1_IN11_PRIORITY (0x11D, bits [3:0]) to a lower value than IN03, i.e., 0x0001. A lower value means a higher priority.

When in Slave mode, several settings are enforced (for more details, see Section 2.4, “Master-Slave Operation”):

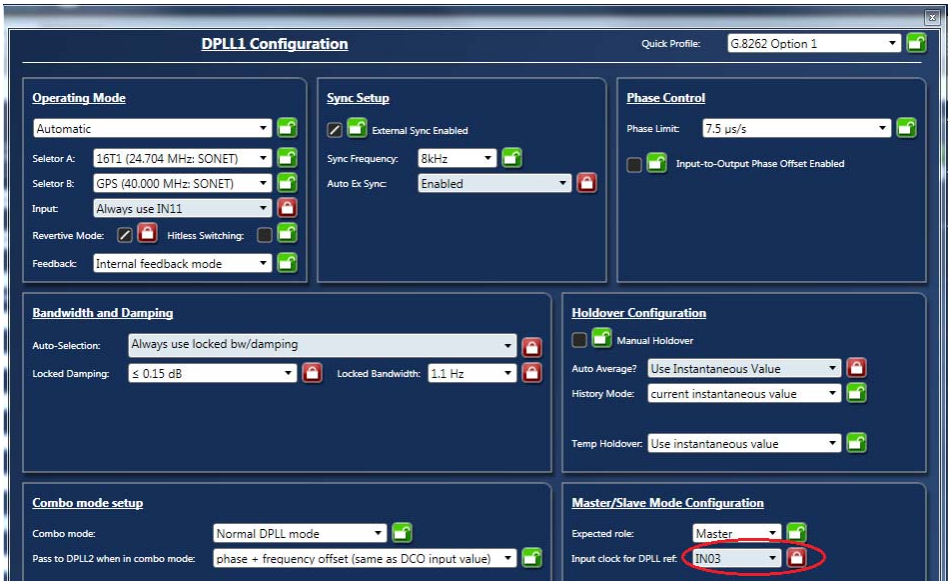
1. Hitless Switch is disabled (DPLL1_HITLESS_SWITCH_EN = '0', 0x117, bit 2).
2. DPLL loop is forced to select the acquisition bandwidth regardless of whether it is locked or not. It is recommended to set the acquisition bandwidth (DPLL1_ACQ_BW_DAMPING_CNFG, 0x125, bit [4:0]) at 18Hz and ACQ Damping (DPLL1_DLL_ACQ_BW_DAMPING_CNFG, 0x125, bit [7:5]) at 0.15dB to allow the Slave PLL to track the Master PLL outside of the wander filtering range. In Timing Commander setting window, DPLL bandwidth can be setup as shown in Figure 4:

**Figure 4. Acquisition Bandwidth and Damping Setting for Slave DPLL1**




3. Note that when a device is switched to Slave mode, it can be forced to use an input clock as its reference. In the above example, IN03 (and its associated Sync at IN09) can be a forced input when the device is switched to Slave mode. Forced input is selected by DPLL1_SLAVE_FORCE_REF_SEL_CNFG (0x150, bits [3:0]). In Timing Commander, it's done by selecting IN03 in Master/Slave Mode Configuration Window as shown in Figure 5 below.

**Figure 5. Forced Input Reference In Slave Mode** (see red oval in the figure)




4. DPLL operates in Locked mode.

## 2.2 SYNC Output Alignment Configuration

Both master and slave devices can generate 8K_1PPS FRSYNC and 2K_1PPS MFRSYNC outputs simultaneously alongside the SEC/EEC/PEC outputs.

Each Master-Slave device generates a group of independent clocks including SEC/EEC/PEC clocks, FRSYNC/MFRSYNC signals that are in a defined phase relationship. The SYNC outputs are simply divided from the SEC/EEC/PEC outputs using digital counters. In order for the SYNC outputs from Master and Slave devices to be aligned, the digital counters in the two devices need to be aligned. 82P33xxx provides a functionality to achieve this by sampling the SYNC input (from SYNC output of another device) and using it to synchronize the counters.

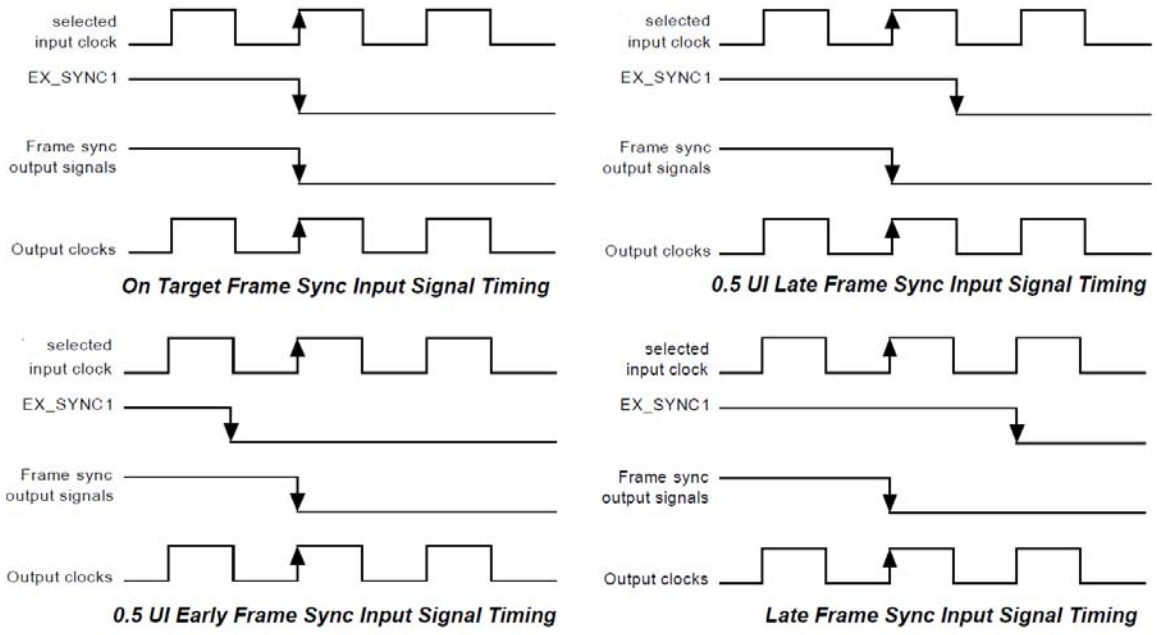
All outputs are synchronous (including the SEC/EEC and SYNC signals). Timing integrity is maintained by the slave device sampling the SYNC input on either edge (rising or falling) of the input reference clock to which the falling edge of the generated Frame SYNC is aligned. All high frequency outputs are rising-edge aligned with the falling edge of the SYNC signal. Please refer to Figure 6 below for phase relationship among 4 signals – input reference clock, input Frame SYNC signal, generated output SYNC signal and the output clocks.

By default, 82P33xxx is configured to sample SYNC input pin on the rising edge of the SEC/EEC clock. Thus, there is approximately ±0.5UI of an SEC/EEC clock of immunity to skew between the SEC/EEC output and output SYNC signal. Locking slave device to an SEC/EEC clock reference ensures that the phase relationship between the sampling clock and the generated clock is maintained.

In order to provide maximum flexibility for immunity to SEC/EEC/PEC and SYNC skew, the 82P33xxx can be programmed to sample the SYNC on the falling edge of the SEC/EEC clock. As the SEC\EEC and SYNC will always be reproduced with their falling edges aligned, 82P33xxx can be programmed to expect the SYNC input to be 0.5UI late or 0.5UI early. In all cases the immunity to skew is ±0.5UI from the expected position.

The result of the configured phase relationship between input and output signals is shown in Figure 6 below. By default, the falling edge of Sync will be aligned (DPLL1_SYNC_EDGE, 0x140, bit 0), the rising edge of the involved input clock can be programed to be aligned with Sync edge (failing or rising) by 0.5UI/1UI early or late (Inx_SYNC_PHASE, address depending on which input).

**Figure 6. Phase Relationship between Input and Output Frame SYNC and Clocks**



## 2.3 1PPS SYNC Configuration

The 1PPS sync signal is synchronized to input clock, i.e., 10MHz GPS reference clock. In 82P33xxx, 1PPS can be generated from 8 output clocks and the 2 Frame SYNC outputs (FRSYNC_8KHz and FRSYNC_2KHz). 1PPS from 8 regular output clock pins will have a nominal 50% duty cycle and its phase alignment can be adjusted by register configurations. The pulse width of the 1PPS output from Frame SYNC outputs can be programmed by setting DPLL1/2_FRSYNC_PULSE and DPLL1/2_MFRSYNC_PULSE registers, respectively.

The 1PPS sync signal output on FRSYNC (1PPS_8KHz) and MRSYNC (1PPS_2KHz) is synchronized with 10 MHz, Ethernet and SONET/SDH clocks. The 1PPS sync signal is not typically synchronized with clocks <10MHz.

## 2.4 Master-Slave Operation

For Master-Slave operations, most of the device configuration is handled by the hardware pin controls on both devices. An external device is required to drive the MS/SL pin on each device. Please note: the two devices should NEVER be configured as Slave at the same time. If both devices are configured as Slave, then a timing "loop" will be created where the two devices try to lock to each other. It is safe, however, for both devices to be configured as Master for a short time during the switchover.

Master-Slave switching by MS/SL pin alone is only suitable for applications where the hitless switch is not required on the Master (see later section). It should also be noted that when the MS/SL pin is driven low to configure the device as a slave. In the Slave, the corresponding registers of the forced functions can still be configured, but their configuration does not take any effect, for example the revertive mode and hitless switch will be disabled when in Slave mode. This behavior will be reflected in the evaluation system GUI.

**Table 2: Initial Set-up of a Master-Slave System**

| Feature | Initial Settings |
|---|---|
| Hitless Switch (HS) | Enabled on *both* devices *if* HS is required on the Master. |
| Non-Revertive mode | Enabled on *both* devices *if* non-revertive mode is required on the Master. |
| Locked bandwidth | Set *both* devices to the required tracking bandwidth when acting as a Master tracking an external reference source,e.g. 1.1Hz |
| Acquisition bandwidth | Set *both* devices to the required tracking bandwidth when acting as a Slave tracking the Master, e.g. 18Hz. |
| Priority of IN03 (IN09 as Sync associated with IN03) | IN03 will be forced to be the input when switched to Slave mode. |
| Priority of IN11 (IN12 as Sync associated with IN11) | IN11 is the input for the device when switched to Master mode. Thus IN11 should have a higher priority. |
| Phase offset control | Set the phase offset in *both* devices to the total characterized delay as follows:<br>(1) Lock one device (the Slave) to the other device (the Master).<br>(2) Measure the phase difference between Master and Slave at one of the I/O cards on the back-plane.<br>(3) Program the phase offset of both devices such that the phase difference measured in (2) becomes as close to zero as possible. |

By using the settings given in the above table, the device will be configured as a Master. When the MS/SL pin is driven low, the settings of some registers are automatically overridden. Overwritten registers/settings by putting the device in Slave mode (MS/SL = "0") include disabling hitless switching, configuring Slave DPLL acquisition bandwidth, etc. Please refer to Section 2.1, “Master–Slave Configuration” above for details.

If device is programmed to enable Hitless Switch, any programmed phase offset would be ignored, and then this will become active when the device is Master. As HS is automatically disabled when the device becomes slave, any programmed phase offset will automatically take over.

The software monitoring functions should also ensure that each device considers the external reference sources in an identical sequence. This is easily achieved by reading the register INn_VALID_DPLLx (n = 1…14, x = 1, 2, 3) from one device and writing it into the other device in the REMOTE_INn_INVALID (n = 1…14). This will ensure that any input considered invalid on one device will also be considered invalid on the other device. Providing that the programmed priorities are identical between the two devices, the active input validation priority table will be identical between the two devices.

Example Sequence of events for a Master-Slave switchover by MS/SL pin control:

- Refer to Figure 1 for system configurations;
- To show how the revertive mode works, another input clock at IN4 (not shown in Figure 1) is added for master device. IN4 will have a lower priority than IN11;
- IN03 is a forced input selection for Slave device;

**Table 3: Example Sequence of Events for a Master-Slave Switchover by MS/SL Pin Control**

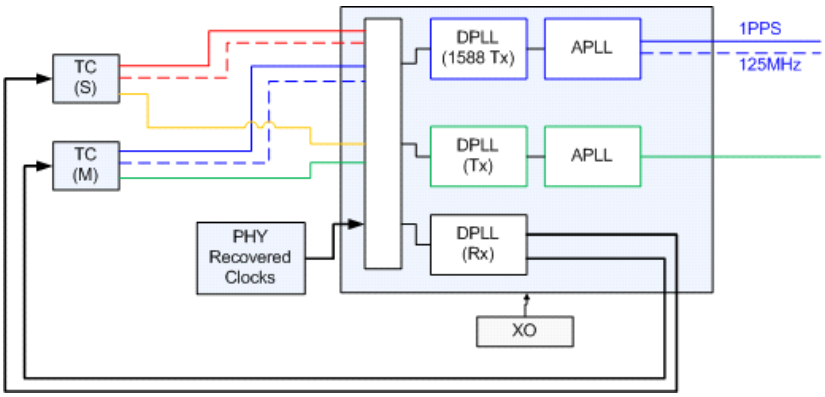
| Device 1 | Device 2 | |
|---|---|---|
| 1. Powers up with MS/SL high - Master mode | Powers up with MS/SL low - Slave mode | |
| 1. Program following settings: | Program following settings: | |
| 2. IN11 priority 1, IN4 priority 2 | IN03 is a forced input | See Section 2.1, “Master–Slave Configuration” |
| 3. All other inputs have priority ignored | All other inputs have priority ignored | |
| 4. Enable HS | Enable HS | Reg 0x117, bit 2 |
| 5. Locked BW = 1.1Hz | Locked BW = 1.1Hz | Reg 0x126, bit [4:0] |
| 6. Acquisition BW = 18Hz | Acquisition BW = 18Hz | Reg 0x125, bit [4:0] |
| 7. Non-Revertive mode enabled | Non-Revertive mode enabled | Reg 0x116, bit 0 |
| 8. External 1PPS/8KHz sync enabled | External 1PPS/8KHz sync enabled | Reg 0x116, bit 6 |
| 9. Automatic external sync enabled | Automatic external sync enabled | Reg 0x116, bit 7 |
| 10. Phase offset programmed to align | Phase offset programmed to align | Reg 0x306/307/30B |
| 11. Device locks to external reference (IN11) with HS | Device locks to IN03 (from Master) with output of Master and Slave closely phase aligned. | |
| 12. Software monitors status registers | Software monitors status registers | |
| **External reference IN11 fails** | | |
| 13. Device detects failure of IN11 and performs hitless switch reference switch to IN4. | Device remains locked to Master, output phase error between Master and Slave remains closely phase aligned. | |
| **External reference IN11 recovers and later fails again** | | |
| 14. Non-revertive mode, so Master takes no action | No change | |
| **External reference IN4 fails** | | |
| 15. Device detects failure of IN4 and enters holdover mode. | Device remains locked to Master, output phase error between Master and Slave remains closely phase aligned. | |
| **External reference IN11 & IN4 recover** | | |
| 16. Device locks to IN11. | Device remains locked to Master. | |
| **System changes Master & Slave arrangement - inverts MS/SL on both devices** | | |

| Device 1 | Device 2 |
|---|---|
| 17. MS\SL goes low–device assumes Slave mode. | MS\SL goes high–device assumes Master mode. |
| 18. Device now disables HS and performs a switch over to the output of Device2. Now tracking phase of new Master. | Device now engages HS and switches over to the highest priority external reference (IN11). |
| 19. Software monitors status register | Software monitors status register |

# 3 Line Card Clock Protection Configurations

Line card will perform non-revertive, hitless reference switching between both (master and slave) timing card references, as illustrated in Figure 7 below.

**Figure 7. In a Master-slave Timing Card Setting, a Line Card Switches between Master and Slave References**




Line card DPLLs will use a wideband filter (>10Hz) with no wander attenuation. Transmit path will attenuate jitter to <1s max RMS (12KHz~20MHz integration range); Receive path will rate-convert recovered line clocks to backplane clocks.

# 4 PTP Clock Protection Configurations

Some users would for T-BC/T-TSC applications, only one PTP port is in slave state; all other PTP ports are in either master or passive state. Only one grander master clock is seen and tracked. When a higher quality or priority master clock is available, or the current master clock is lost, the phase offset from the new grand master is used.

For T-BC application, if an optional PRTC virtual port is available, the 1588 DCO shall hitlessly switch to DPLL mode and acquire the PRTC clock. In this case, since PRTC is deemed to be the highest quality clock, it is assumed that the phase should transition to the PRTC's 1PPS alignment.

If the above optional PRTC virtual port is no longer available, the 1588 DPLL shall hitlessly switch to DCO mode and acquire the PTP clock. In this case, ITU-T has not defined short-term transition response when switching between PRTC reference and PTP reference. However, ITU-T G.8271.1 Appendix V defines 400ns duration allocated for holdover and re-arrangement, which may suggest a means of using phase slope limiting feature supported by 82P338xx.

# 5 Multi-Master Operation

In applications where the Timing Cards do not share synchronization clocks, some users would select the Multi-Master operation. As there are two completely parallel devices, the only task of the software is to ensure that the decisions made by both devices are identical. This is easily achieved by reading registers INn_VALID_DPLLx (n = 1…14, x = 1, 2, 3) from one device and writing it into register REMOTE_INn_INVALID (n = 1…14) of the other device. This will ensure that any input considered invalid on one device will be disabled for locking on the other. Only when both devices consider a reference valid will it be available for locking. If the system does not require Hitless Switch on the 82P33xxx then the outputs of both devices will be in very close alignment. However, if the system does require Hitless Switch then the outputs from the two devices will not be in alignment and the system must be designed to take account of this.

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