8V19N850 Sysref Phase Deterministic and Phase Align

This application note provides 8V19N850 procedures for activating the Sysref for phase deterministic. In addition, it provides examples to determine the global delay for Sysref to clock output Phase alignment.

1. Program Sequence Steps

1. Load general data from all registers 00h to the end for desired I/O frequencies, Feedback Divider, Phase delay, Icp, etc., with some register bits are set as follows:
   - Sequence can be 00 to the end, Reverse registers can be skipped. The register bits are set as follows
   - N_S (R028A D[7:4]), N_SYNC1 (R288 D[6:3]) and N_SYNC0 (R288 D[2:0]), setting:
     i. N_S = 1
     ii. N_SYNC0 and N_SYNC1 divider to achieve target Sysref frequency (e.g., Sysref = 7.68MHz, N_S = 1, N_SYCNC1 = 128, N_SYNC0 = 3)

     If N_S can not be set to 1 to achieve the target Sysref frequency, then the N_SYNC (N_SYNC0 x N_SYNC1) must be LCM of the RFPLL output divider. For example, R0 = 122.88MHz (RFPLL VCO/24), R2 = 491.52MHz (RFPLL VCO/6). Need to be N_SYNC0 x N_SYNC1 = 24.
   - R289 D7 = 0 (PD_S = 0, for Sysref function power on)
   - R28E D7 = 0 (PD_SYSREF, for entire Sysref block and Sysref_r output power on)
   - Make sure individual QREF_Rx outputs that need to be active are not power down, and not Hi-Z.
     i. QREF_R0 - R2F2 D7 = 0 (not power down)
     ii. QREF_R1 - R2F0 D7 = 0 (not power down)
     iii. QREF_R2 - R2EE D7 = 0 (not power down)
     iv. QREF_R3 - R2D6 D7 = 0 (not power down)
     v. QREF_R4 – R2EA D7 = 0 (not power down)
     vi. QREF_R5 - R2E8 D7 = 0 (not power down)
   - R28D D0, R28C D[7:0] = Desired global phase delay (see example of how to get this number provided in this document).
   - Init_ref = 0 (R325, D7 = 0, D = 0)
     i. RELOCK = 1 (R320, D7 = 1, D = 80)
     ii. INIT_CLK_A = 1 (R321, D7 = 1, D = 80)
     iii. INIT_CLK_B = 1 (R322, D7 = 1, D = 80)
     iv. INIT_CLK_C = 1 (R322, D7 = 1, D = 80)
     v. INIT_CLK_D = 1 (R324, D7 = 1, D = 80)

     Note: For EEPROM, INIT_CLK_x, and RELOCK can be set at all 0.
     vi. All Sysref output enable (R327 D0 = 1) - Sysref outputs are still not yet active at this point.

2. Complete this step whenever one of the following parameters must be changed (INIT_CLK_D = 1 (R324, D7 = 1, D = 80):
   - Sysref Global phase delay R28D, R28C
   - QCLK_Rx output phase delay
   - QCLK_Rx output frequency divider

   Note: This step will only interrupt clock outputs that use RFPLL (e.g., Rx outputs or Dx out that select RFPLL). This step will not interrupt output using other APLLs (e.g., Dx that select APLL0).
3. To activate Sysref:

   INIT_REF= 1, Write to Register R325, D7=1 (i.e. D=80) - Sysref output should be active at this point.

   Note: To stop the Sysref, set the Sysref to Limit pulse mode. To Re-activate the Sysref again Set Sysref back to Continuous mode and then write INIT_IREF=1. Do not re-peat step 2 if Global delay is not changed.
   - E.g. In internal trigger mode and set the Sysref in limit pulse mode to stop the Sysref, R28E SRG = 011, SRO = 00.
   - To re-activate the Sysref again, SRG = 100, and INIT_IREF = 1 (R325, D7 = 1).

   Note: This step will not interrupt D and R Clock outputs.
4. Adjust individual Sysref phase delay in order to not interrupt phase.
   - QREF_R0 – Register R2F3, D[3:0]
   - QREF_R1 – Register R2F1, D[3:0]
   - QREF_R2 – Register R2EF, D[3:0]
   - QREF_R3 – Register R2ED, D[3:0]
   - QREF_R4 – Register R2EB, D[3:0]
   - QREF_R5 – Register R2E9, D[3:0]

2. Experiment Examples to Determine Sysref Global Phase Delay Registers 28D, 28C Setting

Scope channel assignment:

- CH3 = QCLK_R (RFPLL Output CLOCK)
- CH4 = QREF_R (Sysref output)

2.1 Example 1: Set Global Delay

1. Start with Setting Global Delay R28D[D7] = 0, R28C = 0. QREF phase = 0ps, R0 = 0ps.
2. Complete steps 2 and Step 3 in the **Programming Sequence Steps**.

   The Sysref and R0 Clock output can be shown as Figure 1. The delay between Sysref rising edge and next Clock rising edge ~7.4ns. The delay is used to determine the Sysref global delay setting.

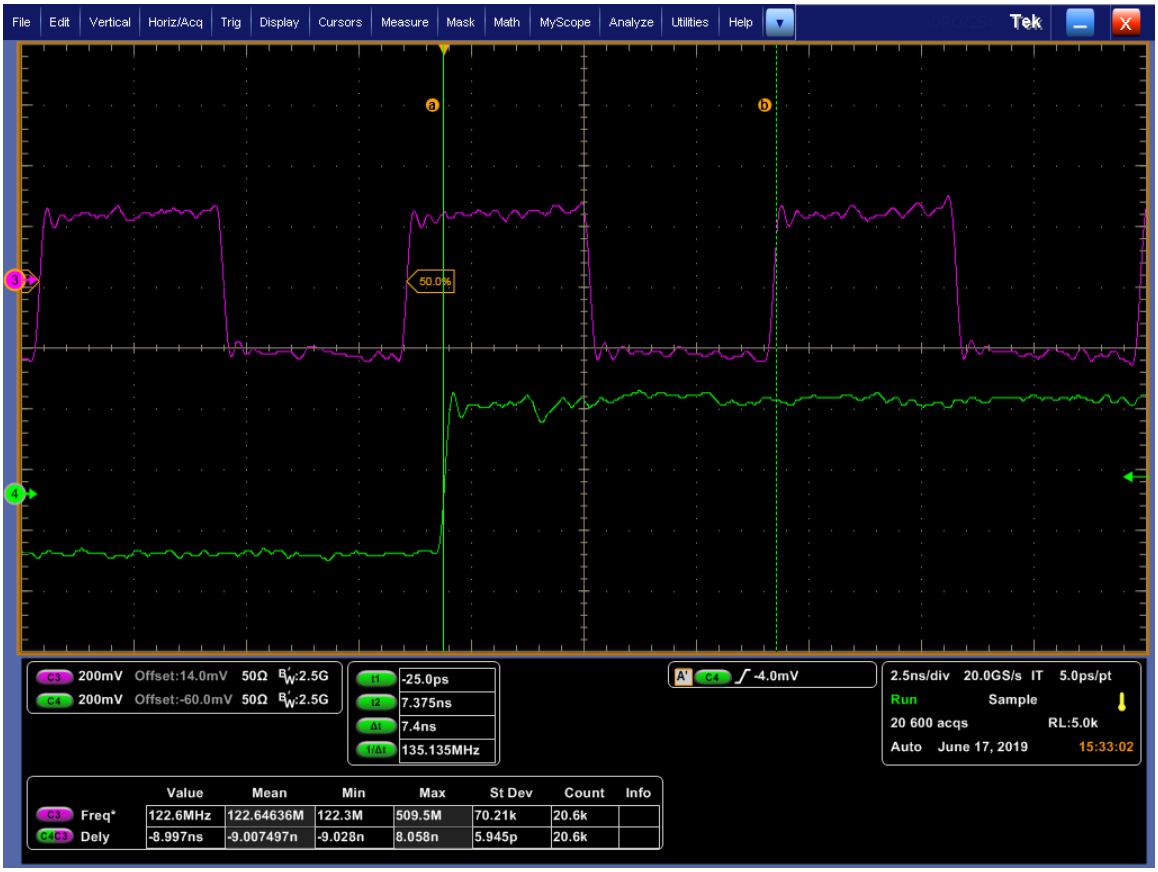

Figure 1. Initial Sysref to QCLK Delay with Sysref Global Delay = 0ps

2.2 Example 2: Re-adjust Global Delay

1. Complete step 2 (INIT_CLK_D) in the **Programming Sequence Steps** again. For example, if user intent to delay Sysref rising edge by 7.4ns.

   For Global phase delay of 169ps per step, set R28C = 44 (i.e., 7.4ns / 169ps~44).

2. Repeat Steps 2 (INIT_CLK_D) and 3 (the waveform is shown in Figure 2). Note that the Sysref rising edge shifts to near phase align to slightly lead the R0 clock output rising edge. Step 2 (INIT_CLK) will interrupt the Rx clock outputs but this will not interrupt other outputs that do not use RF_PLL (e.g., QCLK_Dx outputs that do not use the RFPLL).

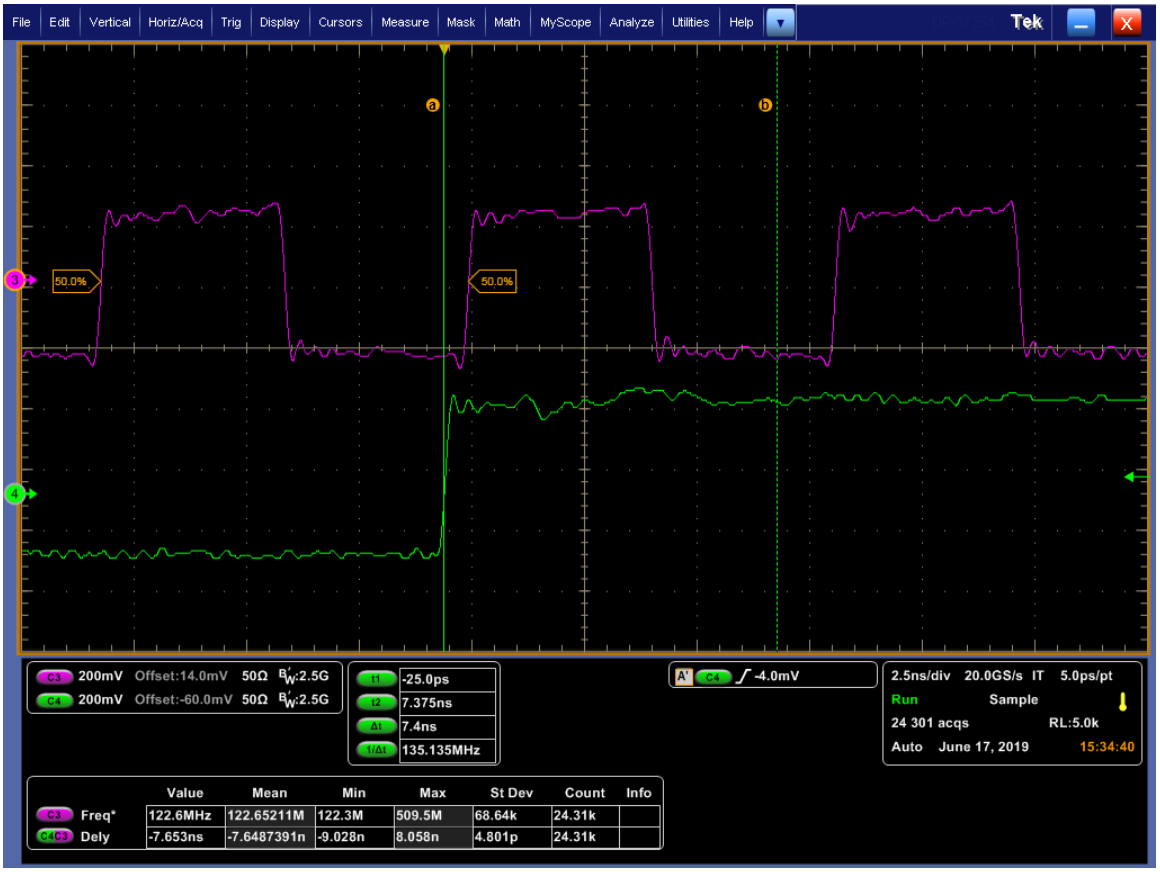

Figure 2. Sysref to QCLK Delay after Updating Sysref Global Phase Delay

2.3 Example 3: Set Individual Delay

1. Perform step 4 in the **Programming Sequence Steps** (Register 2F3 for QREF_R0) with various individual Sysref delay setting with different value, Sysref rising edge to R0 Clock rising edge change as shown in Figure 3. The Rx Clock output are not interrupted.

   (In the scope we need to set the trigger to the lower frequency signal which is Sysref in this case, so the R0 Clock signal is moving for each step setting).

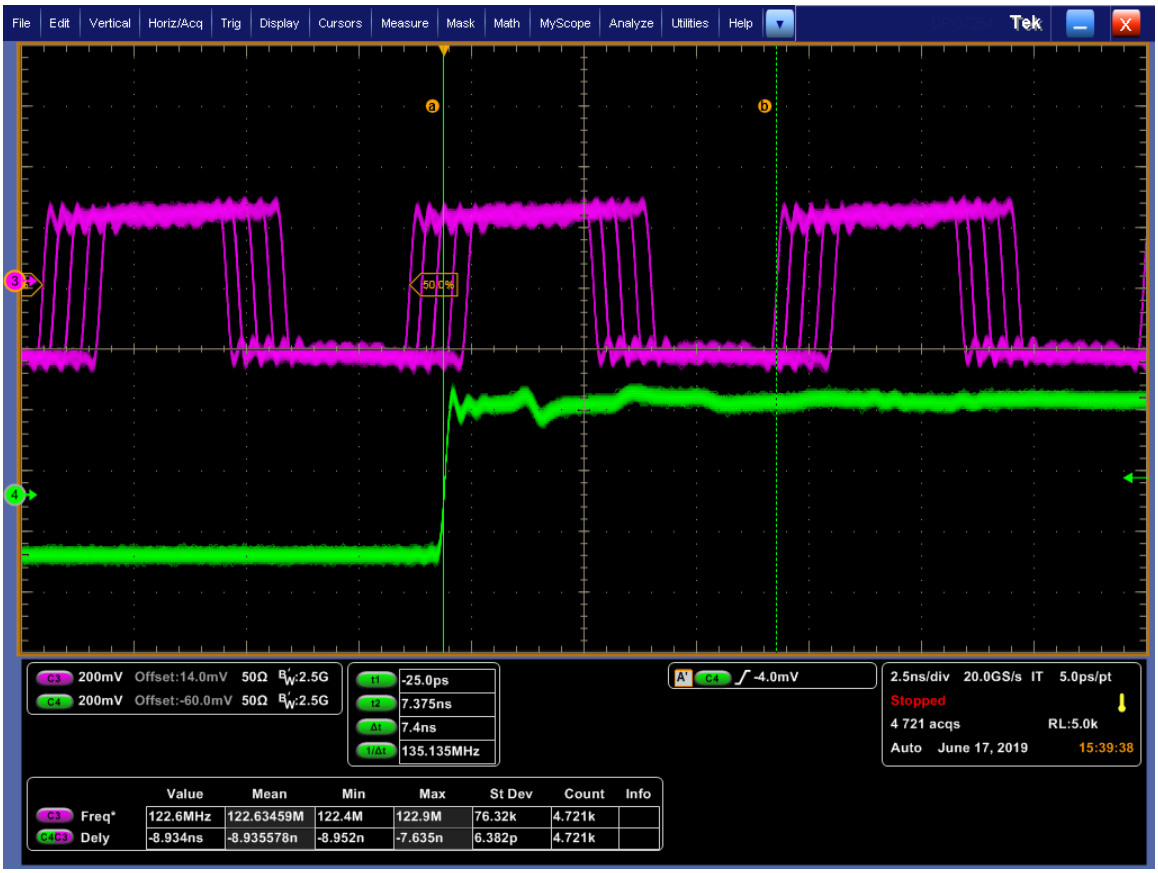

Figure 3. Result of Adjusting Individual Sysref Phase Delay

3. Revision History

Revision	Date	Description
1.0	Mar 25, 2021	Initial release.

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